TSV STRUCTURE PLANARIZATION PROCESS AND APPARATUS

BACKGROUND OF THE INVENTION

1. Field of the Invention

[0001] The present invention generally relates to semiconductor device manufacture, and more particularly to a TSV (through-silicon-via) structure planarization process and apparatus.

2. The Related Art

[0002] With the rapid development of electronic industry, the demand on mini-size, low power consumption and high reliability becomes inevitable to electronic products. Based on Moore's law, decreasing the feature size of integrated circuits is approaching a bottleneck. In recent years, wafer-level vertical miniaturization 3D through-silicon-via (TSV) and 2.5D interposer package integration are becoming an alternative solution to break through the bottleneck of Moore's law by down scaling in design, process and cost. Correspondingly, due to copper's higher conductivity, better electromigration resistance, the copper is widely used to fill vias when making TSV or interposer.

[0003] Conventionally, a copper metal layer deposition and planarization process includes following steps: PVD (physical vapor deposition), ECP (electro-chemical plating), annealing, CMP (chemical-mechanical-planarization). Vias in TSV or interposer are commonly with high aspect ratio. In order to void-free fill the deep vias, a thick overburden copper layer will be deposited on a surface of a substrate by plating process. Hence, huge amount of copper layer needs to remove by CMP, which causes the CMP process costs the most in 3D TSV and 2.5D interposer package integration. For example, in a via-middle process, the CMP process occupies 35% of total cost. On the other hand, the huge CTE (coefficient of thermal expansion)

mismatch between Cu and Si causes stress which is shown as wafer level warpage. The stress further induces micro-crack in Si layer, carrier's mobility change and device defect. It's proved that higher annealing temperature and thicker overburden copper layer result in higher wafer level warpage. During the CMP process, the substrate will be flattened by CMP head's down press. The external mechanical pressure will conflict with the substrate internal stress and induce the substrate cracking or defect. Although the conventional process route is optimized and the copper overburden thickness is minimized before anneal, which can successfully release the stress and minimize the substrate warpage before CMP, however, whether 3D TSV or 2.5D interposer can be rapid industrialization, depends on the solution to reduce the cost and stress.

SUMMARY

[0004] In an embodiment, the present invention provides a TSV structure planarization process. The TSV structure includes a substrate, vias formed in the substrate, an oxide layer formed on the substrate, a barrier layer formed on the oxide layer, bottom and sidewall of the vias, a metal layer formed in the vias and on the barrier layer. The TSV structure planarization process comprises: removing all metal layer formed on a non-recessed area of the substrate by a stress-free polishing process; and removing metal layer residual and the barrier layer on the non-recessed area by a chemical wet etch process.

[0005] In another embodiment, the present invention provides a TSV structure planarization process. The TSV structure includes a substrate, vias formed in the substrate, an oxide layer formed on the substrate, a barrier layer formed on the oxide layer, bottom and sidewall of the vias, a metal layer formed in the vias and on the barrier layer. The TSV structure planarization process comprises: removing a large proportion of metal layer on a non-recessed area of the substrate by a stress-free polishing process and remaining a certain thickness of the metal layer on the non-

recessed area; removing the remained metal layer on the non-recessed area by a metal layer chemical wet etch process; and removing metal layer residual and the barrier layer on the non-recessed area by a barrier layer chemical wet etch process.

[0006] In another embodiment, the present invention provides a TSV structure planarization process. The TSV structure includes a substrate, vias formed in the substrate, an oxide layer formed on the substrate, a barrier layer formed on the oxide layer, bottom and sidewall of the vias, a metal layer formed in the vias and on the barrier layer. The TSV structure planarization process comprises: removing all metal layer formed on a non-recessed area of the substrate by a stress-free polishing process; removing metal layer residual on the non-recessed area by a chemical-mechanical-planarization process; and removing the barrier layer on the non-recessed area by a barrier layer chemical wet etch process.

[0007] In another embodiment, the present invention provides a TSV structure planarization process. The TSV structure includes a substrate, vias formed in the substrate, an oxide layer formed on the substrate, a barrier layer formed on the oxide layer, bottom and sidewall of the vias, a metal layer formed in the vias and on the barrier layer. The TSV structure planarization process comprises: removing a large proportion of metal layer on a non-recessed area of the substrate and remaining a certain thickness of the metal layer on the non-recessed area; removing the remained metal layer on the non-recessed area by a chemical-mechanical-planarization process; and removing metal layer residual and the barrier layer on the non-recessed area by a barrier layer chemical wet etch process.

[0008] In an embodiment, the present invention provides a TSV structure planarization apparatus. The TSV structure includes a substrate, vias formed in the substrate, an oxide layer formed on the substrate, a barrier layer formed on the oxide layer, bottom and sidewall of the vias, a metal layer formed in the vias and on the barrier layer. The TSV structure planarization apparatus comprises at least one SFP module, a CMP module and a wet etch module. The at least one SFP module is used

for applying a stress-free polishing process to the substrate to remove the metal layer on a non-recessed area of the substrate. The CMP module is used for applying a chemical-mechanical-planarization process to the substrate to remove the metal layer on the non-recessed area. The wet etch module is used for applying a chemical wet etch process to the substrate to remove the metal layer and/or the barrier layer on the non-recessed area.

[0009] Comparing to a conventional TSV structure planarization process, which uses the CMP process to remove the metal layer and the barrier layer on the non-recessed area, the present invention utilizes the stress-free polishing process and the chemical wet etch process to stress-free remove the metal layer and the barrier layer on the non-recessed area, just retaining the metal layer and the barrier layer in the vias, which improves the metal layer dishing uniformity, reduces stress during the planarization process, minimizes the opportunity of the substrate micro-crack, and shortens the CMP process duration, finally reduces the planarization process cost and reduces waste chemical drain.

BRIEF DESCRIPTION OF THE DRAWINGS

[0010] FIG. 1 is a cross-sectional view showing an exemplary TSV structure before carrying out planarization process.

[0011] FIG. 2 is a cross-sectional view showing the TSV structure which has been flattened.

[0012] FIG. 3 is a flow chart showing a TSV structure planarization process according to an embodiment of the present invention.

[0013] FIG. 4 is a flow chart showing a TSV structure planarization process according to another embodiment of the present invention.

[0014] FIG. 5 is a flow chart showing a TSV structure planarization process according to another embodiment of the present invention.

[0015] FIG. 6 is a flow chart showing a TSV structure planarization process according to another embodiment of the present invention.

[0016] FIG. 7 is a flow chart showing a TSV structure planarization process according to another embodiment of the present invention.

[0017] FIG. 8 is a flow chart showing a TSV structure planarization process according to another embodiment of the present invention.

[0018] FIG. 9 shows an exemplary wet etch pulse mode recipe.

[0019] FIG. 10 is a block diagram showing a TSV structure planarization apparatus according to the present invention.

[0020] FIG. 11 is a block diagram showing a substrate transferring sequence.

[0021] FIG. 12 is a block diagram showing another substrate transferring sequence.

DETAILED DESCRIPTION OF EMBODIMENTS

[0022] A process sequence of forming a TSV structure generally includes the following steps: forming vias 102 in a substrate 101 by etching, wherein the material of the substrate 101 can select silicon; depositing an oxide layer 103 on the substrate 101 by plasma enhanced chemical vapor deposition (PECVD), wherein the material of the oxide layer 103 can select silicon dioxide (SiO_2); depositing a barrier layer 104 on the oxide layer 103, the bottom and the sidewall of the vias 102 by physical vapor deposition (PVD), wherein the material of the barrier layer 104 can select titanium (Ti); depositing a metal layer 105 in the vias 102 by electrochemical plating, wherein the material of the metal layer 105 can select copper.

[0023] Because the vias 102 of the TSV structure normally have high aspect ratio, therefore, in order to void-free deposit the metal layer 105 in the vias 102, a thick overburden metal layer 105 is deposited on the barrier layer 104 by electrochemical plating. As shown in FIG. 1, an exemplary TSV structure before

carrying out planarization process is illustrated. The thickness of the metal layer 105 deposited on a non-recessed area is about 2um-4um. After depositing the metal layer 105 in the vias 102 and on the non-recessed area, a subsequent step is to remove the metal layer 105 and the barrier layer 104 deposited on the non-recessed area.

[0024] Referring to FIG. 3, FIG. 3 is a flow chart showing a TSV structure planarization process for removing the metal layer 105 and the barrier layer 104 formed on the non-recessed area according to an embodiment of the present invention. The TSV structure planarization process includes the following steps:

[0025] Step 301: removing all metal layer 105 deposited on the non-recessed area by a stress-free polishing (SFP) process. A metal layer dishing in the via 102 is controlled by SFP over polish. The SFP process is a chemical-electrical process. The metal layer 105 on the substrate 101 is as anode and an electrolyte nozzle is as cathode. The metal layer 105 is dissolved and polished by the contacted electrolyte when a positive voltage is applied between the anode and the cathode. For more detailed description of the SFP process, see U.S. patent application Ser. No. 10/590,460, entitled "Controlling removal rate uniformity of an electropolishing process in integrated circuit fabrication", filed on February 23, 2005, the entire content of which is incorporated herein by reference.

[0026] Step 303: removing metal layer residual on the non-recessed area by a metal layer chemical wet etch process. After the SFP process, there maybe some metal layer residual is remained on the barrier layer 104 on the non-recessed area. In order to remove the metal layer residual remaining on the barrier layer 104 on the non-recessed area, the metal layer chemical wet etch process is applied to remove the metal layer residual. The material of the metal layer 105 preferably selects copper, and correspondingly, the etchant for removing copper residual mainly contains hydrogen peroxide (H_2O_2), additive and hydrofluoric acid, and the concentration of the hydrofluoric acid is in the range of 2% to 10%. In the wet etch process, the etchant will be ejected to the surface of the substrate in pulse mode, as shown in FIG. 9. One

pulse mode step is combined with a step of etchant and a step of DIW, for example, firstly 10 sec chemical wet etch is applied to the substrate, after that, a 5 sec DIW is applied to the substrate. A plurality of periodical steps form a wet etch process recipe. The periodical wet etch process will optimize the recessed area copper dishing. The DIW will fill in the recessed area and reduce the etch rate of this area. The substrate is fixed on a chuck, and is rotated with the chuck. The favor substrate spin speed for the wet etch process is from 200RPM to 600RPM. The removal profile is related to the spin speed. The higher spin speed induces the higher substrate edge removal rate and lower substrate center removal rate; and conversely, the lower spin speed induces the lower substrate edge removal rate and higher substrate center removal rate. Furthermore, the etchant nozzle is movable during the process. The etch rate is influenced by the nozzle scan speed and scan area. The optimal scan speed is in range of 40mm/sec to 100mm/sec.

[0027] Step 305: removing the barrier layer 104 on the non-recessed area by a barrier layer chemical wet etch process. The thickness of the barrier layer 104 on the non-recessed area is about 0.2um-0.5um, which is depended on process request. The material of the barrier layer 104 contains Ti, and correspondingly, the chemical for the barrier layer chemical wet etch process mainly contains hydrofluoric acid (HF) and additive, and the concentration of the hydrofluoric acid is in the range of 0.1% to 1%. As similar with the copper wet etch process, in the barrier layer wet etch process, the etchant will be ejected to the surface of the substrate in pulse mode. As shown in FIG. 9, one pulse mode step is combined with a step of etchant and a step of DIW, for example, firstly 10 sec chemical wet etch is applied to substrate, after that, a 5 sec DIW is applied to the substrate. A plurality of periodical steps form a wet etch process recipe. The periodical wet etch process will optimize the barrier layer on the side wall of the recessed area over etch. The DIW will fill in the recessed area and reduce the etch rate of this area. The substrate is fixed on a chuck, and is rotated with the chuck. The favor substrate spin speed for the wet etch process is from 200RPM to 600RPM. The removal profile is related to the spin speed. The higher spin speed induces the

higher substrate edge removal rate and lower substrate center removal rate; and conversely, the lower spin speed induces the lower substrate edge removal rate and higher substrate center removal rate. Furthermore, the etchant nozzle is movable during the process. The etch rate is influenced by the nozzle scan speed and scan area. The optimal scan speed is in range of 40mm/sec to 100mm/sec.

[0028] After the barrier layer 104 on the non-recessed area is removed by the barrier layer chemical wet etch process, the oxide layer 103 under the barrier layer 104 is exposed. The material of the oxide layer 103 is SiO_2, and the thickness of the oxide layer 103 is about 2um. In order to achieve a flat top surface, preferably, a CMP process is applied to remove a part of the oxide layer 103. Normally, the removal thickness of the oxide layer 103 is 0.2um. The CMP process has a high selectivity between the oxide layer 103 and the copper metal layer 105, such as 100:1. The CMP process can recover the roughness of the copper metal layer 105 in the via 102.

[0029] Referring to FIG. 4, FIG. 4 is a flow chart showing a TSV structure planarization process for removing the metal layer 105 and the barrier layer 104 formed on the non-recessed area according to another embodiment of the present invention. The TSV structure planarization process includes the following steps:

[0030] Step 401: removing all metal layer 105 deposited on the non-recessed area by a stress-free polishing (SFP) process. A metal layer dishing in the via 102 is controlled by SFP over polish. The SFP process is a chemical-electrical process. The metal layer 105 on the substrate 101 is as anode and an electrolyte nozzle is as cathode. The metal layer 105 is dissolved and polished by the contacted electrolyte when a positive voltage is applied between the anode and the cathode. For more detailed description of the SFP process, see U.S. patent application Ser. No. 10/590,460, entitled "Controlling removal rate uniformity of an electropolishing process in integrated circuit fabrication", filed on February 23, 2005, the entire content of which is incorporated herein by reference.

[0031] Step 403: removing metal layer residual and the barrier layer 104 on the non-recessed area by a barrier layer chemical wet etch process. In an embodiment, the material of the metal layer 105 is copper and the material of the barrier layer 104 contains Ti. The chemical for the barrier layer chemical wet etch process mainly contains hydrofluoric acid (HF) and additive, and the concentration of the hydrofluoric acid is in the range of 0.1% to 1%. In the barrier layer wet etch process, the etchant will be ejected to the surface of the substrate in pulse mode. As shown in FIG. 9, one pulse mode step is combined with a step of etchant and a step of DIW, for example, firstly 10 sec chemical wet etch is applied to substrate, after that, a 5 sec DIW is applied to the substrate. A plurality of periodical steps form a wet etch process recipe. The periodical wet etch process will optimize the barrier layer on the side wall of the recessed area over etch. The DIW will fill in the recessed area and reduce the etch rate of this area. The substrate is fixed on a chuck, and is rotated with the chuck. The favor substrate spin speed for the wet etch process is from 200RPM to 600RPM. The removal profile is related to the spin speed. The higher spin speed induces the higher substrate edge removal rate and lower substrate center removal rate; and conversely, the lower spin speed induces the lower substrate edge removal rate and higher substrate center removal rate. Furthermore, the etchant nozzle is movable during the process. The etch rate is influenced by the nozzle scan speed and scan area. The optimal scan speed is in range of 40mm/sec to 100mm/sec.

[0032] After the metal layer residual and the barrier layer 104 on the non-recessed area are removed by the barrier layer chemical wet etch process, the oxide layer 103 under the barrier layer 104 is exposed. The material of the oxide layer 103 is SiO_2, and the thickness of the oxide layer 103 is about 2um. In order to achieve a flat top surface, preferably, a CMP process is applied to remove a part of the oxide layer 103. Normally, the removal thickness of the oxide layer 103 is 0.2um. The CMP process has a high selectivity between the oxide layer 103 and the copper metal layer 105, such as 100:1. The CMP process can recover the roughness of the copper metal layer 105 in the via 102.

[0033] Referring to FIG. 5, FIG. 5 is a flow chart showing a TSV structure planarization process for removing the metal layer 105 and the barrier layer 104 formed on the non-recessed area according to another embodiment of the present invention. The TSV structure planarization process includes the following steps:

[0034] Step 501: removing a large proportion of metal layer 105 on the non-recessed area by a SFP process and remaining about 0.2um-0.5um metal layer 105 on the non-recessed area. The SFP process is a chemical-electrical process. The metal layer 105 on the substrate 101 is as anode and an electrolyte nozzle is as cathode. The metal layer 105 is dissolved and polished by the contacted electrolyte when a positive voltage is applied between the anode and the cathode. For more detailed description of the SFP process, see U.S. patent application Ser. No. 10/590,460, entitled "Controlling removal rate uniformity of an electropolishing process in integrated circuit fabrication", filed on February 23, 2005, the entire content of which is incorporated herein by reference.

[0035] Step 503: removing the remained metal layer 105 on the non-recessed area by a metal layer chemical wet etch process. A metal layer dishing in the via 102 is controlled by the over etch time length of the metal layer chemical wet etch process. The material of the metal layer 105 is copper. The chemical for the copper layer chemical wet etch process mainly contains hydrogen peroxide (H_2O_2), additive and hydrofluoric acid, and the concentration of the hydrofluoric acid is in the range of 2% to 10%. In the wet etch process, the etchant will be ejected to the surface of the substrate in pulse mode, as shown in FIG. 9. One pulse mode step is combined with a step of etchant and a step of DIW, for example, firstly 10 sec chemical wet etch is applied to the substrate, after that, a 5 sec DIW is applied to the substrate. A plurality of periodical steps form a wet etch process recipe. The periodical wet etch process will optimize the copper dishing in the recessed area. The DIW will fill in the recessed area and reduce the etch rate of this area. The substrate is fixed on a chuck, and is rotated with the chuck. The favor substrate spin speed for the wet etch process is from 200RPM to 600RPM. The removal profile is related to the spin speed. The higher spin

speed induces the higher substrate edge removal rate and lower substrate center removal rate; and conversely, the lower spin speed induces the lower substrate edge removal rate and higher substrate center removal rate. Furthermore, the etchant nozzle is movable during the process. The etch rate is influenced by the nozzle scan speed and scan area. The optimal scan speed is in range of 40mm/sec to 100mm/sec.

[0036] Step 505: removing metal layer residual and the barrier layer 104 on the non-recessed area by a barrier layer chemical wet etch process. The material of the barrier layer 104 contains Ti. The chemical for the barrier layer chemical wet etch process mainly contains hydrofluoric acid (HF) and additive, and the concentration of the hydrofluoric acid is in the range of 0.1% to 1%. In the barrier layer wet etch process, the etchant will be ejected to the surface of the substrate in pulse mode. As shown in FIG. 9, one pulse mode step is combined with a step of etchant and a step of DIW, for example, firstly 10 sec chemical wet etch is applied to substrate, after that, a 5 sec DIW is applied to the substrate. A plurality of periodical steps form a wet etch process recipe. The periodical wet etch process will optimize the barrier layer on the side wall of the recessed area over etch. The DIW will fill in the recessed area and reduce the etch rate of this area. The substrate is fixed on a chuck, and is rotated with the chuck. The favor substrate spin speed for the wet etch process is from 200RPM to 600RPM. The removal profile is related to the spin speed. The higher spin speed induces the higher substrate edge removal rate and lower substrate center removal rate; and conversely, the lower spin speed induces the lower substrate edge removal rate and higher substrate center removal rate. Furthermore, the etchant nozzle is movable during the process. The etch rate is influenced by the nozzle scan speed and scan area. The optimal scan speed is in range of 40mm/sec to 100mm/sec.

[0037] After the metal layer residual and the barrier layer 104 on the non-recessed area are removed by the barrier layer chemical wet etch process, the oxide layer 103 under the barrier layer 104 is exposed. The material of the oxide layer 103 is SiO_2, and the thickness of the oxide layer 103 is about 2um. In order to achieve a flat top surface, preferably, a CMP process is applied to remove a part of the oxide layer

103. Normally, the removal thickness of the oxide layer 103 is 0.2um. The CMP process has a high selectivity between the oxide layer 103 and the copper metal layer 105, such as 100:1. The CMP process can recover the roughness of the copper metal layer 105 in the via 102.

[0038] Referring to FIG. 6, FIG. 6 is a flow chart showing a TSV structure planarization process for removing the metal layer 105 and the barrier layer 104 formed on the non-recessed area according to another embodiment of the present invention. The TSV structure planarization process includes the following steps:

[0039] Step 601: removing all metal layer 105 deposited on the non-recessed area by a stress-free polishing (SFP) process. A metal layer dishing in the via 102 is controlled by SFP over polish. The SFP process is a chemical-electrical process. The metal layer 105 on the substrate 101 is as anode and an electrolyte nozzle is as cathode. The metal layer 105 is dissolved and polished by the contacted electrolyte when a positive voltage is applied between the anode and the cathode. For more detailed description of the SFP process, see U.S. patent application Ser. No. 10/590,460, entitled "Controlling removal rate uniformity of an electropolishing process in integrated circuit fabrication", filed on February 23, 2005, the entire content of which is incorporated herein by reference.

[0040] Step 603: removing metal layer residual on the non-recessed area by a chemical-mechanical-planarization (CMP) process. After the SFP process, there maybe some metal layer residual is remained on the barrier layer 104 on the non-recessed area. In order to remove the metal layer residual, the chemical-mechanical-planarization process is applied to the substrate 101 to remove the metal layer residual. Since almost all metal layer on the non-recessed area is removed by the SFP process, therefore, the process time of the CMP process is short, which saves cost and avoids damage to the substrate.

[0041] Step 605: removing the barrier layer 104 on the non-recessed area by a barrier layer chemical wet etch process. The thickness of the barrier layer 104 on the

non-recessed area is about 0.2um-0.5um. The thickness of the barrier layer 104 on the non-recessed area is depended on process request. The material of the barrier layer 104 contains Ti, and correspondingly, the chemical for the barrier layer chemical wet etch process mainly contains hydrofluoric acid (HF) and additive, and the concentration of the hydrofluoric acid is in the range of 0.1% to 1%. In the barrier layer wet etch process, the etchant will be ejected to the surface of the substrate in pulse mode. As shown in FIG. 9, one pulse mode step is combined with a step of etchant and a step of DIW, for example, firstly 10 sec chemical wet etch is applied to substrate, after that, a 5 sec DIW is applied to the substrate. A plurality of periodical steps form a wet etch process recipe. The periodical wet etch process will optimize the barrier layer on the side wall of the recessed area over etch. The DIW will fill in the recessed area and reduce the etch rate of this area. The substrate is fixed on a chuck, and is rotated with the chuck. The favor substrate spin speed for the wet etch process is from 200RPM to 600RPM. The removal profile is related to the spin speed. The higher spin speed induces the higher substrate edge removal rate and lower substrate center removal rate; and conversely, the lower spin speed induces the lower substrate edge removal rate and higher substrate center removal rate. Furthermore, the etchant nozzle is movable during the process. The etch rate is influenced by the nozzle scan speed and scan area. The optimal scan speed is in range of 40mm/sec to 100mm/sec.

[0042] After the barrier layer 104 on the non-recessed area is removed by the barrier layer chemical wet etch process, the oxide layer 103 under the barrier layer 104 is exposed. The material of the oxide layer 103 is SiO_2, and the thickness of the oxide layer 103 is about 2um. In order to achieve a flat top surface, preferably, a CMP process is applied to remove a part of the oxide layer 103. Normally, the removal thickness of the oxide layer 103 is 0.2um. The CMP process has a high selectivity between the oxide layer 103 and the copper metal layer 105, such as 100:1. The CMP process can recover the roughness of the copper metal layer 105 in the via 102.

[0043] Referring to FIG. 7, FIG. 7 is a flow chart showing a TSV structure planarization process for removing the metal layer 105 and the barrier layer 104

formed on the non-recessed area according to another embodiment of the present invention. The TSV structure planarization process includes the following steps:

[0044] Step 701: removing a large proportion of metal layer 105 on the non-recessed area by a SFP process and remaining about 0.2um-0.5um metal layer 105 on the non-recessed area. The SFP process is a chemical-electrical process. The metal layer 105 on the substrate 101 is as anode and an electrolyte nozzle is as cathode. The metal layer 105 is dissolved and polished by the contacted electrolyte when a positive voltage is applied between the anode and the cathode. For more detailed description of the SFP process, see U.S. patent application Ser. No. 10/590,460, entitled "Controlling removal rate uniformity of an electropolishing process in integrated circuit fabrication", filed on February 23, 2005, the entire content of which is incorporated herein by reference.

[0045] Step 703: removing the remained metal layer 105 on the non-recessed area by a chemical-mechanical-planarization process. A metal layer dishing in the via 102 is controlled by the over polish time length of the chemical-mechanical-planarization process. The material of the metal layer 105 is copper.

[0046] Step 705: removing metal layer residual and the barrier layer 104 on the non-recessed area by a barrier layer chemical wet etch process. The material of the barrier layer 104 contains Ti. The chemical for the barrier layer chemical wet etch process mainly contains hydrofluoric acid (HF) and additive, and the concentration of the hydrofluoric acid is in the range of 0.1% to 1%. In the barrier layer wet etch process, the etchant will be ejected to the surface of the substrate in pulse mode. As shown in FIG. 9, one pulse mode step is combined with a step of etchant and a step of DIW, for example, firstly 10 sec chemical wet etch is applied to substrate, after that, a 5 sec DIW is applied to the substrate. A plurality of periodical steps form a wet etch process recipe. The periodical wet etch process will optimize the barrier layer on the side wall of the recessed area over etch. The DIW will fill in the recessed area and reduce the etch rate of this area. The substrate is fixed on a chuck, and is rotated with

the chuck. The favor substrate spin speed for the wet etch process is from 200RPM to 600RPM. The removal profile is related to the spin speed. The higher spin speed induces the higher substrate edge removal rate and lower substrate center removal rate; and conversely, the lower spin speed induces the lower substrate edge removal rate and higher substrate center removal rate. Furthermore, the etchant nozzle is movable during the process. The etch rate is influenced by the nozzle scan speed and scan area. The optimal scan speed is in range of 40mm/sec to 100mm/sec.

[0047] After the metal layer residual and the barrier layer 104 on the non-recessed area are removed by the barrier layer chemical wet etch process, the oxide layer 103 under the barrier layer 104 is exposed. The material of the oxide layer 103 is SiO_2, and the thickness of the oxide layer 103 is about 2um. In order to achieve a flat top surface, preferably, a CMP process is applied to remove a part of the oxide layer 103. Normally, the removal thickness of the oxide layer 103 is 0.2um. The CMP process has a high selectivity between the oxide layer 103 and the copper metal layer 105, such as 100:1. The CMP process can recover the roughness of the copper metal layer 105 in the via 102.

[0048] Referring to FIG. 8, FIG. 8 is a flow chart showing a TSV structure planarization process for removing the metal layer 105 and the barrier layer 104 formed on the non-recessed area according to another embodiment of the present invention. The TSV structure planarization process includes the following steps:

[0049] Step 801: removing a large proportion of metal layer 105 on the non-recessed area by a metal layer chemical wet etch process and remaining about 0.2um-0.5um metal layer 105 on the non-recessed area. The material of the metal layer 105 preferably selects copper, and correspondingly, the chemical for copper chemical wet etch process mainly contains hydrogen peroxide (H_2O_2), additive and hydrofluoric acid, and the concentration of the hydrofluoric acid is in the range of 2% to 10%.

[0050] Step 803: removing the remained metal layer 105 on the non-recessed area by a chemical-mechanical-planarization process. A metal layer dishing in the via

102 is controlled by the over polish time length of the chemical-mechanical-planarization process.

[0051] Step 805: removing metal layer residual and the barrier layer 104 on the non-recessed area by a barrier layer chemical wet etch process. The material of the barrier layer 104 contains Ti. The chemical for the barrier layer chemical wet etch process mainly contains hydrofluoric acid (HF) and additive, and the concentration of the hydrofluoric acid is in the range of 0.1% to 1%.

[0052] After the metal layer residual and the barrier layer 104 on the non-recessed area are removed by the barrier layer chemical wet etch process, the oxide layer 103 under the barrier layer 104 is exposed. The material of the oxide layer 103 is SiO_2, and the thickness of the oxide layer 103 is about 2um. In order to achieve a flat top surface, preferably, a CMP process is applied to remove a part of the oxide layer 103. Normally, the removal thickness of the oxide layer 103 is 0.2um. The CMP process has a high selectivity between the oxide layer 103 and the copper metal layer 105, such as 100:1. The CMP process can recover the roughness of the copper metal layer 105 in the via 102.

[0053] Referring to FIG. 10, FIG. 10 is a block diagram showing a TSV structure planarization apparatus according to the present invention. The apparatus includes an EFEM (Equipment Front End Module) 1001, a buffer station 1003, a process robot 1005, two SFP modules 1007 which are stacked, a CMP module 1009, a metrology module 1011, a brush clean module 1013, a wet etch module 1015 and a clean module 1017. The metrology module 1011 and the brush clean module 1013 are stacked. The wet etch module 1015 and the clean module 1017 are stacked. The apparatus also includes an electrical module, a gas module and a plumbing module. The SFP module 1007 is used for applying a stress-free polishing process to the substrate to remove the metal layer on the non-recessed area of the substrate. The CMP module 1009 is used for applying a chemical-mechanical-planarization process to the substrate to remove the metal layer on the non-recessed area. The wet etch

module 1015 is used for applying a chemical wet etch process to the substrate to remove the metal layer and/or the barrier layer on the non-recessed area. The chemical wet etch process includes a metal layer chemical wet etch process and/or a barrier layer chemical wet etch process. The wet etch process takes a pulse mode and each pulse mode step is combined with a step of etchant and a step of DIW.

[0054] Referring to FIG. 11, FIG. 11 is a block diagram showing an exemplary substrate transferring sequence. An EFEM robot takes an unprocessed substrate from a load port and transfers the substrate to the buffer station 1003. The process robot 1005 takes the substrate from the buffer station 1003 and transfers the substrate to the metrology module 1011 for measuring the thickness of the metal layer. After the metrology module 1011 measuring the thickness of the metal layer, the process robot 1005 takes the substrate from the metrology module 1011 and transfers the substrate to one of the SFP modules 1007. In the SFP module 1007, a SFP process is applied to the substrate to remove all metal layer on the non-recessed area. After the SFP process is completed, the process robot 1005 takes the substrate from the SFP module 1007 and transfers the substrate to the clean module 1017 for cleaning the substrate. Then the process robot 1005 takes the substrate from the clean module 1017 and transfers the substrate to the CMP module 1009. In the CMP module 1009, a CMP process is applied to the substrate to remove metal layer residual on the non-recessed area. After the CMP process is completed, the process robot 1005 takes the substrate from the CMP module 1009 and transfers the substrate to the brush clean module 1013 for cleaning the substrate. Then the process robot 1005 takes the substrate from the brush clean module 1013 and transfers the substrate to the wet etch module 1015. In the wet etch module 1015, a barrier layer chemical wet etch process is applied to the substrate to remove the barrier layer on the non-recessed area. After the barrier layer chemical wet etch process is completed, the process robot 1005 takes the substrate from the wet etch module 1015 and transfers the substrate to the clean module 1017 for cleaning the substrate. Then the process robot 1005 takes the substrate from the clean module 1017 and transfers the substrate to the buffer station 1003. At last, the EFEM robot takes the

substrate from the buffer station 1003 and transfers the substrate to the substrate load port.

[0055] If the CMP module 1009 has no function of measuring the thickness of the metal layer, before applying the CMP process to the substrate, the substrate should be transferred to the metrology module 1011 to measure the post SFP metal layer thickness, as shown in FIG. 12.

[0056] Besides the above substrate transferring sequences, other substrate transferring sequences can be carried out according to different process demands by using the apparatus.

[0057] As described above, comparing to a conventional TSV structure planarization process, which uses the CMP process to remove the metal layer and the barrier layer on the non-recessed area, and a part of the oxide layer, the present invention utilizes the SFP process, the metal layer chemical wet etch process and the barrier layer chemical wet etch process to stress-free remove the metal layer 105 and the barrier layer 104 on the non-recessed area, just retaining the metal layer 105 and the barrier layer 104 in the vias 102, as shown in FIG. 2, which improves the TSV structure metal layer dishing uniformity, reduces stress during the planarization process, minimizes the opportunity of the substrate micro-crack, and shortens the CMP process duration, finally reduces the planarization process cost and reduces waste chemical drain.

[0058] The foregoing description of the present invention has been presented for purposes of illustration and description. It is not intended to be exhaustive or to limit the invention to the precise form disclosed, and obviously many modifications and variations are possible in light of the above teaching. Such modifications and variations that may be apparent to those skilled in the art are intended to be included within the scope of this invention as defined by the accompanying claims.

CLAIMS

1. A TSV structure planarization process, wherein the TSV structure includes a substrate, vias formed in the substrate, an oxide layer formed on the substrate, a barrier layer formed on the oxide layer, bottom and sidewall of the vias, a metal layer formed in the vias and on the barrier layer, wherein the TSV structure planarization process comprises:

removing most of the metal layer formed at a non-recessed area of the substrate by a stress-free polishing process; and

removing metal layer residual and the barrier layer formed at the non-recessed area by a chemical wet etch process,

wherein the chemical wet etch process comprises a plurality of periodical pulse mode steps, each pulse mode step including applying an etchant on the non-recessed area for a first period of time, and applying DIW on the non-recessed area for a second period of time.

2. The TSV structure planarization process as claimed in claim 1, wherein the chemical wet etch process includes a barrier layer chemical wet etch process.

3. The TSV structure planarization process as claimed in claim 2, wherein a material of the metal layer is copper and a material of the barrier layer contains titanium, and the etchant for the barrier layer chemical wet etch process contains hydrofluoric acid and an additive.

4. The TSV structure planarization process as claimed in claim 1, wherein the step of removing metal layer residual and the barrier layer formed at the non-recessed area by a chemical wet etch process further comprises:

removing metal layer residual formed at the non-recessed area of the substrate by a metal layer chemical wet etch process; and

removing the barrier layer formed at the non-recessed area by a barrier layer chemical wet etch process.

5. The TSV structure planarization process as claimed in claim 4, wherein a material of the metal layer is copper, and the etchant for the metal layer chemical wet etch process contains hydrogen peroxide, an additive and hydrofluoric acid.

6. The TSV structure planarization process as claimed in claim 4, wherein a material of the barrier layer contains titanium, and the etchant for the barrier layer chemical wet etch process contains hydrofluoric acid and an additive.

7. The TSV structure planarization process as claimed in claim 1, wherein after the metal layer residual and the barrier layer formed at the non-recessed area are removed by the chemical wet etch process, the oxide layer under the barrier layer is exposed, and a part of the oxide layer is removed by a CMP process.

8. The TSV structure planarization process as claimed in claim 1, wherein the oxide layer is SiO_2.

9. A TSV structure planarization process, wherein the TSV structure includes a substrate, vias formed in the substrate, an oxide layer formed on the substrate, a barrier layer formed on the oxide layer, bottom and sidewall of the vias, a metal layer formed in the vias and on the barrier layer, wherein the TSV structure planarization process comprises:

removing a large proportion of metal layer formed at a non-recessed area of the substrate by a stress-free polishing process and remaining a certain thickness of the metal layer on the non-recessed area;

removing most of the remaining metal layer formed at the non-recessed area by a metal layer chemical wet etch process,

wherein the metal layer chemical wet etch process comprises a plurality of periodical pulse mode steps, each pulse mode step including applying a first etchant on the non-recessed area for a first period of time, and applying DIW on the non-recessed area for a second period of time; and

removing metal layer residual and the barrier layer formed at the non-recessed area by a barrier layer chemical wet etch process,

wherein the barrier layer chemical wet etch process comprises a plurality of periodical pulse mode steps, each pulse mode step including applying a second etchant on the non-recessed area for a third period of time, and applying DIW on the non-recessed area for a fourth period of time.

10. The TSV structure planarization process as claimed in claim 9, wherein the thickness of the remaining metal layer on the non-recessed area after the stress-free polishing process is 0.2um-0.5um.

11. The TSV structure planarization process as claimed in claim 9, wherein a material of the metal layer is copper, and the first etchant for the metal layer chemical wet etch process contains hydrogen peroxide, an additive and hydrofluoric acid.

12. The TSV structure planarization process as claimed in claim 9, wherein a material of the barrier layer contains titanium, and the second etchant for the barrier layer chemical wet etch process contains hydrofluoric acid and an additive.

13. The TSV structure planarization process as claimed in claim 9, wherein after the metal layer residual and the barrier layer formed at the non-recessed area are removed, the oxide layer under the barrier layer is exposed and a part of the oxide layer is removed by a CMP process.

14. A TSV structure planarization process, wherein the TSV structure includes a substrate, vias formed in the substrate, an oxide layer formed on the substrate, a barrier layer formed on the oxide layer, bottom and sidewall of the vias, a metal layer formed in the vias and on the barrier layer, wherein the TSV structure planarization process comprises:

removing most of the metal layer formed at a non-recessed area of the substrate by a stress-free polishing process;

removing metal layer residual formed at the non-recessed area by a chemical-mechanical-planarization process; and

removing the barrier layer formed at the non-recessed area by a barrier layer chemical wet etch process,

wherein the barrier layer chemical wet etch process comprises a plurality of periodical pulse mode steps, each pulse mode step including applying an etchant on the non-recessed area for a first period of time, and applying DIW on the non-recessed area for a second period of time.

15. The TSV structure planarization process as claimed in claim 14, wherein a material of the barrier layer contains titanium, and the etchant for the barrier layer chemical wet etch process contains hydrofluoric acid and an additive.

16. The TSV structure planarization process as claimed in claim 14, wherein after the barrier layer formed at the non-recessed area is removed, the oxide layer under the barrier layer is exposed, and a part of the oxide layer is removed by a CMP process.

17. A TSV structure planarization process, wherein the TSV structure includes a substrate, vias formed in the substrate, an oxide layer formed on the substrate, a barrier layer formed on the oxide layer, bottom and sidewall of the vias, a metal layer

formed in the vias and on the barrier layer, wherein the TSV structure planarization process comprises:

removing a large proportion of the metal layer formed at a non-recessed area of the substrate by a stress-free polishing process or a metal layer chemical wet etch process and remaining a certain thickness of the metal layer on the non-recessed area;

removing most of the remaining metal layer formed at the non-recessed area by a chemical-mechanical-planarization process; and

removing metal layer residual and the barrier layer formed at the non-recessed area by a barrier layer chemical wet etch process,

wherein the barrier layer chemical wet etch process comprises a plurality of periodical pulse mode steps, each pulse mode step including applying a first etchant on the non-recessed area for a first period of time, and applying DIW on the non-recessed area for a second period of time.

18. The TSV structure planarization process as claimed in claim 17, wherein a material of the metal layer is copper, and a second etchant for the metal layer chemical wet etch process contains hydrogen peroxide, an additive and hydrofluoric acid.

19. The TSV structure planarization process as claimed in claim 17, wherein the metal layer chemical wet etch process comprises a plurality of periodical pulse mode steps, each pulse mode step including applying the second etchant on the non-recessed area for a third period of time, and applying DIW on the non-recessed area for a fourth period of time.

20. The TSV structure planarization process as claimed in claim 17, wherein a material of the barrier layer contains titanium, and the first etchant for the barrier layer chemical wet etch process contains hydrofluoric acid and an additive.

21. The TSV structure planarization process as claimed in claim 17, wherein the thickness of the remaining metal layer on the non-recessed area is 0.2um-0.5um.

22. The TSV structure planarization process as claimed in claim 17, wherein after the metal layer residual and the barrier layer formed at the non-recessed area are removed, the oxide layer under the barrier layer is exposed, and a part of the oxide layer is removed by a CMP process.

23. A TSV structure planarization apparatus, wherein the TSV structure includes a substrate, vias formed in the substrate, an oxide layer formed on the substrate, a barrier layer formed on the oxide layer, bottom and sidewall of the vias, a metal layer formed in the vias and on the barrier layer, wherein the TSV structure planarization apparatus comprises:

at least one SFP module for applying a stress-free polishing process to the substrate to remove the metal layer on a non-recessed area of the substrate;

a CMP module for applying a chemical-mechanical-planarization process to the substrate to remove the metal layer on the non-recessed area; and

a wet etch module for applying a chemical wet etch process to the substrate to remove the metal layer and/or the barrier layer formed at the non-recessed area,

wherein the chemical wet etch process comprises a plurality of periodical pulse mode steps, each pulse mode step including applying an etchant on the non-recessed area for a first period of time, and applying DIW on the non-recessed area for a second period of time.

24. The TSV structure planarization apparatus as claimed in claim 31, wherein the chemical wet etch process includes a metal layer chemical wet etch process and/or a barrier layer chemical wet etch process.

25. The TSV structure planarization apparatus as claimed in claim 31, further comprising:

a metrology module for measuring the thickness of the metal layer;

a brush clean module for cleaning the substrate after the chemical-mechanical-planarization process; and

a clean module for cleaning the substrate after the stress-free polishing process or the chemical wet etch process.