

METHOD AND CIRCUIT FOR CORRECTING IMAGE EDGE

5 The present invention relates to an image edge correcting circuit and method for a digital image processor.

10 Firstly, examples of circuits of prior art will be described, with reference to Figures 1 to 4 of the accompanying diagrammatic drawings, in which:

Figure 1 is a diagram of a first example of an edge correcting circuit of the prior art;

15 Figure 2 is a waveforms diagram relating to Figure 1;

Figure 3 is a diagram of a second example of an edge correcting circuit of the prior art;

20 Figure 4 is a waveforms diagram relating to Figure 3;

25 - A known example of a general edge correcting circuit for an image in a television is composed as shown in Figure 1 and uses a correcting method to sharpen a edge of an image on a CRT which extracts outline components of an image luminance signal "Y" by passing a band pass filter or a high pass filter, mixes the extracted signal with a gain control signal in a multiplier (2), and then adds the image luminance signal "Y" to the mixed signal in an adder (3).

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Referring now to the waveforms of Figure 2, when the image luminance signal "Y" is as in "2a" of Figure 2, the extracted edge of the image luminance signal "Y" through the filter (1) is as in "2b" of Figure 2. After the edge
35 of the image luminance signal "Y" is extracted, the

extracted edge components signal "2b" of the image
luminance signal "Y" is mixed with a gain control signal
by the multiplier (2), and then added to the image
luminance signal "Y" at the adder (3) to output a final
5 edge-corrected signal "2c". If the final edge- corrected
signal as in "2c" is scanned on a CRT, a difference of the
luminance signal between a dark portion and a bright
portion is about "H2", which is more effective than "H1"
which results by scanning the image luminance signal "Y"
10 as "2a". Therefore, the general edge correcting circuit
for an image which extracts an image edge helps viewers to
enjoy a vivid image by increasing contrast of an edge.

Also, by using a digital differential amplifier as in
15 Figure 3, the edge correcting circuit for an image stated
above can become a digital edge correcting circuit. By
sampling and quantizing the analog image luminance signal
"Y", the analog image luminance signal "Y" becomes a
digital image luminance signal Y. as shown in "4a" of
20 Figure 4. After the digital image luminance signal Y. as
"4a" goes through a first delay circuit (102), the signal
is delayed as in "4b", and the digital luminance signal
"4b" passed through the first delay circuit (102) becomes
as in "4c" after a second delay circuit (103). A signal
25 as in "4d" is obtained at a first subtractor "104" by
subtracting the digital luminance signal "4a" from the
first delayed digital luminance signal "4b", and a signal
as in "4e" is obtained at a second subtractor (105) by
subtracting the second delayed digital luminance signal
30 "4c" from the first delayed digital luminance signal "4b".
A signal "4f" is generated at a first adder (106) by
adding the signal "4d" from the first subtractor (104) and
the signal "4e" from the second subtractor (105). The
signal "4f" from the first adder (106) is mixed with an
35 external gain control signal, by means of a multiplier

(107), and then added to a signal from a delay circuit (101) at a second adder (108) to generate an edge-corrected digital luminance signal for an image "4g". The edge-corrected digital luminance signal for an image
5 "4g" is converted to an analog signal as shown in dotted line, by D/A converter (not shown).

In the first edge-correcting circuit as in Figure 1 or the second edge-correcting circuit as in Figure 3,
10 delay-correction differs according to a constitution of a filter (2) or the first and second subtractors (104) and (105), and a frequency band for edge-correction is determined. Thus, the conventional method uses the image luminance signal for correcting a edge region. Hence,
15 when the image is displayed on a CRT or a Display Unit, the conventional method sharpens an edge region by increasing a difference of level of a luminance signal at boundary region, whether the circuit is used in an analog system or digital system.

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However, when the stated conventional method is used to correct the edge of a bright boundary region such as white captions and capitals, an excessive current flows at the edge of the boundary region. Thus, the conventional
25 method can have the drawback that a blurring phenomenon is caused around the boundary region as a result of the excessive current.

According to one aspect of the present invention, an
30 edge correction method is provided for reducing level transition times of a luminance signal in a digital image processor, the method comprising the steps of:

(a) generating a first control signal by detecting the imminent onset of a signal level transition where a luminance signal starts to change;

5 (b) generating a second control signal by detecting the imminent termination of a signal level transition prior to luminance signal stabilization;

10 (c) converting and outputting a pixel level state which is the same as a pixel level state before onset of said signal level transition, so as to delay the onset of said transition while only said first control signal is being generated;

15 (d) outputting a pixel level state which is the same as a pixel level state after a complete signal level transition, so as to speed up the completion of said transition while only said second control signal is being generated; and

20 (e) when neither said first nor said second control signal is generated, or, when both said first and said second control signal are generated, outputting a stable pixel level state.

25 According to a second aspect of the invention, there is provided an edge correction circuit for reducing level transition times of a luminance signal in a digital image processor, the circuit comprising:

30 a first control signal generator which generates a first control signal by detecting the imminent onset of a signal level transition where said luminance signal starts
35 to change; and

a second control signal generator which generates a said second control signal by detecting the imminent termination of a signal level transition prior to luminance signal stabilization;

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wherein: while said first control signal is being generated, a pixel level state is converted and output, the pixel level state being the same as a pixel level state prior to the onset of said signal level transition; while said second control signal is being generated a pixel level state is converted and output which is the same as a pixel level state following a complete signal level transition; and when neither said first control signal nor said second control signal is generated, or, when both said first and second control signals are generated, converting and outputting a stabilized pixel level state.

Preferably, the circuit comprises:

20 first and second delay circuits which are in serial connection -and generate second and third luminance signals, which are delayed by given amounts with respect to a reference luminance signal;

25 first and second subtractors which generate signal differences by subtracting the second luminance signal and third luminance signal from the reference luminance signal and the second luminance signal, respectively;

30 first and second absolute value circuits which convert outputs from said first and second subtractors to provide first and second absolute values;

35 first and second comparators which reduce noise in said first and second absolute values by comparing outputs

from said first and second absolute value circuits with a given reference signal; and

5 a first gate which generates the second control signal at a point when a level of said third luminance signal changes to a stable state signal level from an unstable state signal level by logically multiplying an inverse output signal of said first comparator by an output signal of said second comparator.

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The circuit preferably further comprises:

15 third and fourth delay circuits which are in serial connection and generate fourth and fifth luminance signals by delaying said third luminance signal by given amounts;

20 third and fourth subtractors which generate signal differences by subtracting said fourth luminance signal and said fifth luminance signal from said third luminance signal and said fourth luminance signal, respectively;

25 third and fourth absolute value circuits which convert outputs from said third and said fourth subtractors to provide third and fourth absolute values;

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third and fourth comparators which reduce noise in said third and fourth absolute values by comparing outputs from said third and fourth absolute value circuits with the given reference signal; and

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a second gate which generates the first control signal at a point when a level of said third luminance signal changes to an unstable state signal level from a stable state signal level by logically multiplying an

output signal of said third comparator by an inverse output signal of said fourth comparator.

Preferably, a data selector is provided in which said
5 third luminance signal is connected to first and fourth
input terminals of said data selector, said second
luminance signal is connected to a second input terminal
of said data selector, and said fourth luminance signal is
connected to a third input terminal of said data selector,
10 wherein said data selector is arranged so as to
selectively output said fourth luminance signal while said
first control signal is generated, and two selectively
output said second luminance signal while said second
control signal is generated.

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The invention includes a digital image processor adapted to perform the method of the first aspect or including a circuit according to the second aspect.

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For a better understanding of the invention and to show how the same may be carried into effect, reference will now be made, by way of example, to Figures 5 to 7 of the accompanying diagrammatic drawings, in which:

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Figure 5 is one example of an edge correcting circuit according to the present invention;

Figure 6 is a waveforms diagram relating to Figure 5;
and

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Figure 7 is a comparative diagram of waveforms in edge correction.

Referring to Figure 5, first through fourth delay
35 circuits (11-14) which are connected in series delay a

digitized first luminance signal for an image by a prescribed unit, and generate second through fifth luminance signals for an image respectively. First through fourth subtractors (21-24) generate first through
5 fourth subtracted signals by subtracting a first through fourth luminance signals from second through fifth luminance signals respectively. First through fourth absolute value circuits (31-34) calculate absolute values from the first through fourth subtracted signals. First
10 through fourth comparators (41-44) generate first through fourth noise reduced compared signals by comparing a given reference signal with outputs from the first through fourth absolute value circuits (31-34). A first gate (51) generates a second control signal by logically multiplying
15 an inverse signal of the first compared signal by the second compared signal. A second gate (52) generates a first control signal by logically multiplying an inverse signal of the fourth compared signal by the third compared signal. A data selector (60) outputs selectively any one
20 of the second through fourth luminance signals for an image by taking the first and second control signals as selective signals after inputting the third luminance signal to the first and the fourth input terminals, the second luminance signal to the second input terminal, and
25 the fourth luminance signal to the third input terminal.

Therefore, by correcting an edge of the image luminance signal according to the above constitution, the correction time at a level-variation region of the image
30 luminance signal is reduced. In other words, a edge portion of the luminance signal becomes less since the data selector (60) outputs the third luminance signal when the first and the second control signals are "00" or "11", outputs the second luminance signal when the first and the
35 second control signals are "01", and outputs the fourth

luminance signal when the first and the second control signals are "10".

In the waveforms diagram of Figure 6:

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Waveforms "6A-6E" are the first through fifth luminance signals;

10 Waveforms "6F-6I" are the first through fourth compared signals;

Waveforms "6J-6K" are the first and the second control signals; and

15 Waveform "6L" is the final corrected luminance signal which is output from the data selector (60) according to the first and second control signals.

20 Figure 7 is a comparative diagram of waveforms relating to an edge correcting circuit of the prior art and to the illustrated example of an edge correcting circuit of the present invention.

25 The illustrated embodiment of the present invention is now described in more detail, with reference to Figures 5, 6, and 7.

30 When the digitized luminance signal "6A" is input into the first through fourth delay circuits (11-14) in series, the second through fifth luminance signals which are delayed by the delay circuits are generated as shown in "6B-6E" respectively. The first through fourth delay circuits (11-14) can consist of D flip-flops, and a delay unit of the delay circuit is one sampling clock cycle to
35 delay the luminance signal. Thus, the first through fifth

luminance signals are the luminance signals which are successively delayed by one sampling period interval. In an actual digital signal processing circuit, a sampled quantized step value is held for one sampling clock period, but is shown as a dot in Figure 6 for ease of explanation. Therefore, the dot in Figure 6 means a sampled luminance signal.

The first through fourth luminance signals as in "6A-6D" and the second through fifth luminance signals as in "6B-6E" are applied to the first through fourth subtractors (21-24) respectively. The first through fourth subtractors subtract one signal from the other, resulting in a zero, positive value, or negative value. If the result is not zero, it means that the level of the luminance signal is changing. Therefore, the first subtractor (21) outputs a non-zero positive data at "t2", "t3", and "t4" of Figure 6. Also, the first subtractor (21) outputs non-zero negative data at "t10", "t11", and "t12" of Figure 6. The outputs from the first through the fourth subtractors at "t1-t16" of Figure 6 can be shown as in Table 1.

TABLE 1		
	RESULT	
	POSITIVE	NEGATIVE
FIRST SUBTRACTOR	t2-t4	t10-t12
SECOND SUBTRACTOR	t3-t5	t11-t13
THIRD SUBTRACTOR	t4-t6	t12-t14
FOURTH SUBTRACTOR	t5-t7	t13-t15

As shown in table 1, the first through fourth subtractors (21-24) output either a positive or a negative value where the level of luminance signal changes. The outputs from the first through fourth subtractors (21-24) are applied to the first through fourth absolute value circuits (31-34) respectively and became same valued positive numbers regardless of their signs. Thus, the negative data from the first through fourth subtractors (21-24) are converted to positive data, by passing the first through fourth absolute value circuits (31-34). The outputs from the first through fourth absolute value circuits (31-34) are applied to the first through fourth comparators (41-44) for a comparison with the external reference signal from outside. When the output signal from the absolute value circuits (31-34) is greater than the reference signal, a logical high signal ("1") as in (6F-6I) is generated. The reason for a comparison between the reference signal and the signals from the first through fourth subtractors at the first through fourth comparators (41-44) is to prevent a malfunction by removing noise using the reference signal since there can be a difference even though two identical luminance signals are applied to the subtractor, due to noise in an actual luminance signal.

Therefore, the first through fourth comparators prevent a malfunction due to noise in the luminance signal, and generate a logical high signal ("1") when a difference in the delayed signal is higher than the given reference level, that is, when the level of the luminance signal is changing with time. Also, when a difference in the delayed signal is lower than the given reference level - that is, when the level of the luminance signal is not changing with time, a logical zero signal ("0") is generated. Therefore, when the first luminance signal as

in "6A" which stays at black level for a specific period and then changes to white level which changes back to black level after a specific period enters and is delayed by one sampling period interval at the first through the
5 fourth delay circuits (11-14) as in "6B-6E". The first and the fourth compared signals as in "6F-6I" are generated only during a transitional period where the level of the luminance signal is changing.

10 At the first gate (51), the second compared signal and the inverse signal of the first compared signal are logically multiplied to generate the second control signal "6K". At the second gate (52), the third compared signal and the inverse signal of the fourth compared signal are
15 logically multiplied to generate the first control signal "6J". Thus, the first control signal becomes the logical signal "1" when the level of a base signal changes from one to the other as in "t4" and "t12" of "6J" if the third luminance signal such as "6C" (that is, a two-times
20 sampling period delayed signal of the first luminance signal) is used as a reference signal. Otherwise, the first control signal stays as logical zero. Also, the second control signal becomes a logical "1" signal just before a stable state from a state where the level of a
25 signal changes as in "t5" and "t13" of "6K" if the third luminance signal as "6C" is used as a reference signal. Otherwise, the second control signal stays as logical zero. Therefore, the first and the second control signals are "00" when the third control signal such as "6C" is the
30 first and second luminance signals before delay and the fourth and fifth luminance signals after delay that are not changed and will not be changed in compared value. The first and second control signals become "10" where the third luminance signal starts to change its level from the
35 stable state and becomes "01" just before the third

luminance signal starts to stabilize from a changing state.

5 The first and the second control signals which change
as stated above are applied to the data selector (60) as
a selection control signal. The data selector (60) takes
the third luminance signal as an input to the first and
the fourth input terminals, the second luminance signal as
an input to the second input terminal, and the fourth
10 luminance signal as an input to the third input terminal.
Therefore, the data selector (60) outputs by selecting the
third luminance signal when the first and the second
control signals are "00" or "11", outputs by selecting the
fourth luminance signal when the control signals are "10"
15 as in "t4" and "t12", and outputs by selecting the second
luminance signal when the control signals are "01" as in
"t5" and "t13". Therefore, a final luminance signal from
the data selector "60" becomes the edge corrected signal
which requires less conversion time where the level of the
20 luminance signal changes, as shown "6L" of Figure 6.

As shown in Figure 7, the edge correction is achieved
by reducing the conversion time and detecting a starting
point and an ending point of a edge region in a signal,
25 that is by outputting data just before a change as in "7C"
where the luminance signal "7A" starts to change as in
"T1" and "T3", and outputting data from a stabilized point
where the point just before the stabilization from a
changing state starts as in "T2" and "T4". Thus, as shown
30 in "7B", it is possible to display the luminance signal
vividly by reducing the time to change levels as in "7C"
without changing an amplitude of a signal level during the
edge correction.

In addition, if the components in Figure 5 are connected in multiple steps series, a certain edge correction can be achieved even though the time for the luminance signal level change is increased.

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As stated above, by applying the edge correcting circuit in a digital image processor, a sharp edge of an image can be effectively generated regardless of a contrast in a pixel of a boundary region by reducing the conversion time of a signal level in the edge of the image.

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Although specific constructions and procedures of the invention have been illustrated and described herein, this is by way of example only, and it is not intended that the invention be limited to the elements, the constructions and the method disclosed. One skilled in the art will easily recognize that the particular elements, subconstructions and similar methods may be used without departing from the scope of the invention.

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CLAIMS:

1. An edge correction method for reducing level transition times of a luminance signal in a digital image processor, the method comprising the steps of:

(a) generating a first control signal by detecting the imminent onset of a signal level transition where a luminance signal starts to change;

(b) generating a second control signal by detecting the imminent termination of a signal level transition prior to luminance signal stabilization;

(c) converting and outputting a pixel level state which is the same as a pixel level state before onset of said signal level transition, so as to delay the onset of said transition while only said first control signal is being generated;

(d) converting and outputting a pixel level state which is the same as a pixel level state after a complete signal level transition, so as to speed up the completion of said transition while only said second control signal is being generated; and

(e) when neither said first nor said second control signal is generated, or, when both said first and said second control signal are generated, outputting a stable pixel level state.

2. An edge correction circuit for reducing level transition times of a luminance signal in a digital image processor, the circuit comprising:



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a first control signal generator which generates a first control signal by detecting the imminent onset of a signal level transition where said luminance signal starts to change; and

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a second control signal generator which generates a said second control signal by detecting the imminent termination of a signal level transition prior to luminance signal stabilization;

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wherein: while said first control signal is being generated, a pixel level state is converted and output, the pixel level state being the same as a pixel level state prior to the onset of said signal level transition;

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while said second control signal is being generated a pixel level state is converted and output which is the same as a pixel level state following a complete signal level transition; and when neither said first control signal nor said second control signal is generated, or, when both said first and second control signals are generated, a stabilized pixel level state is converted and output.

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3. An edge correction circuit as claimed in claim 2, comprising:

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first and second delay circuits which are in serial connection and generate second and third luminance signals, which are delayed by given amounts with respect to a reference luminance signal;

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first and second subtractors which generate signal differences by subtracting the second luminance signal and third luminance signal from the reference luminance signal and the second luminance signal, respectively;

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first and second absolute value circuits which convert outputs from said first and second subtractors to provide first and second absolute values;

5 first and second comparators which reduce noise in said first and second absolute values by comparing outputs from said first and second absolute value circuits with a given reference signal; and

10 a first gate which generates the second control signal at a point when a level of said third luminance signal changes to a stable state signal level from an unstable state signal level by logically multiplying an inverse output signal of said first comparator by an
15 output signal of said second comparator.

4. An edge correction circuit as claimed in claim 3, comprising:

20 third and fourth delay circuits which are in serial connection and generate fourth and fifth luminance signals by delaying said third luminance signal by given amounts;

third and fourth subtractors which generate signal
25 differences by subtracting said fourth luminance signal and said fifth luminance signal from said third luminance signal and said fourth luminance signal, respectively;

third and fourth absolute value circuits which
30 convert outputs from said third and said fourth subtractors to provide third and fourth absolute values;

third and fourth comparators which reduce noise in said third and fourth absolute values by comparing outputs



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from said third and fourth absolute value circuits with the given reference signal; and

5 a second gate which generates the first control signal at a point when a level of said third luminance signal changes to an unstable state signal level from a stable state signal level by logically multiplying an output signal of said third comparator by an inverse output signal of said fourth comparator.

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5. An edge correction circuit as claimed in claim 4, wherein: a data selector is provided in which said third luminance signal is connected to first and fourth input terminals of said data selector, said second luminance signal is connected to a second input terminal of said data selector, and said fourth luminance signal is connected to a third input terminal of said data selector, wherein said data selector is arranged so as to selectively output said fourth luminance signal while said first control signal is generated, and to selectively output said second luminance signal while said second control signal is generated.

25 6. An edge correction circuit substantially as hereinbefore described with reference to Figures 5 to 7 of the accompanying drawing.

30 7. An edge correction method substantially as herein described with reference to Figures 5 to 7 of the accompanying drawings.

8. A digital image processor adapted to perform an edge correction method according to claim 1 or claim 7, or provided with an edge correction circuit according to any of claims 2 to 6.

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