

ABSTRACT

A nonvolatile memory device includes a first pin that receives a first signal, a second pin that receives a second signal, third pins that receive third signals, a fourth pin that receives a write enable signal, a memory cell array, and a memory interface circuit that obtains a command, an address, and data from the third signals in a first mode and obtains the command and the address from the first signal and the second signal and the data from the third signals in a second mode. In the first mode, the memory interface circuit obtains the command from the third signals and obtains the address from the third signals. In the second mode, the memory interface circuit obtains the command from the first signal and the second signal and obtains the address from the first signal and the second signal.

FIG. 2