

Description

The invention relates to evaluation or analysing circuits for passive measuring detectors or measured value receivers having ohmic sensor impedances in bridge connections with adjustment of the output signals of the receivers provided by continuously modulated change-over of a resistor, which is controlled into one change-over position by the overflow signal of a clock pulse counter and into the other change-over position by the output signal of a digital comparator that compares the contents of the clock pulse counter and a forward/backward counter connected to the output of a sign-sensitive voltage-frequency transformer, whose input voltage consists of an amplified balancing difference signal that is rectified by a phase-sensitive rectifier and filtered by a low-pass filter, in which analysing circuits the receivers and the switchable resistor with a change-pole or change-over switch controlled by the overflow of the clock pulse counter are fed from a d.c. current or voltage source and the phase-sensitive rectifier is synchronously controlled with the change-over switch.

Such an analysing circuit is known from DE-PS 22 62 755. The analysing circuit, there called digital compensation device, is, in result, to be free of effects of thermo-voltages and contact potentials in the passive measured value receiver and independent of the zero point drift of a so-called zero amplifier.

In order to make the improvements, which are striven for with the invention compared with this known circuit, comprehensible in a better way, it is put forward that the known circuit be evaluated critically. For this reason the known circuit is represented again in Figure 1. In this Figure 1, two measured value receivers DMS1, DMS2 can be seen, consisting of bridge circuits, the feed diagonals of which are fed with currents I_S' by way of secondary windings of a current

transformer Tr1. The measuring diagonals of the measured value receivers DMS1 and DMS2 are connected in series. The total voltage at the diagonals is denoted with U_m . Connected in opposition to this total voltage is a compensation voltage U_k which falls at a compensation resistor R. The compensation resistor R can be connected by way of a reverser S2 to the secondary winding of a second current transformer Tr2, through which winding a current I_S flows. A second contact of the reverser S2 connects to a resistor R' which can be connected, by way of the reverser alternately with the resistor R, into the secondary current circuit of the transformer Tr2. The primary windings of the current transformers Tr1 and Tr2 are connected in series by way of a change-over switch S1 to a d.c. current source. The current I_S flows in the primary windings. The difference in the voltages U_m and U_k is supplied via lines L1 and L2 to a switch S3 which is previously connected to a zero amplifier NV. Connected to the output terminals of the zero amplifier is a second change-over switch S4. Its output terminals are connected, by way of a low-pass filter TP, to the input terminals of a voltage frequency transformer SPF. The change-over switch S4 is actuated synchronously with the change-over switch S1 so that it acts as a contact rectifier. The output terminals of the voltage frequency transformer SPF are connected to the forward and backward inputs of a pulse counter Z1. The counting input of a clock pulse counter Z2 is connected to the output of a clock generator which supplies a pulse train with the repetition frequency f_0 . The decade outputs of the counters Z1 and Z2 are connected to comparison inputs of a digital comparison circuit DV. An output of the comparison circuit DV, which conducts a pulse k marking the correspondence of the counter contents z_1 and z_2 , is connected to the

input of a switching control logic Lo. A transmission pulse $\bar{u}$, by way of a connection line of the highest decade of the clock pulse counter Z2, reaches a second input of the switching control logic Lo. A

5 transmission pulse v of a pre-clock counter VZ is supplied to a further input of the switching control logic. An output of the switching control logic simultaneously controls the two change-over switches S1 and S4. Two further outputs of the switching control

10 logic are used to control the switches S2 or S3 respectively.

The polarity of the feed voltage or the feed current respectively is changed with the switch S1, by way of the switching control logic Lo, whenever the

15 clock pulse counter Z2 is counted up by the clock pulses of the clock pulse generator TG to its counter final value $z2_{\max}$ and emits a transmission pulse $\bar{u}$.

The switch S2 is changed over, by way of the switching control logic Lo, to the resistor R' at the

20 moment at which the clock pulse counter Z2 has the same content as the counter Z1 and with that the digital comparison circuit DV with a pulse k signals the coincidence of the counter contents to the switching control logic Lo. The arithmetic mean value $\bar{U}_k$ of the

25 compensation voltage U_k obtained in this way is thus directly proportional to the instantaneous counter content $z1$ of the counter Z1, relative to the maximum counter content $z2_{\max}$ of the clock pulse counter Z2.

The interrupter switch S3, which is switched

30 through by the switching control logic Lo at the same moment as the switch S2, shifted by the time Δt relative to the change-over times of the feed current, remains switched through throughout an interrogation clock pulse

35 $T_A = z2_{\max} \cdot \frac{1}{f_0}$

until the next transmission pulse $\bar{u}$ of the clock pulse

counter Z2. The zero amplifier NV, to the input of which the switch S3 is previously connected, accordingly obtains the difference voltage ΔU .

It has been proved that the desired success can only be achieved in a very insufficient manner with this known circuit, for the following reasons.

The known circuit reproduced in Figure 1, as an automatically adjusting compensation device, in terms of its construction is a closed control loop in which the zero amplifier NV, which is called control amplifier in control engineering, serves to amplify the deviation, as far as possible selectively. This deviation is to be called $\bar{\Delta} \bar{U}$ here. It represents the difference in the arithmetic mean values of the receiver signal voltage sum $\bar{U}_m$ and the compensation voltage $\bar{U}_k$, formed in each case over a switching duration T_A ,

$$\bar{\Delta} \bar{U} = \bar{U}_m - \bar{U}_k.$$

As a result of the polarity of the feed currents IS which is changed with each change-over of the change-over switch S1, $\bar{\Delta} \bar{U}$ and all other components of the difference voltage ΔU acting on the input of the zero amplifier NV have opposite signs in two successive switching times T_{An} and $T_{An} + 1$ with equal magnitude. $\bar{\Delta} \bar{U}$ and ΔU are thus alternating voltages with a basic frequency

$$f_W = \frac{1}{T_A} = \frac{1}{T_A}.$$

without any d.c. component.

Basically the following properties are required of zero amplifiers in control loops:

- a) a large amplification factor in the transmission range of the deviation;
- b) a smallest possible zero error in the amplification of the deviation;
- c) in the interests of high selectivity and disturbance variable suppression, a smallest

possible amplification factor outside the transmission range of the deviation.

On the other hand, the following are not required:

- d) a linear modulation characteristic;
- 5 e) a phase-linear frequency response and
- f) special stability of the amplification factor.

With the property c) a zero amplifier, as used in the case of the known circuit, in the transmission range $f < f_w$ will have an amplitude response which
10 falls towards lower frequencies as steeply as possible and will not transmit, more particularly, the frequency 0, that is, d.c. voltage signals (high-pass filter characteristic).

The result of this, however, in the case of the
15 adjustment principle, according to which the operation is effected here, namely the continuously modulated change-over, is that with the resultant rectangular signals ΔU pulse tilts occur which, for their part, lead to a non-linearity of the indication
20 characteristic, as is explained further in greater detail below.

Absence of the property e), that is, a non phase-linear frequency response in the transmission range $f \geq f_w$ of the zero amplifier, results in running time
25 distortions in the amplification of the difference signal ΔU . These, in the case of the phase-selective rectification of the amplified difference signal ΔU by the clocked reverser S4, can lead to the generation of erroneous d.c. voltage components which are not
30 proportional to the deviation ΔU and represent zero errors.

If the property d), a linear modulation characteristic, is missing, even if this is rotationally symmetrical (without even-numbered curve
35 elements), positive and negative amplitude sections are evaluated in the voltage shape of ΔU with differing

weight. This results in errors in the formation of the arithmetic mean value $\bar{\Delta} \bar{U}$ of the difference signal, which errors likewise make themselves felt as zero errors. These further fluctuate in their size if, as in the case of a usual zero amplifier, the property f), more particularly stability of the amplification factor, is also missing. As the errors in the mean value formation are also further dependent upon the switching-in ratio $a = t_e/T_A$, zero errors dependent upon a affect the indication characteristic, in addition, as linearity errors.

The deficiencies caused by the properties of the zero amplifier NV are intensified further by the potential isolation, provided for the feed current IS'' for the compensation resistor R, which is to be switched on and off in a continuously modulated manner, in relation to the feed currents IS' for the measured value receivers through current transformers Tr.

On account of the unavoidable leakage inductance and main inductance of these current transformers, which main inductance can only be dimensioned to be finitely great, and also the finitely small internal resistance of the d.c. voltage source which feeds the switch S1, the secondary feed alternating currents IS' and IS'' cannot have any ideal rectangular form. On the contrary, they show pulse tilts in the form of e-functions, as represented in Figure 2 of the drawing. For the feed current of the compensation resistance R:

$$IS''(t) = \hat{IS}'' e^{-\frac{t}{\tau}}$$

holds good, where τ is a time constant which is determined by the values of the leakage and main inductance of the current transformer Tr2, the internal

resistance of the d.c. current source and the compensation resistance. In Figure 2, T_A signifies the switching duration of a polarity of the change-over switch S1, from which there follows the period $T_W = 2 \cdot T_A$ for the feed alternating currents IS' and IS'' .

5 This means that the compensator circuit has a non-linearity of its indication characteristic which does not satisfy higher accuracy requirements, because in accordance with Figure 3 the arithmetic mean value $\bar{U}_k$ of the compensation voltage U_k over, in each case, a switch-in duration T_A , is not, as required by the principle of continuous pulse modulation, proportional to the adjustment factor $a = t_e/T_A$ but to the quotient from the switch-in time t_e of the compensation resistance R and the switching duration T_A .

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15 On the contrary,

$$\bar{U}_k(a) = \frac{1}{T_A} \int_{t_0}^{t_0 + t_e} \hat{U}_k e^{-\frac{t}{\tau}} dt = -\hat{U}_k \cdot \frac{\tau}{T_A} \cdot e^{-\frac{t}{\tau}} \Big|_0^{t_e}$$

$$\text{with } \hat{U}_k = IS'' \cdot R$$

From the certain integral

$$\bar{U}_k(a) = \hat{U}_k \cdot \frac{\tau}{T_A} \left[1 - e^{-a \cdot \frac{T_A}{\tau}} \right]$$

and according to a series expansion of

$$\frac{\tau}{T_A} \left[1 - e^{-a \frac{T_A}{\tau}} \right]$$

with $a = t_e/T_A$ there results therefrom

$$\bar{U}_k(a) = \hat{U}_k \cdot a \cdot \left[1 - \frac{1}{2} \frac{t_e}{\tau} + \frac{1}{6} \left(\frac{t_e}{\tau} \right)^2 - \frac{1}{24} \left(\frac{t_e}{\tau} \right)^3 + \dots \right]$$

As Figure 3 shows, according to the above series expression the compensation voltage $\bar{U}_k$ does not grow proportionally in relation to $a = t_e/T_A$, but
 5 sublinearly with a linearity error F_{Lin} , which is greater, the smaller the time constant τ of the pulse tilt in comparison with the switching duration T_A .

On the other hand, the arithmetic mean value $\bar{U}_m$
 10 is constantly formed from the sum U_m of the output voltages $U_{m\gamma}$ of all n measured value receivers DMS_γ by the known compensator circuit over the full switching duration T_A , that is,

$$\bar{U}_m = \frac{1}{T_A} \int_0^{T_A} \sum_{\gamma=1}^n \hat{U}_{m\gamma} e^{-\frac{t}{\tau_\gamma}} dt = -\frac{1}{T_A} \sum \tau_\gamma \cdot \hat{U}_{m\gamma} \cdot e^{-\frac{t}{\tau_\gamma}} \Big|_0^{T_A}$$

However, with that

$$\bar{U}_m = \sum_1^n \frac{\tau_\gamma}{T_A} \cdot \hat{U}_{m\gamma} \cdot \left[1 - e^{-\frac{T_A}{\tau_\gamma}} \right] = \sum_1^n k_\gamma \cdot \hat{U}_{m\gamma}$$

with

$$k_\gamma = \tau_\gamma / T_A \left[1 - e^{-\frac{T_A}{\tau_\gamma}} \right]$$

and

$$\hat{U}_{m\gamma} = c_\gamma \cdot G_\gamma \cdot \hat{IS}_\gamma'$$

where c_γ signifies a receiver sensitivity constant. Thus the mean value $\bar{U}_m$ on account of the purely ohmic networks in the receivers DMS_γ despite the pulse tilts of the individual signals $U_{m\gamma}$ represented by τ_γ is strictly linearly proportional to the sum of the measured values G_γ which act at each moment on the n receivers DMS_γ .

10 An indication value A of the known compensator circuit, which is proportional to the switch-in ratio $a = t_e / T_A$, is obtained by way of the adjustment condition

$$\bar{U}_k(a) = \bar{U}_m (\sum G_\gamma).$$

On account of the sub-linearity of $\bar{U}_k$, the known compensator circuit must therefore have, as a whole, a super-linear indication characteristic.

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The underlying object of the invention was to improve the initially described analysing circuit for passive measured value receivers so that it obtains a linear indication characteristic. In this connection, its advantages with regard to insensitivity to thermo- and contact voltages of the receivers, the compensation quantity generator and the input installation as well as to zero drifts of the amplification are to be preserved.

10 This object is achieved according to the invention by means of the measures described in the characterising features of claim 1.

The first measure relates to the shift of the zero amplifier NV, provided in the case of the known circuit according to Figure 1, after the low-pass filter TP with use of a directly coupled pre-amplifier at the previous position of the zero amplifier. This pre-amplifier advantageously consists of an operational amplifier which is d.c. coupled to an output of the network of receiver and compensation resistors and also, if applicable, pertinent coupling elements, which output emits the balancing difference voltage or a balancing difference current. It has a phase-linear frequency response, which begins at the frequency 0 (permeable to d.c. components) and which with a wide band amplifies beyond the polarity reversal frequency $f_W = \frac{1}{T_A}$. Its amplitude response does not then need to be particularly level. The amplification can fluctuate in periods, which are long in relation to the clock time T_A , within further limits without affecting the indication accuracy. Its modulation characteristic must, on the other hand, be strictly linear for each frequency in the transmission range. The pre-amplifier preferably only has a comparatively low amplification in order to guarantee that it is not operated beyond its modulation limits by capacitive or

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inductive disturbance spreading into the input wiring or by means of its own noise components as well as zero drifts in the adjustment state of the analysing device.

5 A further measure relates to the direct coupling of the current, which flows through the switchable resistor, at the change-over switch of the d.c. current source. It ensures that this current has strict rectangular form and no more pulse tilts causing
10 linearity errors.

On account of the transmission properties of the pre-amplifier which are obtained by these measures, the balancing difference signal is amplified so that
15 neither on account of running time distortions nor on account of non-linear modulations in the case of the following phase-sensitive rectification can d.c. components, invalidating the correct indication value, develop as zero errors.

Advantageously, the phase-sensitive rectifier has
20 a strictly linear characteristic, which runs exactly through the zero point.

The considerable advantages of the use of such a pre-amplification with following rectification lie in the fact that all disturbing d.c. components from the
25 input circuit, that is, the zero drifts of the pre-amplifier, thermo-voltages and contact potentials of the receivers of the switch-controlled compensation resistor network and also the feed lines to the pre-amplifier in the phase-sensitive rectifier, are
30 transformed into square-wave voltages of the basic frequency f_w of the inverter. They can be effectively and easily filtered out on account of their great distance from the frequency 0 in subsequently connected low pass-filters.

35 The noise components, during the demodulation process, on the other hand, all experience a frequency

shift by $\pm f_w$ of the inverter frequency f_w . As a result, the very disturbing low-frequency noise components of simple semi-conductor amplifier input stages, the so-called popcorn or $\frac{1}{f}$ noises, are shifted
5 into the direct vicinity of the inverter frequency f_w and can likewise be effectively suppressed by the following low-pass filters. Therefore only the so-called white noise represents the natural resolution limit of the analysing circuit according to the
10 invention.

The synchronous control of the phase-sensitive rectifier with the change-over switch ensures that a suppression of the disturbing d.c. components mentioned, satisfying higher accuracy demands, is obtained in the
15 amplified balancing difference signal, because with that even the selective rectifier is controlled in strict time symmetry.

The generator for the high-frequency pulse train is advantageously quartz-stabilised.

20 The symmetry of two branches of the phase-sensitive rectifier in relation to earth is advantageously made adjustable by means of a potentiometer.

Advantageously, the measured value receiver bridge circuits, in addition to the switchable resistor, are
25 also d.c. coupled with the change-over switch.

A similarly favourable effect is achieved if the measured value receiver bridge circuit and/or the switchable resistor are coupled, by way of operational
30 amplifier or opto-coupler, with the change-over switch.

In the case of a preferred exemplary embodiment of the invention the direct coupling of a measured value receiver bridge circuit and a switchable resistor is realized in that the bridge circuit with its feed
35 diagonal is d.c. coupled to the change-over switch and is divided at one of its diagonal points. The

switchable resistor is inserted into the separating point, in which case the switching contact arm of the reverser replaces the diagonal point at the separating point. The input terminals of the pre-amplifier are
5 arranged at the measuring diagonal of the measured value receiver bridge circuit.

In another exemplary embodiment the feed diagonal of the measured value receiver bridge circuit is d.c. coupled to the change-over switch. The switchable
10 resistor is connected between earth and the output of a first operational amplifier, which is arranged with its input terminals at the change-over switch. The measuring diagonal of the measured value receiver bridge circuit is thereby arranged at the input
15 terminals of a second operational amplifier, the output of which is connected to earth via a resistor and also connects to an input terminal of the pre-amplifier. The pre-amplifier is connected with its other input terminal to the switching contact arm of the reverser
20 which in the one position connects to the output of the first operational amplifier and in the other position connects to earth. In a further exemplary embodiment of the invention, the feed diagonal of the measured value receiver bridge circuit is d.c. coupled to the
25 change-over switch. The switchable resistor is connected via the reverser between the output of a first operational amplifier, which connects to the change-over switch with its input terminals, and earth. The measuring diagonal of the measured value receiver
30 bridge circuit is connected to the input terminals of a second operational amplifier, the output of which is connected via a resistor to that input terminal of the pre-amplifier which is connected to one of the switching contacts of the reverser. The other input
35 terminal of the pre-amplifier connects to earth.

The feature of the direct coupling is realized in

the case of another exemplary embodiment of the invention so that a second resistor bridge circuit is connected in parallel to the measured value receiver bridge circuit on the supply and measuring diagonal side, the second resistor bridge circuit being divided at a measuring diagonal point and the switchable resistor being inserted into the separating point. The input terminals of the pre-amplifier are then connected to the parallel-connected measuring diagonals of the two resistor bridge circuits. A semi-bridge circuit, the branches of which include the switchable resistor, can also replace the second resistor bridge circuit.

Another exemplary embodiment of the invention has a second resistor bridge, which is connected in parallel to the measured value receiver bridge circuit on the feed and measuring diagonal side and which is divided at a feed diagonal point, the separating point being occupied by two contacts of the reverser. The switching contact arm of the reverser thereby connects to one of the feed diagonal points of the measured value receiver bridge circuit. The input terminals of the pre-amplifier are connected to the parallel-connected measuring diagonals of the two resistor bridge circuits.

A final exemplary embodiment of the invention has a switching resistor which, with the aid of the reverser, can be alternately connected in parallel to two resistors, arranged symmetrically relative to a diagonal point, of the measured value receiver bridge circuit, the input terminals of the pre-amplifier being arranged on the measuring diagonal.

The duration of an adjustment period T_A , in relation to the duration T_W of the inverter and rectifier clock time, stands in a ratio of whole numbers (e.g. 1:2; 2:3; 3:5 etc.).

In addition to Figures 1 to 3 which serve to

explain the deficiencies of the prior art and which have already been discussed, various exemplary embodiments of the invention are represented in a further ten Figures.

5 Figure 4 contains an exemplary embodiment of the invention in which a detuning compensation is applied.

10 In Figure 5, in Graphs a, b, c, the voltage shapes, which are obtained at characteristic switching points of the circuit according to Figure 4, are represented.

 Figure 6 represents a modified detail of the circuit according to Figure 4.

15 In Figures 7 to 13, various embodiments of the direct coupling of the receiver and compensation network to the inverter or polarity reversal switch are represented respectively.

20 The circuits according to Figures 7 to 9 follow the principle of voltage compensation; in the case of circuits according to Figures 10 to 13, on the other hand, the principle of current compensation is used.

25 In Figure 4, a preferably balanced-to-earth voltage source SQ is connected via contact break-distances $T_{p1} \dots T_{p4}$, which form a change-over switch or inverter SW, with a measured value receiver G which is represented as receiver measuring bridge with four variable resistors $R_1 \dots R_4$. An adjustment resistor R_K is to be connected in parallel by way of contact break-distances T_{01} and T_{02} alternately to the measuring bridge resistors R_1 or R_2 respectively. The contact
30 break-distances $T_{p1} \dots T_{p4}$ of the change-over switch or inverter are controlled by output signals of a flip-flop FF_1 . A dynamic input of the flip-flop FF_1 is arranged at an output for an overflow signal U_z of a counter Z, upon which clock pulses of a clock generator
35 TG act. Bit outputs of the clock pulse counter Z are connected with corresponding inputs of a digital

comparator V, the comparison bit inputs of which connect to bit outputs of an indication counter A. An output of the comparator V, which conducts signals in the case of equality of the counter contents of the counters Z and A, is connected with one of the control inputs of a second flip-flop FF₂. The other control input of the flip-flop FF₂ connects to the output of the counter Z which emits the overflow signal U_z . The two outputs of the flip-flop FF₂ are each connected with a control input of one of the contact break-distances T₀₁ or T₀₂ respectively.

The measuring diagonal of the receiver G connects to inputs of a pre-amplifier VV. The output of this pre-amplifier VV is connected to the input of a phase-sensitive rectifier D which substantially consists of the contact break-distances T_{G1} and T_{G2}. Control inputs of the contact break-distances T_{G1} and T_{G2} are connected to two outputs of the flip-flop FF₁ which mutually conduct inverted signals and which simultaneously control the contact break-distances of the change-over switch or inverter SW. The two branches of the phase-sensitive rectifier D can be centered by way of a potentiometer PL which connects both branches. The output of the phase-sensitive rectifier D connects, by way of a first low-pass filter element T₁, to the inputs of a post-amplifier NV which acts as d.c. voltage zero amplifier and the output of which is connected, by way of a second low-pass filter element T₂, with the input of a voltage frequency transformer UF. According to the polarity of the input voltage of the voltage frequency transformer, one of two outputs of the voltage frequency transformer becomes signal-conductive. The two outputs are connected with corresponding inputs for forward and backward counting of the indication counter A. Bit outputs of the indication counter A connect to

corresponding inputs of a numerical indicator ZA.

The mode of operation of the circuit is described in the following.

With the aid of the contact break-distances
5 $T_{p1} \dots T_{p4}$ of the change-over switch or inverter SW, there is derived from the balanced-to-earth supply voltage $\pm U_B$ of the voltage source SQ for the electronic components of the analysing circuit, which supply voltage is only stabilized against short-term
10 voltage fluctuations, a square-wave feed voltage U_S with the exact clock ratio 1 : 1 for the feed of the measured value receiver G. This has an amplitude of $2 U_B$ and a period of $T_W = 2T_A$ disregarding the voltage drops by way of the inverter contact break-distances
15 $T_{p1} \dots T_{p4}$. T_A is then the time which is required in order for the clock pulse counter Z to count, by means of the pulses which are supplied by the short-time stable clock generator TG with the repetition frequency f_t , from 0 up to its maximum value Z_{max} . The overflow
20 pulse U_Z , which is supplied by the counter Z after the latter has completed counting, at one time sets the clock pulse counter Z itself back to "0" and simultaneously acts on the dynamic input of the flip-flop FF₁ which as a result respectively varies its
25 switching state at the end of the time T_A . As a result, in each case alternately for an n-th clock time T_{An} the contact break-distances T_{p1} and T_{p3} and for the subsequent clock time $T_{An} + 1$ the contact break-distances T_{p2} and T_{p4} of the inverter SW or change-over
30 switch are controlled for transmission so that a square-wave voltage U_S is available at the feed diagonal of the measured value receiver G with the required exact clock ratio 1 : 1. The contact break-distances T_{G1} and T_{G2} of the phase-sensitive rectifier
35 D are also controlled for transmission in a phase-rigid manner and strictly in synchronism with the contact

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break-distances $T_{p1} \dots T_{p4}$ of the inverter, by the
respective position of the flip-flop FF_1 , alternately
for the duration of the time T_A . The phase-sensitive
rectifier D thereby demodulates the output voltage of
5 the pre-amplifier VV.

The pre-amplifier VV is coupled in terms of d.c.
current with the measuring diagonal of the measured
value receiver G and operates as a phase-linear wide-
band amplifier with highly-linear modulation
10 characteristic line from a frequency 0. It therefore
amplifies the receiver measured voltage u_m , which, in
addition to the undesirable disturbing d.c. portions,
consisting of thermo-voltages and contact potentials,
has exclusively alternating components, the basic
15 frequency of which is

$$f_w = \frac{1}{T} = \frac{1}{T_A}$$

and moreover consists of the harmonic waves of the
latter. The pre-amplifier VV further amplifies
undesirable d.c. components, which result from current
20 and voltage zero drifts of the pre-amplifier VV itself.
The effect of these zero drifts is combined together
with the thermo- and contact voltages of the receiver
and compensation network in a substitute voltage u_0 .
To this purpose the pre-amplifier VV also amplifies all
25 noise voltage portions which are produced mainly in the
input stage of the pre-amplifier VV, but also as white
resistance noise in the receiver and compensation
network.

All disturbing d.c. components are transformed, in
30 the strictly symmetrically connected, highly linear
phase-sensitive rectifier D, into square-wave voltages
of the basic frequency f_w which, on account of their
great distance from the frequency 0, can easily be
effectively filtered in the subsequently connected low-
35 pass filters T_1 and T_2 despite their comparatively high
limiting frequency.

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Another result of the mode of operation of the new circuit is likewise advantageous and this lies in the fact that the noise components of the output signal of the pre-amplifier VV in the demodulation process all experience a frequency shift by $\pm f_w$. As a result, the otherwise very disturbing low-frequency noise components, more particularly of simple semi-conductor amplifier input stages, - the so-called popcorn or $\frac{1}{f}$ noise - are shifted into the direct vicinity of the inverter frequency f_w and can therefore be suppressed likewise in an effective manner by the subsequent low-pass filters T_1 and T_2 . The noise portions, which are smaller by orders of magnitude, of the so-called white noise are not suppressed. Only this type of noise therefore represents the natural resolution limit of the new analysing circuit which can be approximated practically at random even with very inexpensive operational amplifiers. For example, this limit is at 10 to 30 nV, according to internal resistance of the measured value receiver and choice of low-pass filter limiting frequency.

Measured voltage components in u_m originating from a detuning dependent upon measured values

$$\frac{\Delta R}{R} = b \frac{\Delta R}{R}$$

of the measured value receiver, have a square-wave voltage shape with an amplitude of

$$b u_m = \frac{\Delta R}{R} \cdot U_s.$$

which, on account of the set-up of the receiver and compensation network of purely ohmic resistors, is exactly in phase with U_s . Here $\frac{\Delta R_{max}}{R}$ is the detuning change of the receiver measuring bridge which brings

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about the measured value when its measuring range final value is reached at the latter. The factor b accordingly specifies the degree of partial modulation of this measuring range. It can thus assume values
5 between 0 and 1. The square-wave voltage $b \cdot \hat{u}_m$ is transformed, after pre-amplification by means of VV , by the phase-sensitive rectifier D , correctly in terms of sign, into a proportional d.c. voltage which can pass through the low pass filter T_1 and, after post-
10 amplification by the post-amplifier NV , in an unhindered manner also through the low-pass filter T_2 and which with sign-correct evaluation in the subsequent voltage frequency transformer UF is transformed into a pulse train

$$z_{I_{auf}} \quad \text{or} \quad z_{I_{ab}} \quad (\text{auf} = \text{up}; \quad \text{ab} = \text{down})$$

15 with a repetition frequency which is proportional to the respective residual detuning of the measured value receiver.

The counter pulses produced thereby

$$z_{I_{auf}} \quad \text{or} \quad z_{I_{ab}}$$

are used to change the instantaneous counter content of
20 the indication counter A with its counting decades, of which there are four in the exemplary embodiment A_T , A_H , A_Z and A_E , for the purpose of approximating the adjustment state of the measuring circuit, prescribed by b , in an upward or downward direction.

25 It has already been mentioned that it is of crucial significance for the linearity and long-time stability of the indication characteristic of the analysing circuit that the pre-amplifier VV have a modulation characteristic which must be strictly linear

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at least in the frequency range

$$f_w - f_{dyn_{max}} \text{ to } f_w + f_{dyn_{max}}$$

yet not stable in the long term and that the phase-sensitive rectifier D operate in a strictly symmetrical manner and likewise with a highly linear
5 characteristic. It is therefore advantageous to provide, in the phase-sensitive rectifier D with the aid of a trimming potentiometer PL, a possibility for finely adjusting this symmetry. Conversely it is also possible to introduce non-symmetry consciously with the
10 aid of this adjusting possibility if the receiver characteristic is to have even-numbered curve elements. With cooperation of measuring receiver and analysing circuit it is possible in this way to effect a very simple, yet highly effective linearity adjustment.
15 Such a linearity adjustment is particularly recommendable if the analysing circuit, over and above the four counting decades represented in Figure 4, has a greater digital measured value resolution as a result of a greater number of counting decades.
20 In the case of the possibilities of digital circuit engineering which exist today, a resolution between 10^5 and 10^6 can be achieved so that use of five to six counting decades becomes sensible.
In the case of increased resolution it is also
25 sensible to apply a variant of the embodiment which is not represented in Figure 4 and which permits the elimination of the influence of running time fluctuations of the pre-amplifier VV as well as the finite change-over duration and the charge-reversal
30 effects of the change-over stretches for the adjustment resistor R_K .

To this purpose, by means of a correspondingly

designed control system after the occurrence of an overflow signal U_z by blocking the last conducting inverter contact break-distances T_{p1} , T_{p3} or T_{p2} , T_{p4} respectively, the measuring receiver feed voltage U_g is set to "0" for a short period of time t_{u1} . In this voltage-free state, at the end of t_{u1} the change-over of the resistor R_k takes place by means of the switching stretch T_{01} or T_{02} as does the reversal of the phase-sensitive rectifier D.

Only at the end of a further short time span t_{u2} is the feed voltage U_g again switched in by way of the complementary inverter contact break-distances with reversed polarity.

Reference is further made to the fact that the counting, comparison and control task problems, which are solved by means of individual switching elements in the exemplary embodiment represented in Figure 4, can, if applicable, be solved by a microprocessor which is already present and which is required for other tasks. As a result, the task-specific portion of the analysing circuit can be considerably reduced. The result of this is the possibility of effecting a sensible integration in a custom-designed circuit which can be used in a very flexible manner.

In Graph a of Figure 5 the shape of the feed voltage U_g of the measuring receiver is represented along the time axis t . The amplitude of the square-wave alternating voltage, which is generated by polarity-reversal, amounts to $2 U_B$. The period of alternating voltage is $2 T_A$. The semi-period T_A is the product of the maximum content Z_{max} of the counter Z , divided by the repetition frequency f_t of the counting pulses which run into the counter Z .

In Graph b of Figure 5, for the purpose of facilitating the understanding, the shape of the output voltage u_m of the network of receiver and compensation

resistors is plotted with the assumption that a bridge
detuning of the measuring receiver is exactly
compensated by means of the measured value by $b \cdot \frac{\Delta R_{\text{max}}}{R}$
by clocked change-over of the resistor R_K for a
5 switching-in time t_e of respectively $b \cdot T_A$ precisely
and the adjustment process required therefor is
concluded. For this adjustment state for each
adjustment clock pulse irrespective of the polarity of
the measuring receiver feed voltage U_S , it holds true
10 that the integral determining the arithmetic mean value

$$\overline{u_{m0}}$$

of the measuring circuit output voltage u_m from the
moment of switching in t_{Anfang} (Translator's note:
Anfang = start) over a full clock time T_A

$$\overline{u_{m0}} = \frac{1}{T_A} \int_{t_{\text{Anfang}}}^{t_{\text{Anfang}} + T_A} u_m(t) dt = 0$$

no longer has a d.c. portion. If after a pre-
15 amplification, which in the first instance is assumed
to be ideal, of

$$u_{m0}$$

the amplified signal undergoes polarity reversal by
means of the pre-amplifier by the phase-sensitive
rectifier likewise acting as controlled polarity
20 reverser, in each case, exactly at the instants
 t_{Anfang} , it is therefore also no longer possible for a
d.c. portion to originate in the thus formed output
voltage u_a of the phase-sensitive rectifier D from

these alternating components of

$$u_{m0}$$

which portion could pass through the low-pass filters T_1 and T_2 and as a result would erroneously affect the adjustment value of the analysing circuit. This would, however, very probably happen if the phase-sensitive rectifier underwent polarity reversal at times which do not exactly coincide with t_{Anfang} . There originates from this the demand for an extremely time-exact, phase-rigid control of the demodulator D, which control is associated with the polarity reverser of the feed voltage.

In Graph c of Figure 5, finally, the shape of the demodulated output voltage u_a of the pre-amplifier VV, which is really to be found, is plotted in the case of action on the input side by a measuring circuit output voltage $u_m(t)$ in accordance with Graph b and a simultaneous superposition of this voltage $u_m(t)$ by a d.c. component u_0 as a result of zero drifts of the pre-amplifier VV as well as thermo- and contact voltages in the measuring circuit. Both signal components appear at the output of the pre-amplifier, increased by the amplification factor V_1 of the latter.

It can be seen that the demodulated signal in the adjustment state despite all disturbing influences has no d.c. components at all which affect the adjustment value any longer, as the demodulator chops the amplified disturbance d.c. voltages into square-wave alternating voltages of the basic frequency f_w . A precondition for this is that the demodulator D has a characteristic which goes exactly through 0 and which is strictly linear.

There is represented in Figure 6 a further exemplary embodiment for a directly coupled measured value receiver G and a compensation resistor R_{K6} , in

which a detuning compensation is applied.

Connected to a feed voltage source SQ with the voltage $2 U_B$ is a polarity reverser SW which supplies the feed diagonal of a measured value receiver G with a square-wave voltage U_S . The measured value receiver G consists of a bridge circuit of four resistors $R_1...R_4$ which are variable with a measured variable. The connection points of this bridge circuit are designated with 1...4. Deviating from the circuit arrangement according to Figure 4, a compensation resistor R_{K6} , with which a detuning compensation of the output signal of the measured value receiver G can take place, is fixedly connected not to a corner point of the output diagonals, but to a feed diagonal point. With the aid of a reverser S_{U6} the compensation resistor R_{K6} can be alternately connected to both diagonal points 2, 3 of the output diagonals and with that is to be connected in parallel, in each case, to one of the bridge resistors R_1 or R_3 respectively. As a result of this change-over, the adjustment factor a is controlled so that the detuning $\frac{\Delta R}{R}$ of the measured value receiver bridge G conditional on measured values, in the temporal mean value is made precisely 0 by the counter-detuning of the bridge. The instantaneous variable of the detuning is determined by means of the no-load-running measuring voltage

$$u_{m_0},$$

which occurs at the output diagonal of the measured value receiver G and is amplified in the pre-amplifier VV. There is connected to the output of the pre-amplifier VV, the operating voltage of which originates from the voltage source SQ, a further change-over contact S_G , which together with two resistors R_G serving the purpose of balancing, forms the phase-sensitive rectifier or demodulator D. The output

voltage U_G of the demodulator D is, as in the exemplary embodiment of Figure 4, processed further. The reversers SW, S_{U6} and S_G are controlled in the same way as the switching elements $T_{p1} \dots T_{p4}$, T_{01} and T_{02} or T_{G1} and T_{G2} respectively which are represented in Figure 4 as semi-conductor switches, for example, MOS-FET transistors.

A further exemplary embodiment of the measured value receiver, pre-amplifier and phase-sensitive rectifier complex with the pertinent reversers and a compensation resistor is represented in Figure 7. Components, which are similar in terms of their signification, are denoted with the same reference symbols as in the circuit according to Figure 6. The measured value receiver G again consists of four resistors $R_1 \dots R_4$ which are connected together to form a Wheatstone bridge circuit and the feed diagonal points 1 and 4 of which are connected to a feed voltage U_S , connected by way of the periodically switchable reverser SW at the feed source SQ with the d.c. voltage $2 U_B$. At the output diagonal point 3 of the measured value receiver bridge G the bridge is divided and a compensation resistor R_{K7} is inserted into the separating points 3a, 3b. The measured value receiver G is here represented as a full bridge circuit, yet it is self-evident that a quarter- or semi-bridge circuit can also be used. The bridge points 3a and 3b can alternately be connected, with the aid of a reverser S_{U7} , to the one input of the preamplifier VV, the other input of which is connected with the output diagonal point 2 of the measured value receiver G. The partial voltage which drops at the resistor R_{K7}

$$U_K = U_S \cdot \frac{R_{K7}}{R_1 + R_2}$$

is connected in opposition by change-over of S_{U7} in the time ratio $a = t_e/T_A$ of the measuring receiver voltage

u_m according to the principle of voltage compensation.

The other circuit, which is not represented, for analysing the output voltage of the phase-sensitive rectifier D and also for the control of the reversers corresponds to the details which can be inferred from Figure 4.

A circuit, which largely corresponds with the circuit according to Figure 7, is represented in Figure 8. It differs from the circuit according to Figure 7 in that the feed diagonal point 1 of the measured value receiver bridge G is divided and a compensation resistor R_{K8} is inserted at the separating point 1a, 1b. A reverser S_{U8} alternately connects one of the points 1a or 1b respectively to the output voltage U_S of the polarity-reversal switch SW. There is voltage compensation even in the case of the circuit according to Figure 8. The input voltage u_D for the pre-amplifier amounts to $u_D = U_1 - U_2 = u_m - a \cdot \bar{u}_K$.

A further measured value receiver compensation and rectifier complex is shown in Figure 9, which complex operates according to the principle of voltage compensation. In this connection, the voltage u_m at the output diagonal of the measured value receiver G is amplified by way of an operational amplifier V_{T2} . A compensation resistor R_{K9} connects by way of another operational amplifier V_{T1} to the output voltage U_S of the polarity-reversal switch SW. One of the input terminals of the pre-amplifier VV connects to the output of the operational amplifier V_{T2} , the voltage drop $\bar{u}_K$ at the compensation resistor R_{K9} and wet (sic) potential acting alternately on the other input terminal by way of a reverser S_{U9} . The input voltage of the pre-amplifier VV is represented in relation to $u_D = v \cdot u_m - a \cdot \bar{u}_K$ where v signifies the amplification of the operational amplifier V_{T2} .

An example of a circuit for a measured value receiver and compensation network is represented in Figure 10, this operating according to the principle of current compensation. To this purpose, a measured value receiver bridge circuit G and a compensation bridge circuit K, which consists of four resistors $R_1' \dots R_4'$ and a switchable resistor R_{K10} , are connected in parallel with their feed diagonals and output diagonals. On the feed side, both connect to the polarity-reversal switch SW and with that to its output voltage U_S . One of the output diagonal points of the compensation bridge K is divided and between the separating points there is arranged the switchable resistor R_{K10} , the two connection points of which are alternately connected by a reverser S_{U10} to one input of the pre-amplifier VV. The other input of the pre-amplifier VV connects to two output diagonal points, which are connected with each other, of the two bridge circuits G and K. In the case of this circuit arrangement a short-circuit current i_m from the measuring diagonals of the measured value receiver bridge G is offset against the short circuit current i_k of the compensation bridge circuit K. In the interests of low reaction on the receiver bridge circuit and low loading of the current source S_Q , all the bridge resistors of the compensation bridge circuit K are designed with high resistance.

A variant of the circuit according to Figure 10 is represented in Figure 11. The bridge circuit K has been reduced, in this connection, to a semi-bridge consisting of the resistors R_3' and R_4' with the switchable resistor R_{K11} inserted between them. This variant is achieved simply if the resistors R_1' and R_2' of the circuit according to Figure 10 are made infinitely great.

A further exemplary embodiment, in which a current

compensation is used with a compensation bridge circuit, is diagrammatically represented in Figure 12. In this connection only the compensation bridge K consisting of the resistors $R_1' \dots R_4'$ and their
5 connection to the bridge branch of the measured value receiver bridge G consisting of the resistors R_3 and R_4 is shown. A change-over resistor S_{U12} thereby permits the compensation bridge circuit K to be connected to the feed voltage in time with the adjustment factor $a =$
10 t_e/T_A .

A further example for current compensation of the measured value receiver output signal is represented in Figure 13. In this connection, the output diagonal points 2 and 3 of the measured value receiver bridge
15 circuit G connect to the two inputs of an operational amplifier V_{T4} , the output of which connects, by way of a resistor, to the one input of the pre-amplifier VV. The periodically changed-over feed voltage U_S connects to the inputs of a further operational amplifier V_{T3} ,
20 the output of which can be connected, by way of a resistor and a reverser S_{U13} , alternately with earth and the already mentioned input of the pre-amplifier VV. The other input of the pre-amplifier VV connects to earth.

25 The exemplary embodiments represented all have the feature of the coupling, permeable in terms of d.c. voltage, of measured value receiver and compensation network to the change-over switch SW. The possibilities represented of the development of the
30 compensation lay no claim to completeness. It is possible to derive from the basic solutions described here hybrid circuit arrangements in which the measures, which form the basis of the invention, are likewise applied.



Claims

1. Analysing circuits for passive measured value receivers (DMS1, DMS2) having ohmic sensor impedances in bridge connections with adjustment of the output signals of the receivers provided by continuously modulated change-over of a resistor (R_K), which is controlled into one change-over position by the overflow signal of a clock pulse counter (Z2) and into the other change-over position by the output signal of a digital comparator (DV) that compares the contents of the clock pulse counter (Z2) and a forward/backward counter (Z1) connected to the output of a sign-sensitive voltage-frequency transformer (SPF), whose input voltage consists of an amplified balancing difference signal that is rectified by a phase-sensitive rectifier (D) and filtered by a low-pass filter (TP), in which analysing circuits the receivers and the switchable resistor (R_K) with its change-over switch (SW) controlled by the overflow of the clock pulse counter (Z2) are fed from a d.c. current or voltage source (U_B) and the phase-sensitive rectifier (D) is synchronously controlled with the change-over switch, characterised by the combination of the following features:

a) in order to amplify the balancing difference signal the phase-sensitive rectifier (D) is preceded by a preamplifier (VV) that also transmits d.c. components and operates over the entire transmission region with a phase-linear frequency-response curve together with a highly linear modulation characteristic, followed by a zero amplifier (NV); and

b) at least the switchable resistor (R_K) is connected to the change-over switch (SW) by d.c. coupled devices.

2. Analysing circuits as claimed in Claim 1, characterised in that the phase-sensitive rectifier (D)



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has a strictly linear characteristic which runs exactly through the zero point.

3. Analysing circuits as claimed in Claim 1, characterised in that the measured value receiver
5 bridge circuit (G) and/or the switchable resistor (R_K) are d.c. coupled to the change-over switch (SW).

4. Analysing circuits as claimed in Claim 1, characterised in that the measured value receiver
10 bridge circuit (G) and/or the switchable resistor (R_K) are connected to the change-over switch (SW) by means of operational amplifiers.

5. Analysing circuits as claimed in Claim 1, characterised in that the receiver bridge circuit (G)
15 and/or the switchable resistor (R_K) are connected to the change-over switch (SW) by opto-couplers.

6. Analysing circuits as claimed in Claim 3, characterised in that the measured value receiver
20 bridge circuit (G), which has its feed diagonal d.c. coupled to the change-over switch (SW), is divided at one of its diagonal points (3 or 1) and the switchable resistor (R_{K7} or R_{K8}) is inserted into the separating point, where the switching contact arm of the reverser (S_{U7} or R_{K8}) replaces the diagonal point at the
25 separating point and the input terminals of the preamplifier (VV) are arranged on the measuring diagonal of the measured value receiver bridge circuit (G).

7. Analysing circuits as claimed in Claim 4, characterised in that the feed diagonal of the measured
30 value receiver bridge circuit (G) is galvanically connected to the change-over switch (SW), the switchable resistor (R_{K9}) is connected between earth and the output of a first operational amplifier (V_{T1}) whose input terminals are arranged on the change-over
35 switch (SW), that the measuring diagonal of the measured value receiver bridge circuit (G) is arranged

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on the input terminals of a second operational amplifier (V_{T2}), whose output is connected to earth via a resistor and arranged on one of the input terminals of the preamplifier (VV), which has its other input terminal connected to the switching contact arm of the reverser (S_{U9}) which in the one position is connected to the output of the first operational amplifier (V_{T1}) and to earth in the other position.

8. Analysing circuits as claimed in Claim 4, characterised in that the feed diagonal of the measured value receiver bridge circuit (G) is d.c. coupled to the change-over switch (SW), the switchable resistor (R_{K13}) is connected via the reverser (S_{U13}) between the output of a first operational amplifier (V_{T3}), which has its input terminals connected to the change-over switch (SW), and earth, that the measuring diagonal of the measured value receiver bridge circuit (G) is arranged on the input terminals of a second operational amplifier (V_{T4}) whose output is connected via a resistor (R_{13}) to that input terminal of the preamplifier (VV) which is connected to one of the switching contacts of the reverser (S_{U13}), and the preamplifier (VV) is connected to earth by the other input terminal.

9. Analysing circuits as claimed in Claim 3, characterised in that a second resistor bridge circuit (K) is connected in parallel to the measured value receiver bridge circuit (G) at the supply end and the measuring diagonal end, where the second resistor bridge circuit (K) is divided at a measuring diagonal point, the switchable resistor (R_{K10}) is inserted into the separating point, and that the input terminals of the preamplifier (VV) are connected to the parallel measured diagonals of the two resistor bridge circuits (G, K).

10. Analysing circuits as claimed in Claim 9,



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characterised in that a semi-bridge, whose branches (R_3' , R_4') comprise the switchable resistor (R_{K11}), replaces the second resistor bridge.

5 characterised in that at the supply end and the measuring diagonal end a second resistor bridge (K) is connected parallel to the measured value receiver bridge circuit, which resistor bridge is divided at a feed diagonal point and the separating point is
10 occupied by two contacts of the reverser (S_{U12}), where the feed line is arranged on the switching contact arm of the reverser (S_{U12}), and that the input terminals of the preamplifier (VV) are connected to the parallel measured diagonals of the two resistor bridge circuits
15 (G, K).

12. Analysing circuits as claimed in Claim 3, characterised in that with the aid of the reverser (T_{01} , T_{02}) the switchable resistor (R_K) can be alternately connected in parallel to two resistors of
20 the measured value receiver bridge circuit (G), which are symmetrically arranged relative to a diagonal point, and the input terminals of the preamplifier (VV) are arranged on the measuring diagonal.

13. Analysing circuits as claimed in Claim 1, characterised in that a generator (TG) for a high-frequency pulse train is quartz-stabilised.
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14. Analysing circuits as claimed in Claim 2, characterised in that the symmetry of two branches of the phase-sensitive rectifier (D) is adjustable with
30 respect to earth by a potentiometer (PL).

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