CLAIMS

1. A method of manufacturing a tunnel field effect transistor (TFET), comprising:
   a) forming a dummy gate stack (310) surrounded by sidewall spacers (320) on a substrate (200) covered by epitaxially grown source material (220);
   b) forming doped source (510) and drain (520) regions followed by an inter-layer dielectric (ILD) (510) surrounding the sidewall spacers (320);
   c) removing the dummy gate stack (310) followed by etching a self-aligned cavity (710);
   d) epitaxially growing a thin channel within the self-aligned etch cavity; and
   e) depositing gate dielectric and gate materials within the self-aligned etch cavity.

2. The method of claim 1, wherein step b) is followed by exposing dummy gate materials by planarizing said dummy gate stack.

3. The method as recited in claim 2 wherein the planarizing extends over both the ILD and the dummy gate stack, exposing the dummy gate material within the gate stack.

4. The method of claim 1, further comprising forming the self-aligned etch cavity directly under the gate electrode by leveraging replacement gate.

5. The method of claim 1, wherein step e) is followed by planarizing a top surface of the replacement stack, removing residues of said gate dielectric and said metal gate materials.

6. The method of claim 3, further comprising removing said dummy gate stack and forming a self aligned etch cavity.

7. The method of claim 6, wherein said etch is performed during a replacement gate process, and wherein the dummy gate region defines the length and width of said etch cavity.

8. The method of claim 1 further comprising forming P+ and, N+ regions and intrinsic and lightly-doped regions separating the P+ and N+ regions, defining the source, body, and the drain regions.

9. The method of claim 8, wherein forming the P+ and N+ regions is performed by epitaxy, implant, or any combination thereof with an intrinsic or a lightly-doped region separating said P+ and N+ regions.

10. The method of claim 1, wherein said epitaxially grown channel extends over at least the source region, and wherein said epitaxially grown channel is doped or undoped.

11. The method of claim 1, wherein forming the replacement gate stack comprises the gate dielectric, and metal gate electrode over the epitaxially grown channel.

12. The method of claim 1 further comprises forming a TFET with predominantly transverse or longitudinal tunneling.

13. The method of claim 1 further comprising forming a thin epitaxial layer bridging the source, body and drain regions.

14. The method of claim 13, wherein said thin epitaxial layer between the N+ and P+ regions is modulated by said gate.

15. The method of claim 1, wherein removing the dummy gate to achieve the etch cavity is performed by any combination of wet and dry etching.

16. The method of claim 1, wherein the etch cavity comprises one of anisotropic, isotropic, or a sigma-shaped configuration.

17. The method of claim 16, wherein each etch results in an etch surface having different exposed crystal planes.

18. The method of claim 17 wherein the different exposed crystal planes maximize the TFET drive current, depending on materials and direction of an effective mass anisotropy.

19. The method of claim 17 wherein corner regions in the anisotropic and sigma recess etches confine the drain voltage drop to take place between corner regions and drain terminal, resulting in a uniform surface potential along BTBT perimeter at the source to the channel junction.

20. A tunnel field effect transistor (TFET) device, comprising:

a first doped source region for a first type TFET or a second doped source region (530) for a second type TFET;

a second doped drain region for the first type TFET or a first doped drain region (520) for the second type TFET;

a body region that is either intrinsic or doped, with a doping concentration less than that of the first or second source region, separating the first or second source from the first or second drain regions;

a self-aligned etch cavity (710) separating the first or second doped source (530) and drain (520) regions;

a thin epitaxial channel region that is grown within the self-aligned etch cavity (710), covering at least the first or the second source region;

a replacement gate stack (310) comprising a high-k gate dielectric and one or a combination of metals and polysilicon; and

sidewall spacers (320) adjacent to the replacement gate stack.

21. The TFET device of claim 20 further comprising a p+ source region of an n-type TFET or an n+ source region of a p-type TFET; an n+ drain region for the n-type TFET or a p+ drain region for the p-type TFET; a body region that is either intrinsic or doped, with a doping concentration less than that of the source region, separating the p+ and n+ source and drain regions; a self-aligned etch cavity separating the p+ and n+ source and drain regions; a thin epitaxial channel region grown within the self-aligned etch cavity, covering at least the source region; a replacement gate stack comprising a high-k gate dielectric and one or a combination of metals; and sidewall spacer regions adjacent to the replacement gate stack.

CLAIMS

1. A method of manufacturing a tunnel field effect transistor, comprising:

a) forming a dummy gate stack (310) surrounded by sidewall spacers (320) on a substrate (200) covered by epitaxially grown source material (220);

b) forming doped source (530) and drain (520) regions followed by an inter-layer dielectric (510) surrounding the sidewall spacers (320) by forming P+ and, N+ regions and intrinsic and lightly-doped regions separating the P+ and N+ regions, defining the source, and drain regions, and a body region;

c) removing the dummy gate stack (310) followed by etching a self-aligned cavity (710);

d) epitaxially growing a channel within the self-aligned etch cavity; and

e) depositing gate dielectric and gate materials within the self-aligned cavity to form a replacement gate stack.

2. The method of claim 1, wherein step b) is followed by exposing dummy gate materials by planarizing said dummy gate stack.

3. The method as recited in claim 2 wherein the planarizing extends over both the inter-layer dielectric and the dummy gate stack, exposing the dummy gate material within the gate stack.

4. The method of claim 1, wherein step e) is followed by planarizing a top surface of the replacement stack, removing residues of said gate dielectric and said gate materials.

5. The method of claim 1, wherein the dummy gate stack defines the length and width of said etch cavity.

6. The method of claim 1, wherein forming the P+ and N+ regions is performed by epitaxy, implant, or any combination thereof with an intrinsic or a lightly-doped region separating said P+ and N+ regions.

7. The method of claim 1, wherein said epitaxially grown channel extends over at least the source region, and wherein said epitaxially grown channel is doped or undoped.

8. The method of claim 1, wherein the replacement gate stack comprises the gate dielectric and gate materials over the epitaxially grown channel.

9. The method of claim 1 further comprising forming a tunnel field effect transistor with predominantly transverse or longitudinal tunneling.

10. The method of claim 1 further comprising forming a thin epitaxial layer bridging the source, body and drain regions.

11. The method of claim 10, wherein said thin epitaxial layer between the N+ and P+ regions is modulated by said gate.

12. The method of claim 1, wherein removing the dummy gate to achieve the etch cavity is performed by any combination of wet and dry etching.

13. The method of claim 1, wherein the etch cavity comprises one of anisotropic, isotropic, and a sigma-shaped configuration as herein defined to produce an etch surface having different exposed crystal planes to maximize the tunnel field effect transistor drive current, depending on materials and direction of an effective mass anisotropy.

14. The method of claim 13 wherein the etch cavity comprises one of anisotropic and sigma-shaped configurations with corner regions confining drain voltage drop to between such corner regions and a drain terminal to provide uniform surface potential along band-to-band tunnel barrier at the source to channel junction.

15. A tunnel field effect transistor device, comprising:

one of a P+ source region for an N- type tunnel field effect transistor and a N+ source region (530) for a P- type tunnel field effect transistor;

one of a N+ drain region for the N- type tunnel field effect transistor and a P+ drain region (520) for the P- type tunnel field effect transistor;

a self-aligned etch cavity (710) separating the source (530) and drain (520) regions;

an epitaxial channel region that is within the self-aligned etch cavity (710), covering at least the source region;

a gate stack (310) comprising a gate dielectric and gate materials within the self-aligned cavity; and

sidewall spacers (320) adjacent to the gate stack.