

ABSTRACT

A method for manufacturing a silicon optical interposer and a method for manufacturing a three-dimensional structure, which provide a smaller chip package, a shorter delay of electrical signals, a higher degree of integration, a larger bandwidth, and a higher speed. A method for integrating a surface-electrode ion trap and a silicon optoelectronic device, an integrated structure, and a three-dimensional structure, which are highly stable, miniaturized, universal and scalable. Integration of the three-dimensional structure is based on integration of the through silicon vias and the silicon optoelectronic device, which reduces a size of the integrated chips and improves a degree integration. The manufactured three-dimensional structure has a smaller delay in electrical signal, a larger bandwidth, and a higher speed, in comparison with a conventional planar structure or a three-dimensional structure integrated through wire bonding. The surface-electrode ion trap is integrated with the silicon single-photon avalanche detector or the silicon-based germanium single-photon avalanche detector, with the silicon grating and/or the silicon nitride grating, and with a through silicon via. Ions are trapped within a certain range by the surface-electrode ion trap after being powered. A laser source is coupled to the silicon grating and/or the silicon nitride grating through a coupling manner, such as end-coupling. Laser is emitted to the ions in three directions via the silicon gratings and/or the silicon nitride gratings, so as to achieve addressing. The ions are subject to energy level transition after being excited by the laser, and emit fluorescence after the energy level transition. The fluorescence is detected by the silicon single-photon avalanche detector or the silicon-based germanium single-photon avalanche detector, and therefore information of the quantum bits is detected.