

**SEMICONDUCTOR CONSTRUCTIONS, MEMORY ARRAYS, ELECTRONIC
SYSTEMS, AND METHODS OF FORMING SEMICONDUCTOR
CONSTRUCTIONS**

ABSTRACT

The invention includes semiconductor constructions having trenched isolation regions. The trenches of the trenched isolation regions can include narrow bottom portions and upper wide portions over the bottom portions. Electrically insulative material can fill the upper wide portions while leaving voids within the narrow bottom portions. The bottom portions can have substantially vertical sidewalls, and can join to the upper portions at steps which extend substantially perpendicularly from the sidewalls. The trenched isolation regions can be incorporated into a memory array, and/or can be incorporated into an electronic system. The invention also includes methods of forming semiconductor constructions.

FIGURE 5