CLAIMS

1. An inverter-based resistor comprising at least one digital inverter, wherein each of the at least one digital inverter is configured to receive an input and provide an output, each of the at least one digital inverter further comprises a positive voltage rail and a negative voltage rail, wherein the digital inverter input is connected to the inverter output and the positive voltage rail is connected to the negative voltage rail, and wherein a current flowing through the inverter-based resistor varies in direction and magnitude of the current in response to a digital input provided to the positive voltage rail and the negative voltage rail.

2. The inverter-based resistor of claim 1, wherein each of the at least one digital inverter comprises at least one pair of transistors.

3. The inverter-based resistor of claim 2, wherein each of the at least one pair of transistors comprises a pair of field effect transistors (FETs).

4. The inverter-based resistor of claim 3, wherein the pair of field effect transistors comprises a pair of metal-oxide semiconductor field effect transistors (MOSFETs).

5. The inverter-based resistor of claim 4, wherein the pair of MOSFETs comprises a first MOSFET and a second MOSFET, wherein a source of the first MOSFET is connected to a source of the second MOSFET, and wherein a gate of the first MOSFET, a gate of the second MOSFET, a drain of the first MOSFET and a drain of the second MOSFET are all connected.

6. An analog-to-digital converter (ADC) comprising:

a phase feedback voltage controlled oscillator (VCO) quantizer having a VCO input and a quantizer output; and

a feedback loop coupling the VCO input of the phase feedback VCO quantizer to the quantizer output of the phase feedback VCO quantizer, the feedback loop comprising one or more inverter-based resistance devices, wherein each of the one or more digital resistance devices comprises at least one digital inverter.

7. The ADC of claim 6, wherein each of the at least one digital inverter is configured to receive an input and provide an output, the digital inverter further comprising a positive voltage rail and a negative voltage rail, wherein the digital inverter input is connected to the digital inverter output and the positive voltage rail is connected to the negative voltage rail.

8. The ADC of claim 7, wherein the each of the at least one digital inverter comprises at least one pair of transistors.

9. The ADC of claim 8, wherein the each of the at least one pair of transistors comprises at least one pair of field effect transistors (FETs).

10. The ADC of claim 9, wherein each of the at least one pair of field effect transistors comprises at least one pair of metal-oxide semiconductor field effect transistors (MOSFETs).

11. The ADC of claim 10, wherein a resistance of the each of the at least one digital inverter varies in response to sizes of the MOSFETs.

12. The ADC of claim 11, wherein each of the at least one pair of MOSFETs comprises a first MOSFET and a second MOSFET, wherein a source of the first MOSFET is connected to a source of the second MOSFET, and wherein a gate of the first MOSFET, a gate of the second MOSFET, a drain of the first MOSFET and a drain of the second MOSFET are all connected.

13. A method for dynamically generating resistance in a digital-only circuit, the method comprising:

providing at least one digital inverter, wherein each of the at least one digital inverter is configured to receive an input and provide an output, the digital inverter comprising a positive voltage rail and a negative voltage rail, wherein the digital inverter input is connected to the digital inverter output and the positive voltage rail is connected to the negative voltage rail of each of the at least one digital inverter;

providing a first voltage at both the positive voltage rail terminal and the negative voltage rail terminal;

providing a current to flow through each of the at least one digital inverter from the positive voltage rail terminal or the negative voltage rail terminal to the digital inverter output; and

varying a direction of the current flowing through the each of the at least one digital inverter to dynamically generate resistance of the at least one digital inverter.

14. The method of claim 13, wherein the step of providing the bi-directional current to flow through the each of the at least one digital inverter from the digital inverter input to a positive voltage rail or a negative voltage rail comprises providing a second voltage at the digital inverter input and/or the digital inverter output.

15. The method of claim 13, wherein the digital-only circuit is an analog-to-digital converter (ADC) and wherein the step of providing the at least one digital inverter comprises providing a feedback loop connecting an input of a phase feedback voltage-controlled oscillator (VCO) quantizer to an output of the phase feedback VCO quantizer, the feedback loop comprising the at least one digital inverter.