Description

BACKGROUND OF THE INVENTION

The present invention relates to semiconductor integrated circuit devices, and more particularly to a semiconductor integrated circuit device in which a measure against hot carriers and a measure against electrostatic breakdown are taken and whose internal circuit has a MOS field effect transistor of the LDD (Lightly Doped Drain) structure, as well as a method of manufacturing the same.

In a semiconductor device, especially microminiaturized semiconductor device, comprising metal-oxide-semiconductor field effect transistors (MOSFETs), it is proposed to employ the LDD structure for a source and a drain to the end of preventing the appearance of hot carriers. With the LDD structure, source and drain regions are constructed of a high impurity concentration region which is formed away from a gate electrode (hereinbelow, expressed as 'formed in offset to a gate electrode'), and a low impurity concentration region which is disposed between the high impurity concentration region and the gate electrode. Owing to the LDD structure, the electric field of a drain edge in the direction of a channel is relaxed, with the result that the appearance of hot carriers is suppressed. Thus, the degradations of element characteristics attributed to the hot carriers can be restrained to enhance reliability. In case of, for example, an N-channel MOSFET (hereinbelow, termed 'NMOSFET') the low impurity concentration region mentioned above is set at a concentration on the order of 10^{13} cm^{-2} and at a length of 0.2 - 0.4 μm.

The LDD is described in "P. J. Tsang et al, IEEE Transactions on Electron Devices, Vol. ED-29, No. 4, P 590 (1982)".

SUMMARY OF THE INVENTION

Using the LDD structure, the inventors manufactured D-RAMs (Dynamic-RAMs) etc. by way of trial. Then, it has been revealed that electrostatic breakdown voltages in input/output circuits are problematic. That is, in a case where an element of the LDD structure is utilized as an element in a place, such as the input or output circuit, to which external electrostatic energy is directly applied, particularly as an input protective element, the breakdown or destruction of a gate insulator film is induced even by comparatively low electrostatic energy. A cause therefor will be that, since a voltage with which the input protective element turns 'on' is raised by the presence of the low impurity concentration region, a voltage to act on the gate insulator film becomes higher, resulting in a lower electrostatic breakdown voltage.

The inventors therefore repeated studies, and have found out the following.

As regards the prevention of hot carriers, it is more effective to make the source and drain regions of a MOSFET for the input or output circuit, out of phosphorus than to make them out of only arsenic. A circuit using such MOS-transistors for the input or output circuit is known from EP-A-0 043 284. Further, in a case where the source and drain regions of the MOSFET of the input or output circuit are formed by utilizing phosphorus used for the low impurity concentration region of the LDD structure, the impurity concentration is not satisfactory That is, the voltage with which the protective element turns 'on' becomes high. Besides, in a case where phosphorus at a high concentration is introduced into a substrate by an ordinary method (a method employing a gate electrode as a mask) in order to form the source and drain regions, an effective channel length under a gate (gate effective length) becomes small because the diffusion rate of phosphorus is great. When it is intended to cope with this drawback, the length of the gate increases contrariwise to the microminiaturization of the semiconductor device. Of course, the hot carriers appear with the construction which uses only arsenic for the formation of the source and drain regions.

An object of the present invention is to enhance the breakdown or destruction voltage of a MOS type semiconductor integrated circuit device.

Another object of the present invention is to provide a semiconductor device which can enhance an electrostatic breakdown or destruction (ESD) voltage in a semiconductor device employing a MOSFET of the LDD structure in its internal circuit.

Another object of the present invention is to provide a semiconductor device which renders the appearance of hot carriers difficult while enhancing an electrostatic breakdown voltage.

A further object of the present invention is to provide a semiconductor device which can achieve rise in the operating speed of an element without increasing the resistances of source and drain regions.

Still another object of the present invention is to provide a method of manufacturing a semiconductor device which can produce the aforementioned semiconductor devices readily without drastically altering a manufacturing process for a semiconductor device of the LDD structure. The above objects are solved by a semi conductor integrated circuit device according to the appended claims.

The above-mentioned and other objects and novel features of the present invention will become apparent from the description of this specification and the accompanying drawings.

Typical aspects of performance of the present invention will be briefly summarized below.

The input or output circuit of a semiconductor device employing a MOSFET of the LDD structure in its internal circuit is constructed of a MOSFET of a structure in which source and drain regions are doped with phosphorus at a high concentration. Thus, enhancement in an electrostatic destrustion voltage is achieved, while the appearance of hot carriers is rendered difficult.

Further, phosphorus at a high concentration is introduced in such a way that side wall spacers formed on both the sides of a gate electrode are used as a mask. Thus, notwithstanding that the diffusion rate of phosphorus is great, source and drain regions which overlap the gate electrode little can be formed. As the step of forming the side wall spacers, the step of forming side wall spacers for the LDD structure of the internal circuit can be utilized as it is, so that sharp increase in the number of steps is not involved.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a sectional view showing an embodiment of the present invention.

Figs. 2A - 2G are sectional views showing a manufacturing process for the embodiment in Fig. 1.

Fig. 3 is a sectional view of another embodiment of the present invention.

Figs. 4A and 4B are sectional views showing some steps of a manufacturing process for the embodiment in Fig. 3.

Figs. 5 and 6 are circuit diagrams showing examples of input and output circuits to which the present invention is applied, respectively.

Fig. 7 is a sectional view showing still another embodiment of the present invention.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

Fig. 1 shows an embodiment in which the present invention is applied to a semiconductor device, for example, a D-RAM constructed of complementary MOSFETs. A region 1 is a region (input/output circuit region) in which an element for an input/output circuit is formed, while a region 2 is a region (internal circuit region) in which elements constituting an internal circuit other than a memory cell are formed. The figure illustrates the sections of the respective elements.

An NMOSFET 11 is formed as the element of the input/output circuit 1 on a semiconductor substrate 10 made of a P-type silicon single crystal. An NMOSFET 12 and a P-channel MOSFET (hereinbelow, termed 'PMOSFET') 13 are respectively formed as the elements of the internal circuit 2 on the substrate 10 and an N-type well 14 provided therein. The individual MOSFETs are insulated from one another by a field insulator film (SiO_2) 15 which is an element isolating insulator film.

The NMOSFET 11 comprises a gate electrode 17 made of polycrystalline silicon, which is formed on a gate insulator film (SiO_2) 16, and N-type regions 18 as source and drain regions, which are provided in the main surface of the substrate 10. Side wall spacers (insulator films) 22 made of SiO_2 are formed on both the sides of the gate electrode 17 by the low-pressure CVD process. However, the MOSFET 11 has no LDD structure. Each of the N-type regions 18 is composed of a region (low concentration phosphorus region) 19 which is doped with phosphorus at a low concentration, and a region (high concentration phosphorus region) 20 which is doped with phosphorus at a high concentration. In case of this example, the concentrations of the respective phosphorus regions 19 and 20 are 10^{13} cm^{-2} (approximately 1×10^{18} cm^{-3}) or less and $1 - 10 \times 10^{15}$ cm^{-2}. In particular, the phosphorus region 20 is set at a concentration of $1 - 20 \times 10^{19}$ cm^{-3} or above. The concentration of the phosphorus region 20 needs to be, at least, higher than that of a phosphorus region 26 to be described later. The inventors have verified that, even when the phosphorus regions of such a high concentration are used as the source and drain regions, the appearance of hot carriers is little, while a strength against electrostatic destruction increases, as will be stated later. In addition, the depths of junctions which the respective regions 19 and 20 define with the substrate 10 are set to 0.2 μm and 0.5 μm. The high concentration phosphorus regions 20 have their inner ends diffused to positions under both the ends of the gate electrode 17, into the shape in which they encompass the low concentration phosphorus regions 19 therein.

The NMOSFET 12 comprises a gate electrode 23 made of polycrystalline silicon on a gate insulator film 16, and N-type regions 24 as source and drain regions. Side wall spacers 25 are formed on both the sdies of the gate electrode 23. Each of the N-type regions 24 is composed of the low concentration phosphorus region 26, and a region (arsenic region) 27 which is doped with arsenic at a high concentration. In particular, the arsenic region 27 is formed so as to be apart from a projection of the gate electrode 23 in the main surface of the substrate 10 by the side wall spacer 25, and the

low concentration phosphorus region 26 is formed so as to extend to under the side wall spacer 25. Thus, the so-called LDD structure is established. The concentration of the low concentration phosphorus region 26 is at most 10^{13} cm^{-2} (approximately 1 x 10^{18} cm^{-3}), and that of the arsenic region 27 is 5 - 10 x 10^{15} cm^{-2} (1 - 4 x 10^{20} cm^{-3}). The depths of junctions which the respective regions 26 and 27 define with the substrate 10 are 0.2 μm and 0.2 - 0.3 μm.

The PMOSFET 13 comprises a gate electrode 28 made of polycrystalline silicon on a gate insulator film 16, and P-type regions 29 as source and drain regins formed in the N-type well 14. In this example, the PMOSFET 13 is not of the LDD structure. The P-type regions 29 are formed by doping with boron at a concentration of approximately 5 x 10^{15} cm^{-2}.

Layers 33 and 34 of a silicide of platinum or a refractory metal are respectively formed on the surfaces of the source and drain regions 18, 24 and 29 and the gate electrodes 17, 23 and 28. In the figure, numeral 31 designates an inter-layer insulator film which is made of phosphosilicate glass (PSG) or the like, and numeral 32 a wiring layer which is made of aluminum.

Fig. 5 is a diagram showing an input circuit, while Fig. 6 is a diagram showing an output circuit, and they exemplify the input/output circuits 1 respectively. As seen from Figs. 5 and 6, the input/output circuits 1 are circuits which are connected to bonding pads BP. NMOSFETs Q_{N1} - Q_{N3} and PMOSFETs Q_{P1}, Q_{P2} are respectively put into the same structures as those of the NMOSFET 11 and the PMOSFET 13. The internal circuit 2 includes a portion except for the input/output circuits 1 and the memory cell, in other words, a circuit such as decoder, sense amplifier, main amplifier or any of various signal generators.

In the present embodiment, the NMOSFET of the memory cell is put into the same structure as that of the NMOSFET 12.

According to this construction, in the NMOSFET 12 in the internal circuit 2, the N-type region 24 is formed into the LDD structure by the arsenic region 27 and the low concentration phopshorus region 26, so that an electric field at the edge of the drain region 24 can be moderated to suppress the appearance of hot carriers. As a result, the fluctuation of a threshold voltage can be prevented to enhance the reliability of characteristics in the internal circuit 2.

On the other hand, in the NMOSFET 11 of the input/output circuit 1, the source or drain region (N-type region) 18 is formed of the high concentration phosphorus region 20 encompassing the low concentration phosphorus region 19, so that the reverse breakdown voltage of the junction between the high concentration phosphorus region 20 and the substrate 10 becomes small. Thus, the destruction voltage of the gate insulator film against electrostatic destruction can be enhanced.

By setting the source and drain regions 18 at the high impurity concentration, the electric field strength is raised. Since, however, the impurity is phosphorus, the impurity concentration gradient is gentle, and hence, the appearance of hot carriers as in the case of arsenic is not involved. Of course, in the input/output circuits, the influences of the hot carriers are originally little on the basis of the relations between element sizes and voltages to be applied.

Further, owing to the use of the silicide layer 33, it is possible to reduce the resistance of the semiconductor region 18 and to raise the operating speed of the element even when phosphorus is employed as the impurity.

Next, a method of manufacturing the semiconductor device of the above construction will be described with reference to Figs. 2A - 2G.

First, as shown in Fig. 2A, an N-type well 14 is formed in a semiconductor substrate 10 made of a P-type silicon single crystal, and an element isolating insulator film (field insulator film) 15 and a gate insulator film 16 are formed. Polycrystalline silicon is deposited on the whole surface of the substrate by CVD, and it is patterned to form gate electrodes 17, 23 and 28 of respective MOSFETs 11, 12 and 13. It is needless to say that these gate electrodes are formed of a second polycrystalline silicon layer in the case of a D-RAM.

Subsequently, as shown in Fig. 2B, under the state under which the portion of the PMOSFET 13 is masked by a photoresist film 40, phosphorus at a low concentration (10^{13} cm^{-2} or less) is ion-implanted into the whole surface by employing the gate electrodes 17 and 23 as a mask. Thus, low-concentration ion-implanted layers 41 are formed. At this time, an input/output circuit domain 1 may well be covered with the photoresist film 40 so as to prevent the phosphorus from being introduced into the source and drain regions of the NMOSFET 11.

After removing the photoresist film 40, the resultant structure is annealed thereby to form low concentration phosphorus regions 19 and 26 in the respective NMOSFETs 11 and 12 as shown in Fig. 2C. An SiO_2 film 42 is formed on the whole surface of the substrate by the low-pressure CVD process or the like.

The SiO_2 film 42 is etched by reactive ion etching (RIE), whereby side wall spacers 22, 25 and 30 are respectively formed on both the sides of the gate electrodes 17, 23 and 28 as shown in Fig. 2D.

Next, as shown in Fig. 2E, under the state under which an internal circuit region 2, namely, the portion of the NMOSFET 12 as well as the portion of the PMOSFET 13 is masked by a photoresist film 43, phosphorus at a high concentration ($1 - 10 \times 10^{15}$ cm^{-2}) is ion-implanted by employing the gate electrode 17 and the side wall spacers 22 as a mask. Thus, layers 44 ion-implanted with the high concentration of phosphorus are formed.

After removing the photoresist film 43, the resultant structure is annealed thereby to form source and drain regions 18 made up of high concentration phosphorus regions 20 encompassing the low concentration phosphorus regions 19 as shown in Fig. 2F.

Thereafter, as shown in Fig. 2F, under the state under which the PMOSFET 13 and the input/output circuit region 1 are masked by a photoresist film 45, arsenic is ion-implanted at a concentration of $5 - 10 \times 10^{15}$ cm^{-2} by employing the gate electrode 23 and the side wall spacers 25 as a mask. Thus, arsenic ion-implanted layers 46 are formed for the NMOSFET 12.

By annealing after the removal of the photoresist film 45, arsenic regions 27 are formed as shown in Fig. 2G. That is, the source and drain regions 24 of the NMOSFET 12 of the internal circuit 2 are finished up as the LDD structures.

Subsequently, as shown in Fig. 2G, under the state under which the NMOSFETs 11 and 12 are masked by a photoresist film 47, boron (B) is ion-implanted at a concentration of 5×10^{15} cm^{-2} by employing the gate electrode 28 and the side wall spacers 30 as a mask. Thus, boron-implanted layers are formed. By annealing after the removal of the photoresist film 47, P^+-type regions 29 as source and drain regions are formed. Thereafter, the parts of the insulator film 16 on the source and drain regions are removed. Subsequently, a metal film of molybdenum (Mo) or the like is formed on the whole surface of the resultant substrate and is heat-treated into a silicide, and the unreacted parts of the metal film are removed, whereby silicide layers 33 and 34 are formed.

Thenceforth, an inter-layer insulator film 31,aluminum wiring 32 and final passivation film (not shown) are formed by well-known processes, whereby the semiconductor device in Fig. 1 can be completed.

With this method, the NMOSFET of the input/output circuit can be readily formed merely by adding the masking step of the photoresist film 43 and the doping step of the high concentration phosphorus as shown in Fig. 2E, to the steps of fabricating the NMOSFET (12) of the LDD structure. Besides, in forming the high concentration phosphorus regions 20, the side wall spacers 22 are utilized, and hence, the high concentration phosphorus regions 20 can be formed into a required depth. Also, the channel length can be readily formed into a required length, and increase in the channel length is not incurred, which is effective for microminiaturization.

Fig. 3 shows another embodiment of the present invention. In the figure, the same portions as in Fig. 1 are assigned the same symbols, and they shall not be repeatedly explained.

In this example, each of N-type regions 18A as the source and drain regions of the NMOSFET 11A of an input/output circuit 1 comprises a low concentration phosphorus region 19, a high concentration phosphorus region 20 so as to substantially encompass the region 19, and an arsenic region 21 which is formed on the surface side of the region 20 and shallower than this region 20 and to be apart from a gate electrode 17. The concentrations of the phosphorus regions 19 and 20 are the same as in the foregoing example, and the concentration of the arsenic region 21 is the same as that of the arsenic region 27 of the NMOSFET 12 of an internal circuit 2. The depths of the respective regions 19, 20 and 21 are 0.2 μm, 0.5 μm and 0.2 - 0.3 μm.

A method of manufacturing this semiconductor device is as follows. First, the steps of Fig. 2A - Fig. 2E in the foregoing example are carried out. Thereafter, as shown in Fig. 4A, under the state under which only the PMOSFET 12 of the internal circuit 2 is covered with a mask of photoresist 50, arsenic is ion-implanted at a concentration of $5 - 10 \times 10^{15}$ cm^{-2}. Arsenic ion-implanted layers 51 formed for both the NMOSFETs 11A and 12 are annealed, and the arsenic regions 21 and 27 being apart from respect to the corresponding gate electrodes 17 and 23 can be formed. Thus, the above-stated construction of the source and drain regions 18A is obtained in the NMOSFET 11A, and the LDD structures are obtained in the NMOSFET 12.

Subsequently, as shown in Fig. 4B, the NMOSFETs 11A and 12 are masked by the use of a photoresist film 52, and if necessary, side wall spacers 30 are etched and removed, whereupon boron is ion-implanted. By subsequent annealing, source and drain regions 29 are formed.

Thereafter, an inter-layer insulator film 31, aluminum wiring 32 and final passivation film are formed, whereby the semiconductor device in Fig. 3 is finished up.

According to this example, the NMOSFET 12 of the internal circuit 2 is put into the LDD construction as in the preceding example, so that the appearance of hot carriers is suppressed. On the other hand, in the NMOSFET 11A of the input/output circuit, the main constituents of the source and drain regions 18A are the high con-

centration phosphorus regions 20 extended to both the ends of the gate electrode 17, so that the electrostatic destruction voltage can be enhanced. Moreover, the regions 20 have the high impurity concentration but use phosphorus, so that the lowering of the hot carrier generation can be suppressed.

Further, since the arsenic regions 21 apart from the gate electrode are included in the source and drain regions 18A, the overlaps of the high concentration phosphorus regions 20 with the gate electrode 17 can be made smaller than in the preceding example, and the transconductance can be enhanced owing to reduction in the junction capacitances. Of course, the operating speed can also be raised by the lowered resistances of the source and drain regions 18A owing to the arsenic regions 21.

Even in a case where the high concentration phosphorus regions 20 do not get to both the sides of the gate electrode 17, the low concentration phosphorus regions 19 previously formed have been formed by utilizing the gate electrode 17 and reliably extend to under this gate electrode, so that the MOS structure is not spoilt.

According to the present invention, the following effects are produced.

In a semiconductor device whose internal circuit has a MOSFET of the LDD structure, the source and drain regions of a MOSFET for an input/output circuit are so constructed as to be doped with phosphorus at a high concentration, so that the electrostatic destruction voltage can be enhanced.

Since source and drain regions are constructed by the use of phosphorus at a high concentration, the concentration gradient is gentle in spite of the high impurity concentration, and the apperance of hot carriers can be suppressed.

Since the concentration of phosphorus is made as high as 1 - 20 x 10^{19} cm^{-3}, the appearance of hot carriers can be suppressed, and the electrostatic destruction voltage can be enhanced.

Only an input/output circuit is provided with regions made by the use of a high concentration of phosphorus, and the others are put into the LDD structures, so that even when the junction capacitances between a substrate and the phosphorus regions increase, the operating speed of the whole IC does not lower.

Since source and drain regions are formed with arsenic regions, resistances can be reduced to achieve a raised speed.

Since source and drain regions are formed with silicide layers, resistances can be reduced to achieve a raised speed.

Since source and drain regions are formed with arsenic regions a part with respect to a gate electrode, the overlaps between phosphorus regions and the gate electrode can be diminished, and junction capacitances can be reduced to enhance a transconductance.

Since the overlaps between a gate electrode and high concentration phosphorus regions can be diminished, a gate length relative to an effective gate length is shortened, which is effective for the microminiaturization of an element.

Under the state under which at least an internal circuit is masked, doping with a high concentration of phosphorus is carried out by utilizing side wall spacers, whereupon doping with arsenic is carried out for at least the internal circuit by utilizing the side wall spacers. Thus, the LDD structures can be formed in the internal circuit, and source and drain regions of the high concentration of phosphorus can be formed in an input/output circuit. A semiconductor device of the present invention can be readily manufactured by adding the step of the masking and the step of the doping with the high concentration of phosphorus, to a process for manufacturing an NMOSFET of the LDD structure.

An impurity is introduced by doping beforehand with a gate electrode used as a mask. Therefore, even when the diffusion of a high concentration of phosphorus is insufficient in case of doping with the high concentration of phosphorus, the MOS structure is not spoilt.

While, in the above, the invention made by the inventors has been concretely described in conjunction with embodiments, it is needless to say that the present invention is not restricted to the foregoing embodiments but that it can be variously modified within a scope not departing from the purport thereof.

The present invention is effective for a MOSFET, Q_{N1} or Q_{N3} whose drain is connected to a bonding pad, especially a bonding pad to which an input or output signal is applied. The reason is that electrostatic breakdown is liable to occur in a circuit connected to the bonding pad to which the input or output signal is applied.

Accordingly, the MOSFET Q_{N2} in Fig. 5 need not be put into the same structure as that of the MOSFET 11. To the contrary, the present invention is also applicable to an NMOSFET constituting a circuit of the next stage which is connected to an inverter INV_1 or INV_2 constructed of the MOSFET Q_{N1} or Q_{N3}. Further, it is possible that only the drain region of an N-channel MOSFET such as the MOSFET Q_{N1} or Q_{N3} is put into the structure conforming with the present invention.

The low impurity concentration regions 19 in the MOSFET 11 can be omitted. As shown in Fig. 7, each of the source and drain regions 18 of the

MOSFET 11 is made up of only the phosphorus region 20 of high impurity concentration. This can be achieved in such a way that the resist mask 40 shown in Fig. 2B is formed so as to cover the input/output circuit domain 1. That is, the number of manufacturing steps does not increase in a CMOSIC. In an IC (NMOSIC) which is constructed of NMOSFETs without having the PMOSFET 13, a masking step needs to be added.

As shown in Fig. 7, the layers 33 and 34 of the silicide of platinum or a refractory metal can be omitted.

An input protective resistor R shown in Fig. 5 can be formed by extending the source or drain region 18 of the MOSFET 11. In case of forming a resistor R made of a semiconductor region which is identical and continuous to the region 18, the structure shown in Fig. 7 is desirable. That is, the source and drain regions 18 of the MOSFET 11 are constructed only of the phosphorus regions 20. The resistor R is formed by extending either phosphorus region 20. In order to bring the sheet resistance of the region 20 to a proper value, the silicide layer 33 is not formed. For the same reason, at least the arsenic region 27 is not formed. Accordingly, the resistor R can be formed in a small area. One end of the resistor R is connected to the bonding pad BP which is made of the aluminum layer 32.

While, in the above, the invention made by the inventors has been chiefly described on the applications to semiconductor devices of the CMOS type which form the background field of utilization, it is not restricted thereto. The present invention is applicable to a memory IC and also a logic IC other than a DRAM as long as a MOSFET of the LDD structure is included in an internal structure. Further, it is applicable, not only to CMOSICs, but also to NMOSICs. The LDD structure in the present invention may include, at least, a first semiconductor region has a high impurity concentration, and a second semiconductor region which has an impurity concentration lower than that of the first semiconductor region and which is formed closer to a channel side (gate electrode side) than the first semiconductor region. The first semiconductor region need not be deeper than the second semiconductor region. A bonding pad includes, not only a pad for wire bonding, but also a pad for bonding which utilizes a bump electrode or the like. Various semiconductor regions may well be opposite in conductivity type to the foregoing. The concentrations of phosphorus and arsenic can be variously altered within the scope of the purport of the present invention.

Claims

1. A semiconductor integrated circuit device comprising

   a first MOSFET (12) forming part of an internal circuit (1), and

   a second MOSFET (11) forming part of an input/output circuit (2), the second MOSFET (11) being formed on the same semiconductor substrate (10), and being of the same conductivity type, as the first MOSFET (12), having a source/drain region (18) which is connected to a bonding pad and a gate insulator film (16) of the same thickness as that of the first MOSFET (12),

   characterized in

   that the source/drain region (24) of the first MOSFET (12) includes a first semiconductor region (27) of high impurity concentration and a second semiconductor region (26) which has a lower impurity concentration, and is formed closer to the channel, than the first semiconductor region (27), and

   that the source/drain region (18) of the second MOSFET (11) includes a third semiconductor region (20) being in contact with with the substrate (10) and having a higher impurity concentration than the second semiconductor region (26) of the first MOSFET (12).

2. The device of claim 1, wherein said first and second MOSFETs (12, 11) are N-channel MOSFETs, and said first, second and third semiconductor regions (27, 26, 20) respectively include arsenic, phosphorus and phosphorus as impurities.

3. The device of claim 1 or 2, further comprising a third MOSFET (13) formed on said semiconductor substrate (10) and being of a conductivity type opposite to that of the first and second MOSFETs (12,11).

4. The device of any of claims 1 to 3, wherein the impurity concentration of said third semiconductor region (20) is at least $1 \times 10^{19}/cm^3$.

5. The device of many of claims 1 to 4, further comprising side wall spacers (25, 22, 30) which are formed on two side walls of each of the gate electrodes (23, 17, 28) of said first, second and third MOSFETs (12, 11, 13),

   wherein said first semiconductor region (27) is defined by said gate electrode (23) of said first MOSFET (12) and said side wall

MOSFET 11 is made up of only the phosphorus region 20 of high impurity concentration. This can be achieved in such a way that the resist mask 40 shown in Fig. 2B is formed so as to cover the input/output circuit domain 1. That is, the number of manufacturing steps does not increase in a CMOSIC. In an IC (NMOSIC) which is constructed of NMOSFETs without having the PMOSFET 13, a masking step needs to be added.

As shown in Fig. 7, the layers 33 and 34 of the silicide of platinum or a refractory metal can be omitted.

An input protective resistor R shown in Fig. 5 can be formed by extending the source or drain region 18 of the MOSFET 11. In case of forming a resistor R made of a semiconductor region which is identical and continuous to the region 18, the structure shown in Fig. 7 is desirable. That is, the source and drain regions 18 of the MOSFET 11 are constructed only of the phosphorus regions 20. The resistor R is formed by extending either phosphorus region 20. In order to bring the sheet resistance of the region 20 to a proper value, the silicide layer 33 is not formed. For the same reason, at least the arsenic region 27 is not formed. Accordingly, the resistor R can be formed in a small area. One end of the resistor R is connected to the bonding pad BP which is made of the aluminum layer 32.

While, in the above, the invention made by the inventors has been chiefly described on the applications to semiconductor devices of the CMOS type which form the background field of utilization, it is not restricted thereto. The present invention is applicable to a memory IC and also a logic IC other than a DRAM as long as a MOSFET of the LDD structure is included in an internal structure. Further, it is applicable, not only to CMOSICs, but also to NMOSICs. The LDD structure in the present invention may include, at least, a first semiconductor region has a high impurity concentration, and a second semiconductor region which has an impurity concentration lower than that of the first semiconductor region and which is formed closer to a channel side (gate electrode side) than the first semiconductor region. The first semiconductor region need not be deeper than the second semiconductor region. A bonding pad includes, not only a pad for wire bonding, but also a pad for bonding which utilizes a bump electrode or the like. Various semiconductor regions may well be opposite in conductivity type to the foregoing. The concentrations of phosphorus and arsenic can be variously altered within the scope of the purport of the present invention.

Claims

1. A semiconductor integrated circuit device comprising

a first MOSFET (12) forming part of an internal circuit (1), and

a second MOSFET (11) forming part of an input/output circuit (2), the second MOSFET (11) being formed on the same semiconductor substrate (10), and being of the same conductivity type, as the first MOSFET (12), having a source/drain region (18) which is connected to a bonding pad and a gate insulator film (16) of the same thickness as that of the first MOSFET (12),

characterized in

that the source/drain region (24) of the first MOSFET (12) includes a first semiconductor region (27) of high impurity concentration and a second semiconductor region (26) which has a lower impurity concentration, and is formed closer to the channel, than the first semiconductor region (27), and

that the source/drain region (18) of the second MOSFET (11) includes a third semiconductor region (20) being in contact with with the substrate (10) and having a higher impurity concentration than the second semiconductor region (26) of the first MOSFET (12).

2. The device of claim 1, wherein said first and second MOSFETs (12, 11) are N-channel MOSFETs, and said first, second and third semiconductor regions (27, 26, 20) respectively include arsenic, phosphorus and phosphorus as impurities.

3. The device of claim 1 or 2, further comprising a third MOSFET (13) formed on said semiconductor substrate (10) and being of a conductivity type opposite to that of the first and second MOSFETs (12,11).

4. The device of any of claims 1 to 3, wherein the impurity concentration of said third semiconductor region (20) is at least $1 \times 10^{19}/cm^3$.

5. The device of many of claims 1 to 4, further comprising side wall spacers (25, 22, 30) which are formed on two side walls of each of the gate electrodes (23, 17, 28) of said first, second and third MOSFETs (12, 11, 13),

wherein said first semiconductor region (27) is defined by said gate electrode (23) of said first MOSFET (12) and said side wall

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spacers (25), and said second semiconductor region (26) is defined by said gate electrode (23) of said first MOSFET (12).

6. The device of claim 1, wherein the source/drain region (18) of the second MOSFET (11) includes at least one further semiconductor region (19, 21) having a lower impurity concentration than the third semiconductor region (20).

7. A method of manufacturing a semiconductor integrated circuit device which has first and second MOSFETs (12, 11) formed on a semiconductor substrate (10) and forming part of an internal circuit and an input/output circuit, respectively, comprising:

forming gate electrodes (23, 17) of said first and second MOSFETs (12, 11) on said semiconductor substrate (10),

introducing an impurity of the first conductivity type at a low concentration into at least a region to form said first MOSFET (12), by employing said gate electrodes (23, 17) as a mask, whereby second semiconductor regions (19, 26) are formed,

forming side wall spacers (25, 22) on two side walls of each of said gate electrodes (23, 17) of said first and second MOSFETs (12, 11),

introducing an impurity of the first conductivity type into a region to form said second MOSFET (11), by employing said gate electrode (17) of said second MOSFET (11) and said side wall spacers (22) thereof as a mask, whereby third semiconductor regions (20) as source and drain regions (18) of said second MOSFET (11) are formed, the impurity concentration of said third semiconductor regions (20) being higher than that of said second semiconductor regions (19), and

introducing an impurity of the first conductivity type into at least said region to form said first MOSFET (12), by employing said gate electrode (23) and said side wall spacers (25) as a mask, whereby first semiconductor regions (27) are formed, the impurity concentration of said first semiconductor regions (27) being higher than that of said second semiconductor regions (26), a source or drain region (24) of said first MOSFET (11) being made of said second and first semiconductor regions (26, 27).

8. The method of claim 7, wherein said first and second MOSFETs (12, 11) are N-channel MOSFETs, and said first, second and third semiconductor regions (27,26,20) are respectively formed by introducing arsenic phosphorus, and phosphorus.

9. The method of claim 7 or 8, wherein said first semiconductor regions (27) are formed in only said first MOSFET (12).

10. The method of any of claims 7 to 9, wherein a resistor (R) is formed one end of which is connected to said source or drain region (18) of said second MOSFET (11), said resistor (R) being made of a semiconductor region which is formed by the same step as that of said third semiconductor region (20), the other end of said resistor (R) being connected to a bonding pad (BP).

Revendications

1. Dispositif à circuits intégrés à semiconducteurs comprenant

un premier transistor MOSFET (12) faisant partie d'un circuit interne (1), et

un second transistor MOSFET (11) faisant partie d'un circuit d'entrée/sortie (2), le second transistor MOSFET (11) étant formé sur le même substrat semiconducteur (10) et possédant le même type de conductivité que le premier transistor MOSFET (12) et comportant une région de source/drain (18) qui est raccordée à un plot de liaison, et une pellicule d'isolant de grille (16) possédant la même épaisseur que celle du premier transistor MOSFET (12),

caractérisé en ce

que la région de source/drain (24) du premier transistor MOSFET (12) comprend une première région semiconductrice (27) possédant une concentration élevée en impuretés et une seconde région semiconductrice (26), qui possède une concentration inférieure en impuretés et est formée dans une position plus proche du canal, que ne l'est la première région semiconductrice (27), et

que la région de source/drain (18) du second transistor MOSFET (11) comprend une troisième région semiconductrice (20) qui est en contact avec le substrat (10) et possède une concentration en impuretés plus élevée que la seconde région semiconductrice (26) du premier transistor MOSFET (12).

2. Dispositif selon la revendication 1, dans lequel lesdits premier et second transistors MOSFET (12,11) sont des transistors MOSFET à canal N et que lesdites première, seconde et troisiè-

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me régions semiconductrices (27,26,20) comprennent respectivement, comme impuretés, de l'arsenic, du phosphore et du phosphore.

3. Dispositif selon la revendication 1 ou 2, comprenant en outre un troisième transistor MOSFET (13) formé sur ledit substrat semiconducteur (10) et possédant un type de conductivité opposé à celui des premier et second transistors MOSFET (12,11).

4. Dispositif selon l'une quelconque des revendications 1 à 3, dans lequel la concentration en impuretés de ladite troisième région semiconductrice (20) est égale à au moins 1 x $10^{19}/cm^3$.

5. Dispositif selon l'une quelconque des revendications 1 à 4, comportant en outre des entretoises de parois latérales (25,22,30), qui sont formées sur deux parois latérales de chacune des électrodes de grille (23,17,28) desdits premier, second et troisième transistors MOSFET (12,11,13),

dans lequel ladite première région semiconductrice (27) est définie par ladite électrode de grille (23) dudit premier transistor MOSFET (12) et par lesdites entretoises (25) des parois latérales, et ladite seconde région semiconductrice (26) est définie par ladite électrode de grille (23) dudit premier transistor MOSFET (12).

6. Dispositif selon la revendication 1, dans lequel la région de source/drain (18) du second transistor MOSFET (11) comprend au moins une autre région semiconductrice (19,21) qui possède une concentration en impuretés inférieure à celle de la troisième région semiconductrice (20).

7. Procédé de fabrication d'un dispositif à circuits intégrés à semiconducteurs, qui possède des premier et second transistors MOSFET (12,11) formés sur un substrat semiconducteur (10) et faisant partie respectivement d'un circuit interne et d'un circuit d'entrée/sortie, comprenant :

la formation d'électrodes de grille (23,17) desdits premier et second transistors MOSFET (12,11) sur ledit substrat semiconducteur (10),

l'introduction d'une impureté possédant le premier type de conductivité en une faible concentration dans au moins une région pour former ledit transistor MOSFET (12), moyennant l'utilisation desdites électrodes de grille (23,17) en tant que masque, ce qui permet de former des secondes régions semiconductrices (19,26),

la formation d'entretoises (25,22) sur deux parois latérales de chacune desdites électrodes de grille (23,17) desdits premier et second transistors MOSFET (10,11),

l'introduction d'une impureté possédant le premier type de conductivité dans une région pour former ledit second transistor MOSFET (11), moyennant l'utilisation de ladite électrode de grille (17) dudit second transistor MOSFET (11) et desdites entretoises (22) des parois latérales de cette électrode en tant que masque, ce qui permet de former des troisièmes régions semiconductrices (20) en tant que régions de source et de drain (18) dudit second transistor MOSFET (11), la concentration en impuretés desdites troisièmes régions semiconductrices (20) étant supérieure à celle desdites secondes régions semiconductrices (19), et

l'introduction d'une impureté possédant le premier type de conductivité dans au moins ladite région pour former ledit premier transistor MOSFET (12), moyennant l'utilisation de ladite électrode de grille (23) et desdites entretoises (25) des parois latérales en tant que masque, ce qui permet de former des premières régions semiconductrices (27), la concentration en impuretés desdites premières régions semiconductrices (27) étant supérieure à celle desdites secondes régions semiconductrices (26), une région de source ou de drain (24) dudit premier transistor MOSFET (12) étant formée par lesdites seconde et première régions semiconductrices (26,27).

8. Procédé selon la revendication 7, selon lequel lesdits premier et second transistors MOSFET (12,11) sont des transistors MOSFET à canal N, et lesdites première, seconde et troisième régions semiconductrices (27,26,20) sont formées respectivement par introduction d'arsenic, de phosphore, et de phosphore.

9. Procédé selon la revendication 7 ou 8, selon lequel lesdites premières régions semiconductrices (27) sont formées uniquement dans ledit premier transistor MOSFET (12).

10. Procédé selon l'une quelconque des revendications 7 à 9, selon lequel on forme une résistance (R), dont une extrémité est raccordée à ladite région de source ou de drain (18) dudit second transistor MOSFET (11), ladite résistance (R) étant formée d'une région semiconductrice qui est réalisée au moyen de la même étape que l'étape de formation de ladite

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troisième région semiconductrice (20), l'autre extrémité de ladite résistance (R) étant raccordée à un plot de liaison (BP).

Patentansprüche

1. Integrierte Halbleiterschaltung mit
einem ersten MOSFET (12), der Teil einer internen Schaltung (1) ist, und
einem zweiten MOSFET (11), der Teil einer Eingangs-/Ausgangsschaltung (2) ist und den gleichen Leitfähigkeitstyp aufweist sowie auf dem gleichen Halbleitersubstrat (10) gebildet ist wie der erste MOSFET (12), und mit einem mit einem Bonding-Anschluß verbundenen Source/Drain-Gebiet (18) sowie einem Gate-Isolationsfilm (16) der gleichen Dicke wie derjenige des ersten MOSFETs (12) versehen ist,
dadurch gekennzeichnet, daß das Source/Drain-Gebiet (24) des ersten MOSFETs (12) ein erstes Halbleitergebiet (27) hoher Störstellenkonzentration und ein weiteres Halbleitergebiet (26), das eine niedrigere Störstellenkonzentration aufweist und dichter am Kanal gebildet ist als das erste Halbleitergebiet (27), umfaßt, und
daß das Source-Drain-Gebiet (18) des zweiten MOSFETs (11) ein drittes Halbleitergebiet (20) umfaßt, das in Kontakt mit dem Substrat (10) steht und eine höhere Störstellenkonzentration als das zweite Halbleitergebiet (26) des ersten MOSFETs (12) aufweist.

2. Vorrichtung nach Anspruch 1, wobei der erste und der zweite MOSFET (12, 11) N-Kanal MOSFETs sind und das erste, das zweite und das dritte Halbleitergebiet (27, 26, 20) entsprechenderweise Arsen, Phosphor und Phosphor als Störstoffe enthalten.

3. Vorrichtung nach Anspruch 1 oder 2 mit einem auf dem Halbleitersubstrat (10) gebildeten dritten MOSFET (13), eines zum ersten und zweiten MOSFET (12, 11) entgegengesetzten Leitfähigkeitstyps.

4. Vorrichtung nach einem der Ansprüche 1 bis 3, wobei die Störstellenkonzentration des dritten Halbleitergebiets (20) mindestens 1 x $10^{19}/cm^3$ beträgt.

5. Vorrichtung nach einem der Ansprüche 1 bis 4, weiterhin umfassend:
Seitenwand-Abstandshalter (25, 22, 30), die an zwei Seitenwänden jeder der Gate-Elektroden (23, 17, 28) des ersten, zweiten und dritten MOSFETs (12, 11, 13) ausgebildet sind, wobei das erste Halbleitergebiet (27) durch die Gate-Elektrode (23) des ersten MOSFETs (12) und die genannten Seitenwand-Abstandshalter (25) definiert wird und das genannte zweite Halbleitergebiet (26) von der Gate-Elektrode (23) des ersten MOSFETs (12) definiert wird.

6. Vorrichtung nach Anspruch 1, wobei das Source/Drain-Gebiet (18) des zweiten MOSFETs (11) mindestens ein weiteres Halbleitergebiet (19, 21) mit einer niedrigeren Störstellenkonzentration als das dritte Halbleitergebiet (20) umfaßt.

7. Verfahren zur Herstellung einer integrierten Halbleiterschaltung mit einem ersten und einem zweiten MOSFET (12, 11), die auf dem Halbleitersubstrat (10) ausgebildet sind und entsprechenderweise einen Teil einer internen Schaltung und einer Eingangs/Ausgangsschaltung bilden, umfassend:
Bildung von Gate-Elektroden (23, 17) des ersten und zweiten MOSFETs (12, 11) auf dem Halbleitersubstrat (10),
Einbringen eines Störstoffs des ersten Leitfähigkeitstyps niedriger Konzentration in mindestens ein Gebiet, um den ersten MOSFET (12) zu bilden, indem die Gate-Elektroden (23, 17) als Maske verwendet werden, wodurch zweite Halbleitergebiete (19, 26) gebildet werden,
Bildung von Seitenwand-Abstandshaltern (25, 22) auf zwei Seitenwänden jeder der genannnten Gate-Elektroden (23, 17) des ersten und zweiten MOSFETs (12, 11),
Einbringen eines Störstoffs des ersten Leitfähigkeitstyps in ein Gebiet, um den zweiten MOSFET (11) zu bilden, indem die Gate-Elektrode (17) des zweiten MOSFETs (11) und deren genannte Seitenwand-Abstandshalter (22) als Maske verwendet werden, wodurch dritte Halbleitergebiete (20) als Source- und Drain-Gebiete (18) des zweiten MOSFETs (11) gebildet werden, wobei die Störstellenkonzentration der dritten Halbleitergebiete (20) höher als die der zweiten Halbleitergebiete (19) ist, und
Einbringen eines Störstoffs des ersten Leitfähigkeitstyps in mindestens das zur Bildung des ersten MOSFETs (12) vorgesehene Gebiet, indem die genannte Gate-Elektrode (23) und die Seitenwand-Abstandshalter (25) als Maske verwendet werden, wodurch erste Halbleitergebiete (27) gebildet werden, wobei die Störstellenkonzentration der ersten Halbleitergebiete (27) höher als die der zweiten

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Halbleitergebiete (26) ist und das Source- oder Drain-Gebiet (24) des zweiten MOSFETs (11) aus den zweiten und ersten Halbleitergebieten (26, 27) gebildet ist.

8. Verfahren nach Anspruch 7, wobei die ersten und zweiten MOSFETs (12, 11) N-Kanal MOSFETs sind und das genannte erste, das zweite und das dritte Halbleitergebiet (27, 26, 20) entsprechenderweise durch Einbringen von Arsen, Phosphor und Phosphor gebildet werden.

9. Verfahren nach Anspruch 7 oder 8, wobei die ersten Halbleitergebiete (27) lediglich im ersten MOSFET (12) gebildet werden.

10. Verfahren nach einem der Ansprüche 7 bis 9, wobei ein Widerstand R gebildet wird, dessen eines Ende mit dem Source- oder Drain-Gebiet (18) des zweiten MOSFETs (11) und dessen anderes Ende mit einem Bonding-Anschluß (BP) verbunden ist, wobei der Widerstand von einem im gleichen Schritt wie das dritte Halbleitergebiet (20) hergestellten Halbleitergebiet gebildet wird.

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