

SEMICONDUCTOR DEVICE, OPTICAL DEVICE, AND MANUFACTURING METHOD FOR SEMICONDUCTOR STRUCTURE

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TECHNICAL FIELD

[0001] The present disclosure belongs to the field of semiconductor technology, and particularly relates to a semiconductor device, an optical device, and a manufacturing method for a semiconductor structure.

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BACKGROUND

[0002] With continuous advance of Moore's law, after semiconductor processes develop to 3nm node, a Gate All Around (GAA) transistor is considered to be an effective substitute for a Fin Field-Effect Transistor (FinFET). Horizontally stacked nanosheets with sacrificial layers etched with a high selectivity ratio are important in a GAA manufacturing process. In the industry, vertically stacked Si nanosheets are generally formed by selectively removing SiGe from a Si-SiGe multilayer stack, so as to form an n-type GAA-FET.

[0003] However, due to a large difference between a lattice constant of Si and that of SiGe, as the number of stacked layers of Si layers and SiGe layers increases, internal stress of the Si layers and the SiGe layers continuously accumulates. When the number of stacked layers of the Si layers and the SiGe layers are increased to a certain level, the accumulation of the internal stress may cause wafer warpage, and in severe cases, may even cause wafer cracking. Thus, the number of stacked layers of the Si layers and the SiGe layers is limited. In addition, due to the lattice mismatch between the Si layers and the SiGe layers, a dislocation defect of the Si layers epitaxially grown on the SiGe layers is increased. Since the Si layers serve as channels of a GAA-FET, the dislocation defect in the Si layers may reduce performance of the GAA-FET.

SUMMARY

[0004] Embodiments of the present disclosure disclose a semiconductor device, an optical device, and a manufacturing method for a semiconductor structure, so as to solve the problems in the related technology that the number of stacked layers is small and the dislocation defect can be easily caused.

[0005] In order to solve the above technical problems, in a first aspect, an embodiment of the present disclosure discloses a manufacturing method for a semiconductor structure, including: forming a stacked structure on a substrate, the stacked structure including a functional layer and a sacrificial layer which are alternately stacked, the functional layer and the sacrificial layer being made of a same material, the sacrificial layer being doped with n-type or p-type impurities, and a doping concentration of the sacrificial layer being greater than a doping concentration of the functional layer; and selectively removing the sacrificial layer from the stacked structure.

[0006] In some implementations, a plurality of functional layers and a plurality of sacrificial layers are provided, and at least part of at least one of the functional layers is curved or kinked; and/or at least part of at least one of the sacrificial layers is curved or kinked.

[0007] In some implementations, the substrate includes a flat surface, and the stacked structure is formed on the flat surface; or the substrate includes a wavy surface, and the stacked structure is adaptively formed on the wavy surface; or the substrate includes a protrusion structure protruding from a surface of a substrate body, and the stacked structure is adaptively formed on the surface of the substrate body and a surface of the protrusion structure.

[0008] In some implementations, the protrusion structure includes: a first protrusion, which is located on the substrate body; and a second protrusion, which is located on the first protrusion, a projection area of the second protrusion on a plane where the substrate body is located being greater than a projection area of the first protrusion on the plane where the substrate body is located, and a projection of the first protrusion on the plane where the substrate body is located being within a projection of the second protrusion on the plane where the substrate body is located.

[0009] In some implementations, selectively removing the sacrificial layer from the stacked structure includes: performing anisotropic etching on the stacked structure, and remaining a

part of the stacked structure just below the second protrusion; and selectively removing the sacrificial layer from the remaining part of the stacked structure.

[0010] In some implementations, the functional layer is an undoped layer; or the doping concentration of the functional layer is less than $5 \times 10^{14} \text{cm}^{-3}$; or the doping concentration of the sacrificial layer is greater than $5 \times 10^{14} \text{cm}^{-3}$; or the doping concentration of the sacrificial layer is $6 \times 10^{14} \text{cm}^{-3}$ to $5 \times 10^{21} \text{cm}^{-3}$.

[0011] In some implementations, forming the stacked structure on the substrate includes: alternately epitaxially growing the functional layer and the sacrificial layer on the substrate by a chemical vapor deposition process.

[0012] In some implementations, the material of the functional layer and the sacrificial layer is silicon; epitaxially growing the functional layer includes: introducing a silicon-containing gas into a process chamber; and epitaxially growing the sacrificial layer includes: introducing the silicon-containing gas and a gas containing impurity elements into the process chamber.

[0013] In some implementations, the silicon-containing gas includes at least one of SiH_4 , Si_2H_6 , or SiH_2Cl_2 ; and the gas containing the impurity elements includes B_2H_6 , or the gas containing the impurity elements includes at least one of PH_3 , AsH_3 , SbH_3 , or BiH_3 .

[0014] In some implementations, a temperature for epitaxial growth is 400°C to 750°C .

[0015] In some implementations, selectively removing the sacrificial layer from the stacked structure includes: performing isotropic plasma etching on the stacked structure with a process gas.

[0016] In some implementations, the material of the functional layer and the sacrificial layer is silicon; and the process gas includes at least one of a chlorine-containing gas or a bromine-containing gas.

[0017] In some implementations, the chlorine-containing gas includes at least one of Cl_2 or HCl ; the bromine-containing gas includes at least one of Br_2 or HBr ; and the process gas further includes at least one of N_2 , He , or Ar .

[0018] In some implementations, after selectively removing the sacrificial layer from the stacked structure, the manufacturing method further includes: performing oxidation treatment on the functional layer; and removing an oxide layer from a surface of the functional layer.

[0019] In a second aspect, an embodiment of the present disclosure discloses a semiconductor device, including: a substrate; at least one functional layer, which is

disposed on the substrate, the at least one functional layer being disposed at intervals in a vertical direction, and at least part of at least one of functional layers being curved or kinked; a gate structure, which is disposed around each of the at least one functional layer; and source/drain regions, which are respectively disposed on two sides of the at least one functional layer and are connected to the at least one functional layer.

[0020] In a third aspect, an embodiment of the present disclosure discloses a semiconductor device, including: a substrate; at least one functional layer, which is disposed on the substrate, the at least one functional layer being disposed at intervals in a vertical direction and manufactured with the manufacturing method for a semiconductor structure described in the first aspect; a gate structure, which is disposed around each of the at least one functional layer; and source/drain regions, which are respectively disposed on two sides of the at least one functional layer and are connected to the at least one functional layer.

[0021] In a fourth aspect, an embodiment of the present disclosure discloses an optical device, including: at least one functional layer, which is configured to transmit optical signals, the at least one functional layer being manufactured with the manufacturing method for a semiconductor structure described in the first aspect.

[0022] In the semiconductor device, the optical device, and the manufacturing method for a semiconductor structure according to the embodiments of the present disclosure, the functional layer and the sacrificial layer are made of the same material, only the doping concentrations are different, and there is almost no lattice constant difference between the functional layer and the sacrificial layer. Thus, stress accumulation caused by lattice mismatch does not occur at an interface between the functional layer and the sacrificial layer, and the dislocation defect is not introduced into the functional layer. Moreover, compared with the related technology adopting the gradual changed sacrificial layer, the sacrificial layer provided in the embodiment of the present disclosure can be made very thin, resulting in simple process, large number of stacked layers, and high production capacity. The number of stacked layers of the stacked structure provided in the embodiment of the present disclosure can be more than a hundred, without causing wafer warpage or wafer cracking.

BRIEF DESCRIPTION OF DRAWINGS

[0023] FIG. 1 is a schematic diagram of a Si/SiGe stacked structure in the related technology;

[0024] FIG. 2 is a flowchart illustrating a manufacturing method for a semiconductor structure according to an embodiment of the present disclosure;

[0025] FIG. 3 is another flowchart illustrating a manufacturing method for a semiconductor structure according to an embodiment of the present disclosure;

[0026] FIG. 4 to FIG. 10 are schematic structural diagrams respectively illustrating steps of a manufacturing method for a semiconductor structure according to an embodiment of the present disclosure;

[0027] FIG. 11 is a schematic diagram of lattices of a SiGe material;

[0028] FIG. 12 is a schematic diagram of lattices of a P-doped Si material;

[0029] FIG. 13 and FIG. 14 are schematic structural diagrams illustrating steps of a manufacturing method for a semiconductor structure according to an example of an embodiment of the present disclosure;

[0030] FIG. 15 and FIG. 16 are schematic structural diagrams illustrating steps of a manufacturing method for a semiconductor structure according to an example of an embodiment of the present disclosure;

[0031] FIG. 17 is a schematic diagram illustrating other examples of a protrusion structure according to an embodiment of the present disclosure;

[0032] FIG. 18 to FIG. 20 are schematic structural diagrams illustrating steps of a manufacturing method for a semiconductor structure according to an example of an embodiment of the present disclosure; and

[0033] FIG. 21 is a schematic diagram of a semiconductor device according to an embodiment of the present disclosure.

DETAIL DESCRIPTION OF EMBODIMENTS

[0034] In order to make the objective, technical solutions and advantages of the present disclosure clearer, the technical solutions in the embodiments of the present disclosure will be clearly and thoroughly described below with reference to the drawings for the embodiments of the present disclosure. Apparently, the embodiments described herein are

only part of the embodiments of the present disclosure, but are not all the embodiments. All other embodiments derived by those of ordinary skill in the art from the embodiments described herein without inventive work fall within the scope of the present disclosure.

[0035] It should be understood by those of ordinary skill in the art that the embodiments of the present disclosure are just an explanation of the structure and method which are claimed by the present disclosure and can be embodied in various forms. Further, each example given in connection with each embodiment is for the purpose of illustration, rather than for the purpose of limitation. Further, the drawings are not necessarily drawn to scale, some features may be exaggerated to show details of particular components. Therefore, the specific structural and functional details in the embodiments of the present disclosure should not be interpreted as being for the purpose of limitation, and are just representative bases for teaching those of ordinary skill in the art to adopt the method and structure according to the embodiments of the present disclosure in various ways. It should be further noted that the same elements and the corresponding elements are referred to by the same reference numerals.

[0036] In the following description, many specific details such as particular structures, components, materials, dimensions, processing steps, and techniques are described, so as to provide understanding of each embodiment of the present disclosure. However, it should be understood by those of ordinary skill in the art that each embodiment of the present disclosure may be practiced without these specific details. In other cases, well-known structures or processing steps are not described in detail for avoiding obscuring the present disclosure.

[0037] For the purpose of description, the terms “on”, “right”, “left”, “vertical”, “horizontal”, “top”, “bottom” and the derivative terms thereof relate to the orientations of the structure and method disclosed in the drawings of the specification. It should be understood that when an element as a layer, region or substrate is referred to as being “on” the other element, the element may be directly on the other element, or an intermediate element may be present. In contrast, when an element is referred to as being “directly on” the other element, there is no intermediate element between the two elements. It should be further understood that when an element is referred to as being “under” the other element, the element may be directly under the other element, or an intermediate element may be present. In contrast, when an element is referred to as being “directly under” the element, there is no intermediate element between the two elements.

[0038] As described above, due to the lattice mismatch between the Si layers and the SiGe layers, on the one hand, the number of stacked layers of the Si layers and the SiGe layers is limited; on the other hand, the dislocation defect is introduced into the Si layers, resulting in poor performance of the manufactured GAA-FET. In order to solve the above technical problems, a technical solution is provided in the related technology. As shown in FIG. 1, according to the technical solution, when a SiGe layer 2 is epitaxially grown on a surface of a substrate 1, a Ge concentration in the SiGe layer 2 needs to be gradually changed, that is, the Ge concentration is gradually increased as a growth thickness of the SiGe layer 2 increases, and then the Ge concentration is gradually decreased as the growth thickness of the SiGe layer 2 continues to increase. Thus, lattice constants of two sides of the SiGe layer 2 that are in contact with a Si layer 3 are close to a lattice constant of the Si layer 3, so as to avoid or reduce the stress between the Si layers and the SiGe layers and the dislocation defect in the Si layers which are caused by the lattice mismatch. However, on the one hand, this solution requires continuous adjustment of the Ge concentration during the epitaxial growth of the SiGe layer 2, resulting in high process complexity and high manufacturing cost; on the other hand, the SiGe layer 2 is required to be relatively thick to produce a gradual buffer effect, resulting in small number of stacked layers and low production capacity.

[0039] In order to solve the above technical problems, an embodiment of the present disclosure provides a manufacturing method for a semiconductor structure, which may include the following steps, as shown in FIG. 2.

[0040] At S110, a stacked structure is formed on a substrate.

[0041] As shown in FIG. 4 which is a top view of a semiconductor structure according to an embodiment of the present disclosure and FIG. 5 which is a schematic cross-sectional view taken along line A-A of FIG. 4, a stacked structure 200 is formed on a substrate 100, and includes functional layers 201 and sacrificial layers 202 which are alternately stacked. The functional layers 201 are configured to perform a function of the semiconductor structure. For example, in a case where the semiconductor structure is used for a GAA-FET, the functional layers 201 serve as channels of the GAA-FET, and the sacrificial layers 202 are removed in a subsequent process. It should be understood by those of ordinary skill in the art that the present disclosure is not limited thereto, and the functional layers 201 may perform other functions in different application scenarios, such as functioning as a waveguide in an active or passive optical device.

[0042] The functional layers 201 and the sacrificial layers 202 are made of a same material, such as Si. It should be understood by those of ordinary skill in the art that the functional layers 201 and the sacrificial layers 202 may be made of other materials, such as Ge, SiGe, GaAs, InSb, GaP, GaN, GaSb, InAlAs, InGaAs, GaSbP, GaAsSb, or InP. It should be noted that in a case where the functional layers 201 and the sacrificial layers 202 are made of compound materials, the “same material” in the embodiment of the present disclosure refers to that elements contained in the compound materials are the same in kind and proportion, and the compound materials only differ in doping concentration. In the prior art, n-type or p-type impurities are well-defined, and doping a semiconductor material with a small amount of n-type or p-type impurities does not change composition of host elements of the semiconductor material, and generally aims to change a concentration of free electrons or free holes in the semiconductor material to change electrical properties of the semiconductor material. It should be understood by those of ordinary skill in the art that since doping concentrations in conventional semiconductor doping processes are extremely minute relative to contents of the host elements, the lattice constants of the functional layers 201 and the sacrificial layers 202 can be hardly changed by different doping concentrations, and the “same material” having different doping concentrations makes the lattice constant of the functional layers 201 almost identical with that of the sacrificial layers 202. For example, if the functional layers 201 and the sacrificial layers 202 are both made of Si_xGe_y , the “same material” in the embodiment of the present disclosure refers to that Si and Ge are the same in proportion for the functional layers 201 and the sacrificial layers 202, that is, values of x are the same, and values of y are the same, and only the doping concentrations are different. If the elements in the compound materials are different in proportion for the functional layers 201 and the sacrificial layers 202, a large difference between the lattice constants of the functional layers 201 and the sacrificial layers 202 is caused even if the elements in the compound material of the functional layers 201 and the elements in the compound material of the sacrificial layers 202 are the same in kind. Therefore, in a case where the elements in the compound material of the functional layers 201 and the elements in the compound material of the sacrificial layers 202 are different in proportion, the technical problems of the stress between the Si layers and the SiGe layers and the dislocation defect in the Si layers caused by the lattice mismatch in the related technology cannot be solved. It should be understood by those of ordinary skill in the art that if the constituent elements in the compound materials are the same in kind but different

in proportion, and the compound materials should not be considered as the “same material” described in the embodiment of the present disclosure. In some implementations of the embodiment of the present disclosure, the sacrificial layers 202 may be doped with n-type or p-type impurities, and the functional layers 201 may not be doped, for example, the functional layers 201 is an intrinsic semiconductor, in which case a doping concentration of the sacrificial layers 202 is necessarily greater than that of the functional layers 201 (that is, the functional layers 201 are not doped). In other implementations of the embodiment of the present disclosure, the functional layers 201 may be doped, for example, the functional layers 201 is doped with n-type or p-type impurities, in which case the doping concentration of the sacrificial layers 202 is greater than that of the functional layers 201.

[0043] In some implementations of the embodiment of the present disclosure, the functional layers 201 may be undoped layers or lightly-doped layers, and the sacrificial layers 202 may be heavily-doped layers. Due to a difference between the doping concentrations of the functional layers 201 and the sacrificial layers 202, the sacrificial layers 202 can be selectively etched from the stacked structure 200 in a subsequent etching process. In some implementations, the functional layers 201 may be made of an intrinsic semiconductor material or the doping concentration of the functional layers 201 may be less than $5 \times 10^{14} \text{cm}^{-3}$, and the doping concentration of the sacrificial layers 202 may be greater than $5 \times 10^{14} \text{cm}^{-3}$. It has been found in the present disclosure that the doping concentration of $5 \times 10^{14} \text{cm}^{-3}$ is a cut-off point. Taking an n-type doped Si material as an example, a doped layer with a doping concentration greater than $5 \times 10^{14} \text{cm}^{-3}$ has a higher etch selectivity ratio relative to a doped layer with a doping concentration less than $5 \times 10^{14} \text{cm}^{-3}$ or an undoped layer. Further, the doping concentration of the sacrificial layers 202 should not be too high because an excessive doping concentration of the sacrificial layers 202 may cause an increase of the difference between the lattice constants of the functional layers 201 and the sacrificial layers 202. In some implementations, the doping concentration of the sacrificial layers 202 is $6 \times 10^{14} \text{cm}^{-3}$ to $5 \times 10^{21} \text{cm}^{-3}$, and in an embodiment, the doping concentration of the sacrificial layers 202 is $1 \times 10^{15} \text{cm}^{-3}$ to $5 \times 10^{21} \text{cm}^{-3}$.

[0044] The substrate 100 includes a single-crystal semiconductor layer at least disposed on a surface thereof. The substrate 100 may include a single-crystal semiconductor material such as, but not limited to, Si, Ge, SiGe, GaAs, InSb, GaP, GaN, GaSb, InAlAs, InGaAs, GaSbP, GaAsSb, and InP. In some implementations, the substrate 100 may be made of crystalline Si. Other layers may be provided between the substrate 100 and the stacked

structure 200. A material of the substrate 100 may be the same as or different from that of the functional layers 201 or the sacrificial layers 202. In a case where the material of the substrate 100 is different from that of the functional layers 201 or the sacrificial layers 202, a buffer layer may be further provided between the substrate 100 and the stacked structure 200, and may be configured to gradually change a lattice constant from a lattice constant of the substrate 100 to the lattice constant of the functional layers 201 or the sacrificial layers 202.

[0045] In the related technology, a Ge content in the SiGe layers is on the order of 20% to 50%, as shown in FIG. 11, resulting in the large difference between the lattice constant of SiGe and that of Si. Therefore, the internal stress of the Si layers and the SiGe layers continuously accumulates as the number of stacked layers of the Si layers and the SiGe layers is increased; when the number of stacked layers of the Si layer and the SiGe layer reaches a certain level, the accumulation of the internal stress may cause wafer warpage, and in severe cases, may even cause wafer cracking. Thus, the number of stacked layers of the Si layers and the SiGe layers is limited. In the embodiment of the present disclosure, the functional layers 201 and the sacrificial layers 202 are made of the same material, only the doping concentrations are different, and the difference between the lattice constants of the functional layers 201 and the sacrificial layers 202 is very small. Taking the functional layers 201 and the sacrificial layers 202 being made of a Si material as an example, when a Group V element such as P is doped into the sacrificial layers 202, and P atoms replace a small number of Si atoms in the Si crystal and occupy positions of the Si atoms in the lattice. Since the doping concentrations in the conventional semiconductor doping processes are extremely minute relative to the Ge content in the SiGe layers, as shown in FIG. 12, the lattice constant of the sacrificial layers 202 can be hardly changed, and the lattice constant of the functional layers 201 is almost identical with that of the sacrificial layers 202. Thus, stress accumulation caused by the lattice mismatch does not occur at interfaces between the functional layers 201 and the sacrificial layers 202, and the dislocation defect is not introduced into the functional layers 201. Compared with the related technology illustrated by FIG. 1, a thickness of the sacrificial layers 202 of the stacked structure provided in the embodiment of the present disclosure can be made very small, for example, the thickness of the sacrificial layers 202 of the stacked structure is identical with that of the functional layers, resulting in simple process, large number of stacked layers, and high production capacity. The number of stacked layers of the stacked

structure provided in the embodiment of the present disclosure can be more than a hundred, without causing wafer warpage or wafer cracking and introducing the dislocation defect caused by the lattice mismatch into the functional layers 201.

[0046] In some implementations of the embodiment of the present disclosure, step S110 may include: alternately epitaxially growing the functional layers 201 and the sacrificial layers 202 on the substrate 100 by a Chemical Vapor Deposition (CVD) process.

[0047] In an example illustrated by FIG. 5, a sacrificial layer 202 is epitaxially grown first on the substrate 100, and then a functional layer 201 is epitaxially grown. However, the present disclosure is not limited thereto, it may be the case that the functional layer 201 is epitaxially grown first and then the sacrificial layer 202 is epitaxially grown, and other layers may be provided between the functional layer 201 and the sacrificial layer 202.

[0048] Still taking the functional layers 201 and the sacrificial layers 202 being made of a Si material as an example, a step of epitaxially growing the functional layer 201 includes: introducing a silicon-containing gas into a process chamber; and a step of epitaxially growing the sacrificial layer 202 includes: introducing a silicon-containing gas and a gas containing impurity elements into the process chamber. Exemplarily, the process chamber is a CVD process chamber, and the silicon-containing gas may include at least one of SiH_4 , Si_2H_6 , or SiH_2Cl_2 . At the step of epitaxially growing the functional layer 201, the silicon-containing gas decomposes when heated, and Si atoms are deposited on the surface of the substrate to form a film. At the step of epitaxially growing the sacrificial layer 202, the silicon-containing gas and the gas containing the impurity elements decompose when heated, and Si atoms and impurity atoms are deposited on the surface of the substrate to form a film, that is, a doped semiconductor layer is formed by in-situ doping. When n-type doping is needed, the gas containing the impurity elements may include, for example, at least one of PH_3 , AsH_3 , SbH_3 , or BiH_3 ; when p-type doping is needed, the gas containing the impurity elements may include, for example, B_2H_6 . In some implementations, the sacrificial layers 202 are doped with an impurity element having a high atomic weight, such as As, Sb, and/or Bi. Accordingly, the gas containing the impurity elements used at the step of epitaxially growing the sacrificial layer 202 may include AsH_3 , SbH_3 , and/or BiH_3 . The impurity element having the high atomic weight is more difficult to diffuse to the functional layer, which may avoid reduction of the difference between the doping concentrations of the sacrificial layers 202 and the functional layers 201, and improve an etch selectivity ratio of the sacrificial layers 202 relative to the functional layers 201.

[0049] In some implementations of the embodiment of the present disclosure, a temperature for epitaxial growth is 400°C to 750°C. The temperature for epitaxial growth should not be too high because an excessive temperature for epitaxial growth may cause part of the impurity atoms in the sacrificial layers 202 to diffuse into the functional layers 201, such that the difference between the doping concentrations of the sacrificial layers 202 and the functional layers 201 is reduced, and the etch selectivity ratio of the sacrificial layers 202 relative to the functional layers 201 is reduced in a subsequent selective etching process.

[0050] At S120, the sacrificial layers are selectively removed from the stacked structure.

[0051] As shown in FIG. 9 which is a schematic cross-sectional view taken along line A-A of FIG. 4, the sacrificial layers 202 are selectively removed from the stacked structure 200, and only the functional layers 201 remain. In some implementations of the embodiment of the present disclosure, the functional layers 201, for example, may serve as channels of a GAA-FET, and a gate structure is formed around the functional layers 201 in a subsequent process.

[0052] In some implementations of the embodiment of the present disclosure, as shown in FIG. 3, after step S110 and before step S120, the method may further include the following steps.

[0053] At S111, the sacrificial layers 202 are removed by a predetermined thickness.

[0054] As shown in FIG. 6 which is a schematic cross-sectional view taken along line B-B of FIG. 4, the sacrificial layers 202 are removed on both sides by the predetermined thickness along a direction of line B-B, and the predetermined thickness is about 3 nm to 10 nm, and in an embodiment, the predetermined thickness is about 5 nm.

[0055] At S112, the space formed after the sacrificial layers 202 are removed by the predetermined thickness is filled with an insulating layer 203.

[0056] As shown in FIG. 7, the insulating layer 203, for example, may be made of silicon nitride, may be formed by an Atomic Layer Deposition (ALD) process, and may be configured to prevent a subsequently formed gate structure from being conductive to a source region or a drain region.

[0057] At S113, an epitaxial layer 204 is epitaxially grown on side surfaces of the functional layers 201.

[0058] As shown in FIG. 8, the epitaxial layer 204, for example, may serve as a source region and a drain region of a GAA-FET. Due to the support of the epitaxial layer 204, after

the sacrificial layers 202 are removed, a plurality of functional layers 201 spaced apart from each other may be formed as shown in FIG. 9.

[0059] In some implementations of the embodiment of the present disclosure, step S120 may include: performing isotropic plasma etching on the stacked structure 200 with a process gas.

[0060] Since the sacrificial layers 202 needs to be subjected to lateral etching, isotropic plasma etching needs to be adopted. During the etching, a lower electrode power of the process chamber is 0, or a low lower electrode power is applied.

[0061] In order to improve the etch selectivity ratio of the sacrificial layers 202 relative to the functional layers 201 to completely remove the sacrificial layers 202 under the condition that the functional layers 201 are not damaged or just slightly damaged, it has been found in the present disclosure through research that using a chlorine-containing gas and/or a bromine-containing gas as a primary etching gas may endow the heavily-doped sacrificial layers 202 with good selectivity, the chlorine-containing gas may include, for example, at least one of Cl_2 or HCl , and the bromine-containing gas may include, for example, at least one of Br_2 or HBr . In order to further improve etching morphology, the process gas may further include an auxiliary etching gas, which may include at least one of N_2 , He , or Ar . Further, a flow ratio of the auxiliary etching gas to the primary etching gas may be 3 to 2500 in the process gas, a flow rate of the primary etching gas may be 20 sccm to 1000 sccm, and a flow rate of the auxiliary etching gas may be 3 slm to 50 slm. Through tests, by adopting the isotropic plasma etching provided in the embodiment of the present disclosure, lateral etching on the order of tens of micrometers and a high etch selectivity ratio can be achieved.

[0062] In some implementations of the embodiment of the present disclosure, after step S120, the method may further include the following steps.

[0063] At S121, oxidation treatment is performed on the functional layers 201.

[0064] The functional layers 201 may have residual impurity elements due to various factors, for example, part of the impurity atoms in the heavily-doped sacrificial layers 202 may diffuse into the functional layers 201 in the process of forming the functional layers 201 by epitaxial growth, or a small amount of the sacrificial layers 202 may remain on surfaces of the functional layers 201 after the selective etching of the sacrificial layers 202 at step S120 is completed. In some application scenarios, the impurity elements remaining in the functional layers 201 may have an adverse effect, for example, the residual impurity

elements may make it hard to completely shut down the channels when the functional layers 201 serve as the channels of the GAA-FET. In order to remove the residual impurity elements, the functional layers 201 may be subjected to oxidation treatment to form oxide layers on the surfaces of the functional layers 201. In a case where the functional layers 201 are made of a Si material, the oxide layers, for example, may be silicon oxide layers. The oxide layers can enable the impurity atoms near the surfaces of the functional layers 201 to be enriched in the oxide layers.

[0065] At S122, the oxide layers are removed from the surfaces of the functional layers 201.

[0066] Since the impurity elements are enriched in the oxide layers, the residual impurity elements in the functional layers 201 can be removed after removing the oxide layers formed on the surfaces of the functional layers 201 by oxidation.

[0067] Through the above steps S121 and S122, not only can the residual impurity elements in the functional layers 201 be removed, but also the surfaces of the functional layers 201 can be made smooth. Since burrs protruding from the surfaces of the functional layers 201 can be easily oxidized, the burrs can be removed from the surfaces of the functional layers 201 after selectively removing the oxide layers from the surfaces of the functional layers, so as to further improve performance of a device manufactured subsequently. In some implementations, since the functional layers are also removed by a certain thickness at steps S121 and S122, the thickness of the functional layers may be slightly greater than a predetermined thickness in the process of epitaxially growing the functional layers, so that the thickness of the functional layers may be made to be exactly equal to the predetermined thickness after steps S121 and S122.

[0068] In order to form a semiconductor device, in some implementations of the embodiment of the present disclosure, after step S120, the method may further include:

[0069] At S130, a gate structure is formed around the functional layers.

[0070] As shown in FIG. 10, the gate structure is formed around the functional layers 201, so that the functional layers 201 may serve as channels of the semiconductor device, with the gate structure disposed around the channels. The gate structure may include gate dielectric layers 205 around the functional layers 201 and a gate electrode layer 206. The gate dielectric layer 205 may include, for example, one or more layers of a dielectric material such as HfO_2 and other high-k dielectric materials; and the gate electrode layer 206 may include one or more layers of a conductive material such as polysilicon, aluminum,

copper, titanium, tantalum, tungsten, cobalt, molybdenum, tantalum nitride, nickel silicide, cobalt silicide, TiN, WN, TiAl, TiAlN, TaCN, TaC, TaSiN, alloys thereof, other suitable materials, and/or combinations thereof.

[0071] Accordingly, in a case where the functional layers serve as the channels of the semiconductor device, an embodiment of the present disclosure further provides a semiconductor device. As shown in FIG. 3 to FIG. 10, the semiconductor device may include a substrate 100; at least one functional layer 201 disposed on the substrate 100, with the at least one functional layer 201 disposed at intervals in a vertical direction, and being manufactured with the above manufacturing method for a semiconductor structure; a gate structure disposed around each functional layer 201; and source/drain regions 204 respectively disposed on two sides of the functional layer 201 and connected to the functional layer 201. In an embodiment, a plurality of functional layers 201 are provided. Exemplarily, the semiconductor device may be a three-dimensional Dynamic Random Access Memory (3D DRAM).

[0072] In a case where the functional layers serve as a waveguide of an optical device, an embodiment of the present disclosure further provides an optical device, and the optical device includes at least one functional layer 201, which is configured to transmit optical signals and is manufactured with the above manufacturing method for a semiconductor structure. In an embodiment, a plurality of functional layers 201 are provided.

[0073] Since each layer in the stacked structure in the embodiment of the present disclosure is made of the same material, the difference between the lattice constants of the layers is extremely small, and stress accumulation does not occur in the process of epitaxial growth, so that there is no wafer warpage or wafer cracking caused by the stress accumulation, and the dislocation defect is not introduced into the functional layers. Therefore, the stacked structure provided in the embodiment of the present disclosure can be formed on a flat surface, and can also be adaptively formed on various complex surfaces to meet requirements of different application scenarios. In this case, at least part of at least one of the functional layers of the stacked structure is curved or kinked, and/or at least part of at least one of the sacrificial layers of the stacked structure is curved or kinked. The conventional Si/SiGe stacked structure cannot be made curved or kinked because a curved portion or a kinked portion may cause more stress. The curved or kinked stacked structure provided in the embodiment of the present disclosure will be illustrated in detail below by several examples, and it should be understood by those of ordinary skill in the art that the

following examples are not exhaustive. Since there is almost no lattice constant difference between the functional layers and the sacrificial layers of the stacked structure implemented in the present disclosure, those of ordinary skill in the art can design other curved or kinked stacked structures based on actual situations.

5 [0074] In an example of the embodiment of the present disclosure, as shown in FIG. 13 and FIG. 14, the substrate 110 includes a wavy surface. It should be understood by those of ordinary skill in the art that the substrate 110 does not need to have an entirely wavy surface, but may only have a partially wavy surface. The stacked structure 210 is adaptively formed on the wavy surface of the substrate 110, and includes the functional layers 211 and
10 the sacrificial layers 212 which are alternately stacked. Similarly, the functional layers 211 and the sacrificial layer s212 may be alternately epitaxially grown on the substrate 110 by a CVD process. After the sacrificial layers 212 are selectively removed from the stacked structure 210, a plurality of wavy functional layers 211 spaced apart from each other are formed as shown in FIG. 14. More details of the steps of forming the stacked structure on
15 the substrate and selectively removing the sacrificial layers from the stacked structure can be found in the corresponding description above, and will not be described here.

[0075] In another example of the embodiment of the present disclosure, as shown in FIG. 15 and FIG. 16, the substrate 120 includes a protrusion structure 122 protruding from a surface of a substrate body 121, the stacked structure 220 is adaptively formed on the
20 surface of the substrate body 121 and a surface of the protrusion structure 122, and includes the functional layers 221 and the sacrificial layers 222 which are alternately stacked, and a plurality of Ω -like functional layers 221 spaced apart from each other are formed as shown in FIG. 16 after selectively removing the sacrificial layers 222 from the stacked structure 220. In the example illustrated by FIG. 15 and FIG. 16, a cross section of the protrusion
25 structure 122 is rectangular, but the present disclosure is not limited thereto, and the protrusion structure may be in other shapes. As shown in FIG. 17, the protrusion structure may be a saw-tooth protrusion structure 123 or a trapezoidal protrusion structure 124. In the example illustrated by FIG. 15 and FIG. 16, a top surface and side surfaces of the protrusion structure 122 are all flat surfaces, but the present disclosure is not limited thereto.
30 All the surfaces of the protrusion structure may be curved surfaces, such as a protrusion structure 125 in FIG. 17; or part of the surfaces of the protrusion structure may be curved surfaces, such as a protrusion structure 126 in FIG. 17. It should be further understood by those of ordinary skill in the art that the upper surface of the substrate body 121 is not

limited to a flat surface, and may be a curved or kinked surface. More details of the steps of forming the stacked structure on the substrate and selectively removing the sacrificial layers from the stacked structure can be found in the corresponding description above, and will not be described here.

5 [0076] In still another example of the embodiment of the present disclosure, as shown in FIG. 18 to FIG. 20, a substrate 130 is provided with a protrusion structure protruding from a surface of a substrate body 131, the protrusion structure may include a first protrusion 132 and a second protrusion 133, the first protrusion 132 is located on the substrate body 131, the second protrusion 133 is located on the first protrusion 132, a projection area of
10 the second protrusion 133 on a plane where the substrate body 131 is located is greater than that of the first protrusion 132 on the plane where the substrate body 131 is located, and a projection of the first protrusion 132 on the plane where the substrate body 131 is located is within that of the second protrusion 133 on the plane where the substrate body 131 is located. A stacked structure 230 is adaptively formed on the surface of the substrate body
15 131 and a surface of the protrusion structure, and includes functional layers 231 and sacrificial layers 232 which are alternately stacked. More details of the step of forming the stacked structure on the substrate can be found in the corresponding description above, and will not be described here.

[0077] Further, a step of selectively removing the sacrificial layers 232 from the stacked
20 structure 230 may include the following steps.

[0078] At S120a, anisotropic etching is performed on the stacked structure 230.

[0079] At this step, a lower electrode power may be applied to a process chamber to achieve anisotropic plasma etching. During the anisotropic etching, the substrate body 131 and the second protrusion 133 have a high etch selectivity ratio relative to the functional
25 layers 231 and the sacrificial layers 232, that is, the second protrusion 133 serves as an etching mask, the stacked structure 230 other than a part thereof just below the second protrusion 133 is etched off, and only the part of the stacked structure 230 just below the second protrusion 133 remains, as shown in FIG. 19.

[0080] At S120b, the sacrificial layers 232 are selectively removed from the remaining part
30 of the stacked structure 230.

[0081] As shown in FIG. 20, after selectively removing the sacrificial layers 232 from the stacked structure 230, a plurality of functional layers 221 in a shape similar to square brackets are formed and spaced apart from each other. More details of the step of

selectively removing the sacrificial layers from the stacked structure can be found in the corresponding description above, and will not be described here.

[0082] In the examples illustrated by FIG. 13 to FIG. 20, the formation of the stacked structure on the substrates with different morphologies are respectively described, the functional layers and the sacrificial layers in the stacked structures are both adaptively formed on the substrates and are formed in a curved shape or a kinked shape, the sacrificial layers are selectively removed from the stacked structures to obtain the functional layers spaced apart from each other and having different morphologies, and the functional layers having the different morphologies can meet requirements in different application scenarios.

For example, when the semiconductor structure is used in a GAA-FET, compared with straight channels in a conventional GAA-FET, the curved or kinked functional layers provided in the embodiment of the present disclosure enable a larger gate width when a gate structure is formed around the functional layers provided in the embodiment of the present disclosure, so that short-channel effects can be suppressed better, and leakage current can be controlled better. When the semiconductor structure is used in an active or passive optical device, the functional layers provided in the embodiment of the present disclosure can function as a waveguide, and realize propagation of optical signals between endpoints in different scenarios.

[0083] Correspondingly, an embodiment of the present disclosure further provides a semiconductor device, as shown in FIG. 21, which may include: a substrate 110; at least one functional layer 211 disposed on the substrate, with the at least one functional layer 211 disposed at intervals in a vertical direction, and at least part of at least one of functional layers 211 being curved; a gate structure disposed around each functional layer 211; and source/drain regions (not shown) respectively disposed on two sides of a plurality of functional layers 211 and connected to the functional layers 211. In the present embodiment, the gate structure may include a gate dielectric layer 215 disposed around the functional layer 211, and a gate electrode layer 216. Due to the curved or kinked functional layer of the semiconductor device provided in the embodiment of the present disclosure, compared with the conventional straight channels, the semiconductor device provided in the embodiment of the present disclosure has a larger gate width, and thus can suppress short-channel effects better and control leakage current better. In an embodiment, a plurality of functional layers 211 are provided. Exemplarily, the semiconductor device may be a 3D DRAM.

[0084] In an example illustrated by FIG. 21, all the functional layers 211 are curved. It should be understood by those of ordinary skill in the art that it is feasible that only part of the functional layers 211 are curved; for one functional layer 211, it is feasible that the functional layer 211 is not entirely curved, and part of sections of the functional layer 211 are curved. It should be understood by those of ordinary skill in the art that the functional layers may be kinked, as shown in FIG. 15 to FIG. 20. Similarly, it is feasible that not all the functional layers are kinked, and only part of the functional layers 211 are kinked; for one functional layer, it is feasible that the functional layer is not entirely kinked, and part of sections of the functional layer are kinked. It should be further understood by those of ordinary skill in the art that in the semiconductor device provided in the embodiment of the present disclosure, some functional layers may include curved sections or be entirely curved, and some functional layers may include kinked sections or be entirely kinked; or one functional layer may include both a curved section and a kinked section, which is not limited in the present disclosure.

[0085] The above embodiments of the present disclosure focus on the differences between the embodiments, and different optimization features of the embodiments can be combined to form better embodiments as long as the different optimization features are not contradictory, which will not be described in detail here for conciseness of the description.

[0086] What is described above is just the embodiments of the present disclosure, but is not intended to limit the present disclosure. Various modifications and changes may be made to the present disclosure by those of ordinary skill in the art. Any modification, equivalent replacement and improvement made within the spirit and principle of the present disclosure should be included in the scope of the appended claims of the present disclosure.

What is claimed is:

1. A manufacturing method for a semiconductor structure, comprising:

forming a stacked structure on a substrate, the stacked structure comprising a functional layer and a sacrificial layer which are alternately stacked, the functional layer and the sacrificial layer being made of a same material, the sacrificial layer being doped with n-type or p-type impurities, and a doping concentration of the sacrificial layer being greater than a doping concentration of the functional layer; and

selectively removing the sacrificial layer from the stacked structure.

2. The manufacturing method of claim 1, wherein a plurality of functional layers and a plurality of sacrificial layers are provided, and at least part of at least one of the functional layers is curved or kinked; and/or

at least part of at least one of the sacrificial layers is curved or kinked.

3. The manufacturing method of claim 1, wherein the substrate comprises a flat surface, and the stacked structure is formed on the flat surface; or

the substrate comprises a wavy surface, and the stacked structure is adaptively formed on the wavy surface; or

the substrate comprises a protrusion structure protruding from a surface of a substrate body, and the stacked structure is adaptively formed on the surface of the substrate body and a surface of the protrusion structure.

4. The manufacturing method of claim 3, wherein the protrusion structure comprises:

a first protrusion, which is located on the substrate body; and

a second protrusion, which is located on the first protrusion, a projection area of the second protrusion on a plane where the substrate body is located being greater than a projection area of the first protrusion on the plane where the substrate body is located, and a projection of the first protrusion on the plane where the substrate body is located being within a projection of the second protrusion on the plane where the substrate body is located.

5. The manufacturing method of claim 4, wherein selectively removing the sacrificial layer from the stacked structure comprises:

performing anisotropic etching on the stacked structure, and remaining a part of the stacked structure just below the second protrusion; and

selectively removing the sacrificial layer from the remaining part of the stacked structure.

6. The manufacturing method of claim 1, wherein the functional layer is an undoped layer; or the doping concentration of the functional layer is less than

$5 \times 10^{14} \text{cm}^{-3}$; or

the doping concentration of the sacrificial layer is greater than $5 \times 10^{14} \text{cm}^{-3}$; or

the doping concentration of the sacrificial layer is $6 \times 10^{14} \text{cm}^{-3}$ to $5 \times 10^{21} \text{cm}^{-3}$.

7. The manufacturing method of any one of claims 1 to 6, wherein forming the stacked structure on the substrate comprises:

alternately epitaxially growing the functional layer and the sacrificial layer on the substrate by a chemical vapor deposition process.

8. The manufacturing method of claim 7, wherein a material of the functional layer and the sacrificial layer is silicon;

epitaxially growing the functional layer comprises: introducing a silicon-containing gas into a process chamber; and

epitaxially growing the sacrificial layer comprises: introducing the silicon-containing gas and a gas containing impurity elements into the process chamber.

9. The manufacturing method of claim 8, wherein the silicon-containing gas comprises at least one of SiH_4 , Si_2H_6 , or SiH_2Cl_2 ; and

the gas containing the impurity elements comprises B_2H_6 , or the gas containing the impurity elements comprises at least one of PH_3 , AsH_3 , SbH_3 , or BiH_3 .

10. The manufacturing method of claim 7, wherein a temperature for epitaxial growth is 400°C to 750°C .

11. The manufacturing method of any one of claims 1 to 6, wherein selectively removing the sacrificial layer from the stacked structure comprises:
performing isotropic plasma etching on the stacked structure with a process gas.

12. The manufacturing method of claim 11, wherein a material of the functional layer and the sacrificial layer is silicon; and
the process gas comprises at least one of a chlorine-containing gas or a bromine-containing gas.

13. The manufacturing method of claim 12, wherein the chlorine-containing gas comprises at least one of Cl_2 or HCl ;
the bromine-containing gas comprises at least one of Br_2 or HBr ; and
the process gas further comprises at least one of N_2 , He , or Ar .

14. The manufacturing method of any one of claims 1 to 6, after selectively removing the sacrificial layer from the stacked structure, further comprising:
performing oxidation treatment on the functional layer; and
removing an oxide layer from a surface of the functional layer.

15. A semiconductor device, comprising:
a substrate;
at least one functional layer, which is disposed on the substrate, the at least one functional layer being disposed at intervals in a vertical direction, and at least part of at least one of functional layers being curved or kinked;
a gate structure, which is disposed around each of the at least one functional layer;
and
source/drain regions, which are respectively disposed on two sides of the at least one functional layer and are connected to the at least one functional layer.

16. A semiconductor device, comprising:
a substrate;

at least one functional layer, which is disposed on the substrate, the at least one functional layer being disposed at intervals in a vertical direction and manufactured with the manufacturing method for a semiconductor structure of any one of claims 1 to 14;

a gate structure, which is disposed around each of the at least one functional layer;

5 and

source/drain regions, which are respectively disposed on two sides of the at least one functional layer and are connected to the at least one functional layer.

17. An optical device, comprising:

10 at least one functional layer, which is configured to transmit optical signals, the at least one functional layer being manufactured with the manufacturing method for a semiconductor structure of any one of claims 1 to 14.