

CLAIMS

1. A method of dicing a semiconductor wafer comprising a plurality of integrated circuits, the method comprising:
 - 5 forming a mask above the semiconductor wafer, the mask comprising a layer covering and protecting the integrated circuits;
patterning the mask with a multiple pass laser scribing process to provide a patterned mask with gaps exposing regions of the semiconductor wafer between the integrated circuits, the multiple pass laser scribing process comprising a first pass along a first edge scribing path, a second pass along a center scribing path, a third pass along a second edge scribing path, a fourth pass along the second edge scribing path, a fifth pass along the center scribing path, and a sixth pass along the first edge scribing path; and
10 plasma etching the semiconductor wafer through the gaps in the patterned mask to singulate the integrated circuits.
- 15 2. The method of claim 1, wherein the multiple pass laser scribing process comprises using a laser beam having a spot size of approximately 10 microns.
3. The method of claim 2, wherein a spacing between centers of the first edge scribing path and the center scribing path is approximately 5 microns, and a spacing between centers of the center scribing path and the second edge scribing path is approximately 5 microns.
- 20 4. The method of claim 3, wherein patterning the mask with the multiple pass laser scribing process comprises forming trenches in the regions of the semiconductor wafer between the integrated circuits, wherein plasma etching the semiconductor wafer comprises extending the trenches to form corresponding trench extensions, and wherein the trenches have a width of approximately 20 microns and a depth in the range of 5-6 microns.
- 25 5. The method of claim 2, wherein a spacing between centers of the first edge scribing path and the center scribing path is approximately 8 microns, and a spacing between centers of the center scribing path and the second edge scribing path is approximately 8 microns.
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6. The method of claim 5, wherein patterning the mask with the multiple pass laser scribing process comprises forming trenches in the regions of the semiconductor wafer between the integrated circuits, wherein plasma etching the semiconductor wafer comprises extending the trenches to form corresponding trench extensions, and wherein the trenches have a width in the
5 range of 25 to 30 microns and a depth of 5 microns or less.
7. The method of claim 1, wherein the multiple pass laser scribing process is based on a Gaussian laser beam.
- 10 8. The method of claim 1, wherein the multiple pass laser scribing process is based on a line-shaped laser beam having a flat top.
9. A method of dicing a semiconductor wafer comprising a plurality of integrated circuits, the method comprising:
15 forming a mask above the semiconductor wafer, the mask comprising a layer covering and protecting the integrated circuits;
patterning the mask with a multiple pass laser scribing process to provide a patterned mask with gaps exposing regions of the semiconductor wafer between the integrated circuits, the multiple pass laser scribing process comprising a first pass along a center scribing path, a
20 second pass along a first edge scribing path, a third pass along a second edge scribing path, a fourth pass along the second edge scribing path, a fifth pass along the first edge scribing path, and a sixth pass along the center scribing path; and
plasma etching the semiconductor wafer through the gaps in the patterned mask to
singulate the integrated circuits.
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10. The method of claim 9, wherein the multiple pass laser scribing process comprises using a laser beam having a spot size of approximately 10 microns.
11. The method of claim 10, wherein a spacing between centers of the first edge scribing path
30 and the center scribing path is approximately 5 microns, and a spacing between centers of the center scribing path and the second edge scribing path is approximately 5 microns.

12. The method of claim 11, wherein patterning the mask with the multiple pass laser scribing process comprises forming trenches in the regions of the semiconductor wafer between the integrated circuits, wherein plasma etching the semiconductor wafer comprises extending the trenches to form corresponding trench extensions, and wherein the trenches have a width of
5 approximately 20 microns and a depth in the range of 5-6 microns.

13. The method of claim 10, wherein a spacing between centers of the first edge scribing path and the center scribing path is approximately 8 microns, and a spacing between centers of the center scribing path and the second edge scribing path is approximately 8 microns.
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14. The method of claim 13, wherein patterning the mask with the multiple pass laser scribing process comprises forming trenches in the regions of the semiconductor wafer between the integrated circuits, wherein plasma etching the semiconductor wafer comprises extending the trenches to form corresponding trench extensions, and wherein the trenches have a width in the
15 range of 25 to 30 microns and a depth of 5 microns or less.

15. The method of claim 9, wherein the multiple pass laser scribing process is based on a Gaussian laser beam.
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