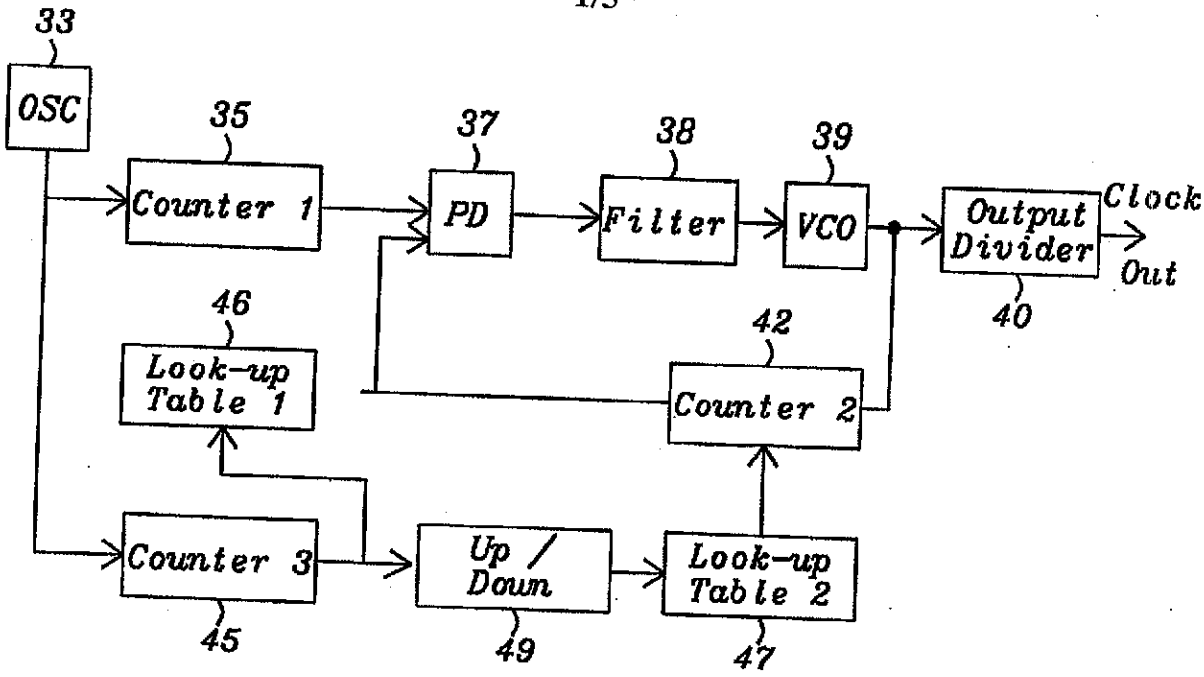

FIG. 1 – Prior Art

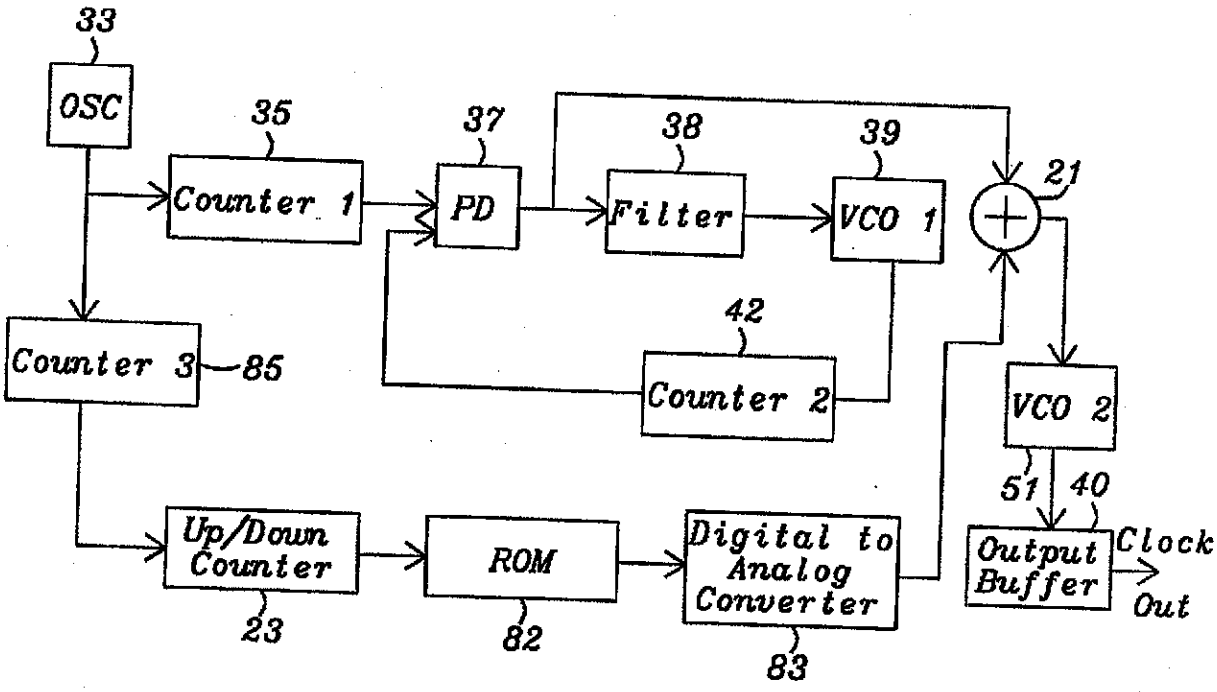

FIG. 2 – Prior Art

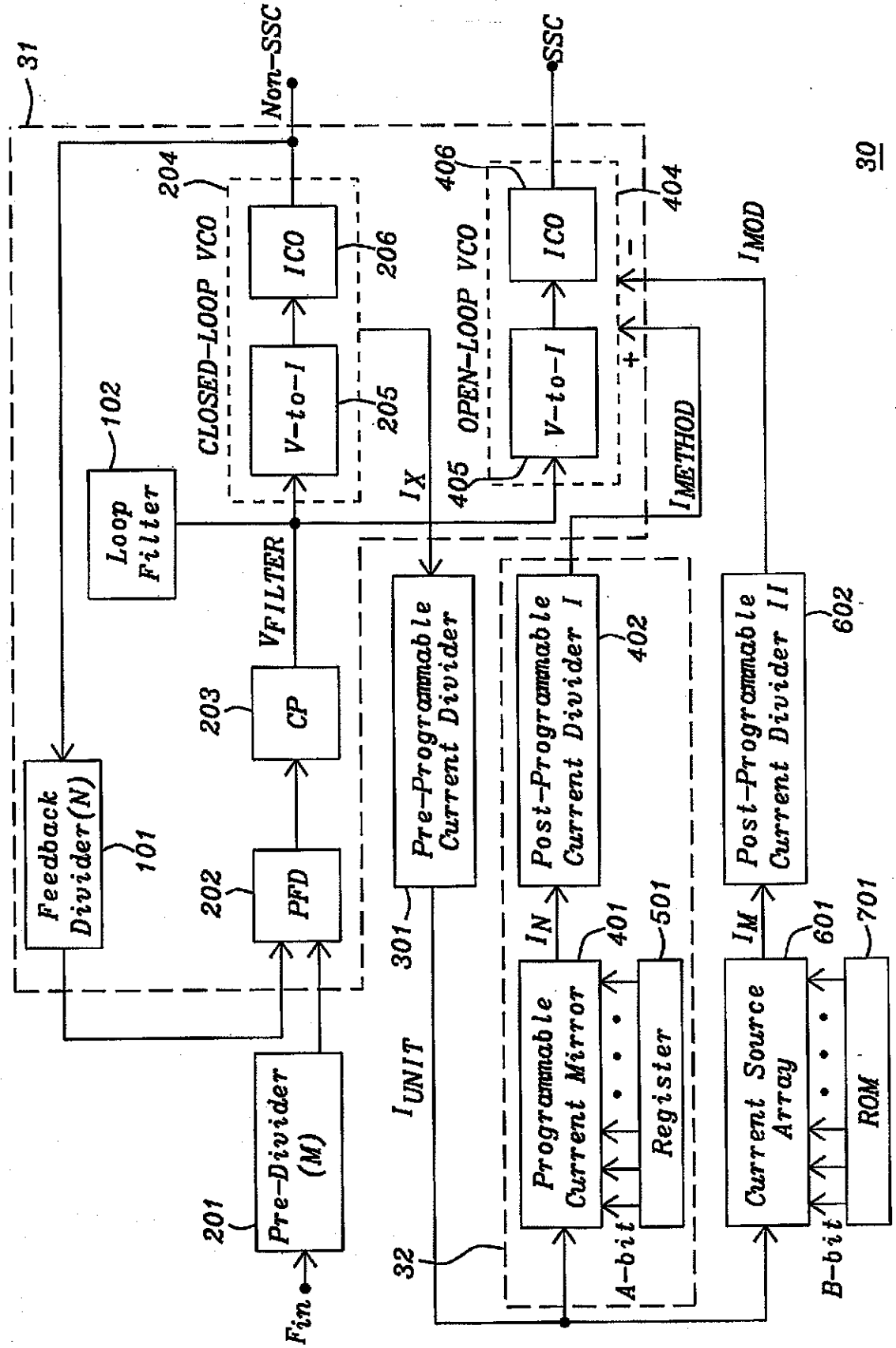
31
Non-SSC
SSC
30
204
CLOSED-LOOP VCO
ICO
206
V-to-I
205
102
Loop Filter
I_X
406
OPEN-LOOP VCO
ICO
V-to-I
405
404
I_{MOD}
I_{METHOD}
V_{FILTER}
203
CP
202
PFD
Feedback Divider(N)
101
Pre-Programmable Current Divider
301
Post-Programmable Current Divider I
402
Post-Programmable Current Divider II
602
I_{UNIT}
I_N
401
501
I_M
601
701
Programmable Current Mirror
Register
Current Source Array
ROM
A-bit
B-bit
32
201
Pre-Divider (M)
Fin

FIG. 3

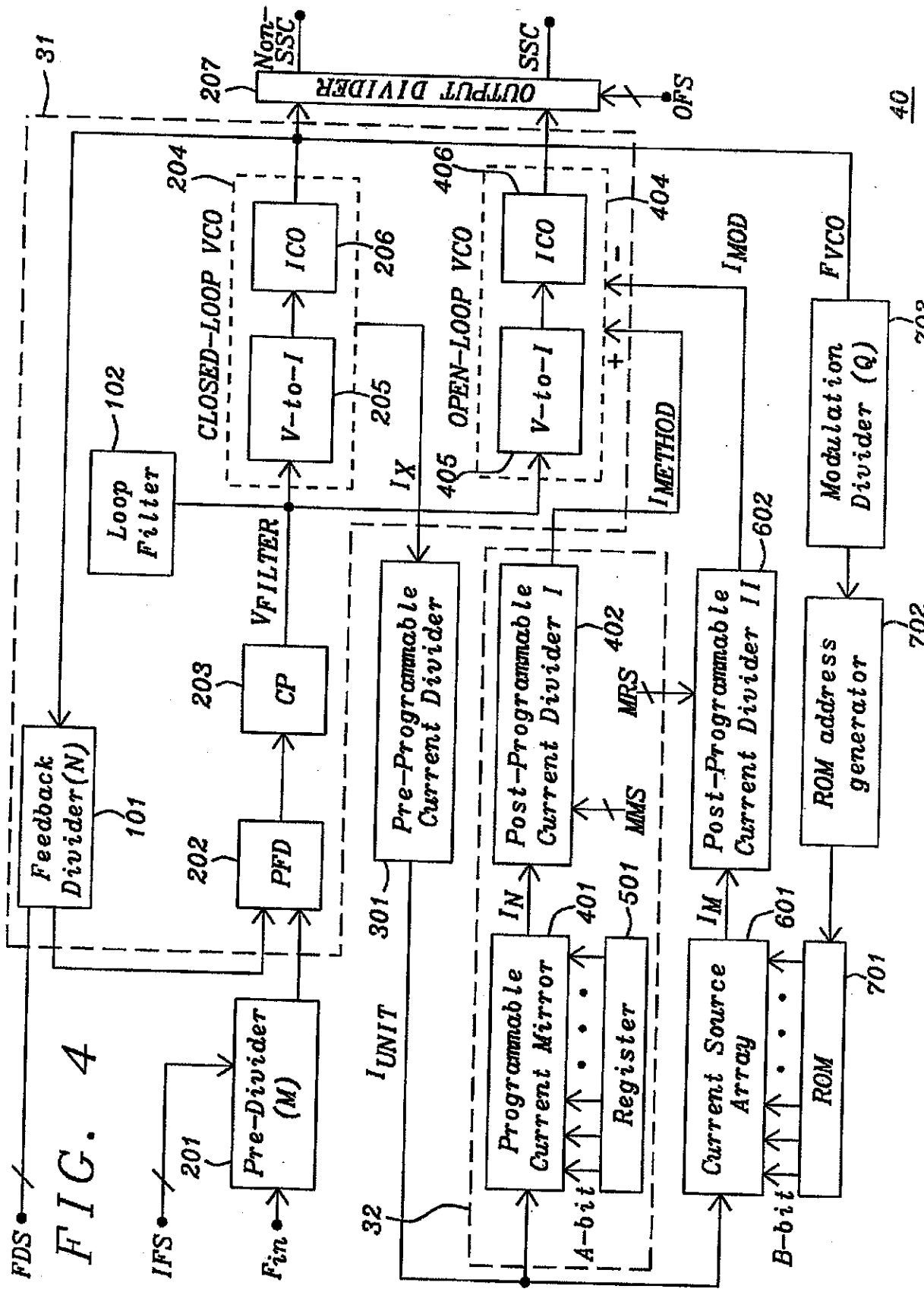
FDS
IFS
Fin
Feedback Divider(N)
101
Pre-Divider (M)
201
PFD
202
CP
203
VFILTER
Loop Filter
102
CLOSED-LOOP VCO
204
V-to-I
205
ICO
206
OUTPUT DIVIDER
207
Non-SSC
SSC
OFS
31
IX
OPEN-LOOP VCO
405
406
V-to-I
ICO
404
IMETHOD
IMOD
FVCO
Modulation Divider (Q)
703
ROM address generator
702
Pre-Programmable Current Divider
301
IUNIT
32
Post-Programmable Current Divider I
402
MRS
MMS
IN
Programmable Current Mirror
401
Register
501
A-bit
Post-Programmable Current Divider II
602
IM
Current Source Array
601
ROM
701
B-bit
40

FIG. 4

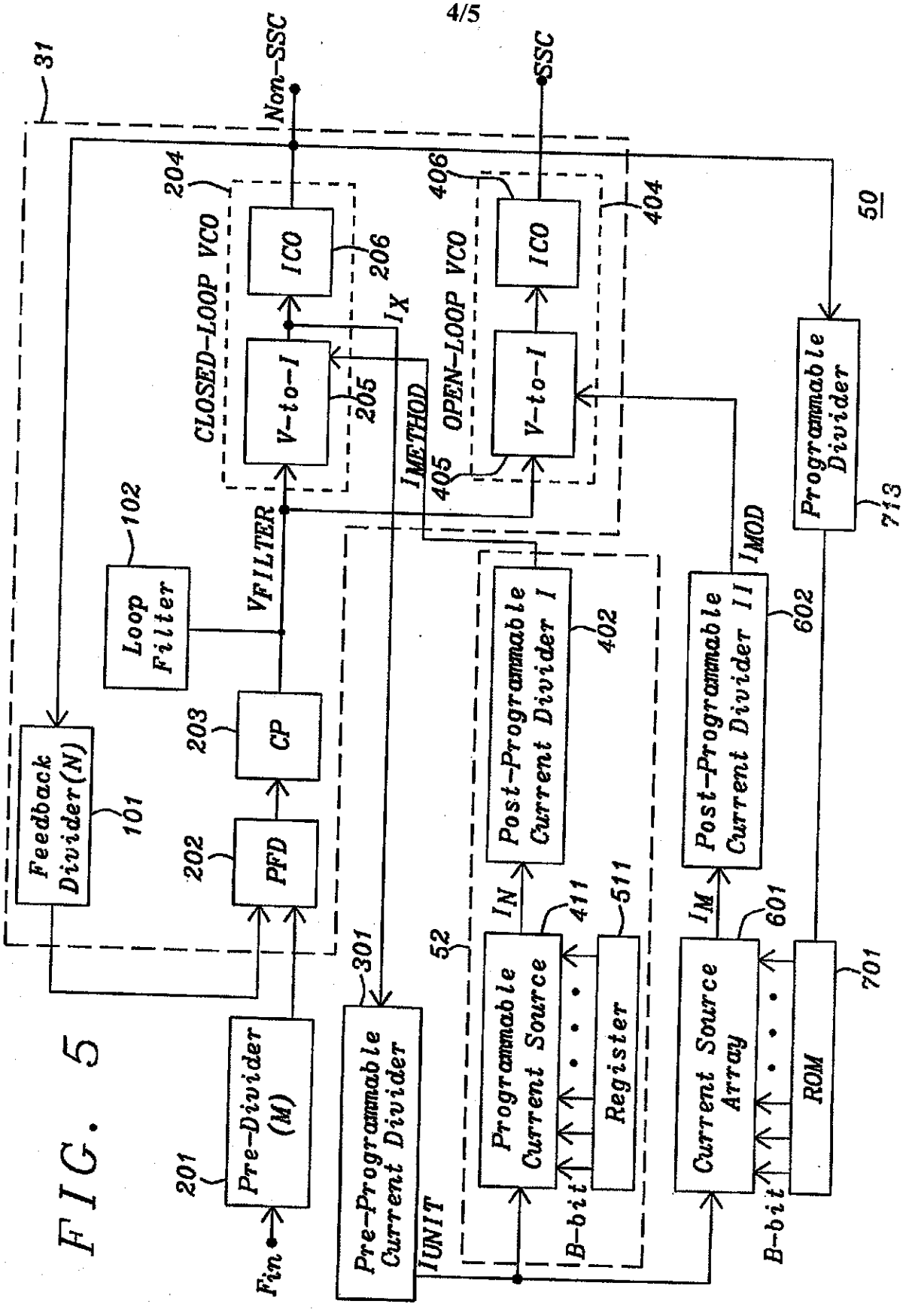
31
Non-SSC
SSC
204
406
404
50
CLOSED-LOOP VCO
OPEN-LOOP VCO
ICO
ICO
206
I_X
V-to-I
V-to-I
205
I_{METHOD}
405
102
Loop Filter
V_{FILTER}
203
CP
202
PFD
Feedback Divider(N)
101
Post-Programmable Current Divider I
402
Post-Programmable Current Divider II
602
I_{MOD}
Programmable Divider
713
I_N
411
511
I_M
601
52
Programmable Current Source
Register
Current Source Array
ROM
701
B-bit
B-bit
301
Pre-Programmable Current Divider
I_{UNIT}
201
Pre-Divider (M)
F_{in}

FIG. 5

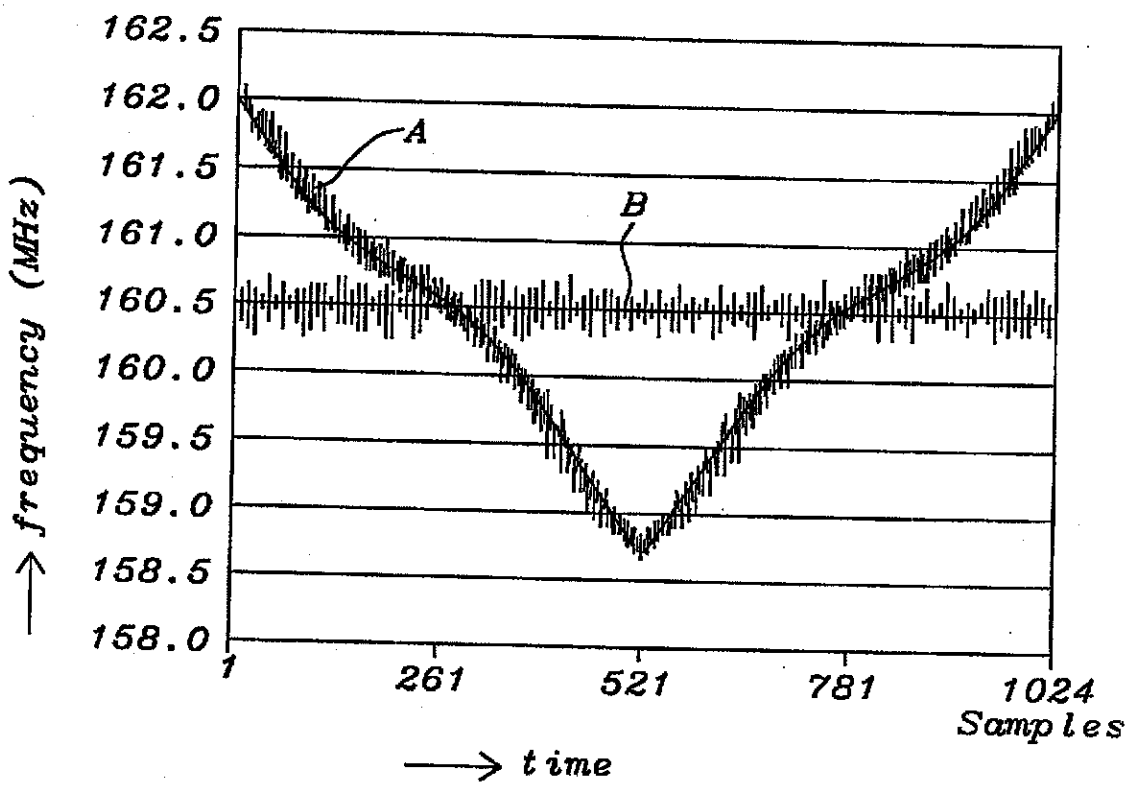
162.5
162.0
161.5
161.0
160.5
160.0
159.5
159.0
158.5
158.0
frequency (MHz)
A
B
1
261
521
781
1024
Samples
time

FIG. 6