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(54) IMPROVEMENTS IN OR RELATING TO TELECOMMUNICATIONS RECEIVERS

(71) We, LICENTIA PATENT-VERWALTUNGS-GESELLSCHAFT MIT BESCHRANKTER HAFTUNG, a company organised under the laws of Germany, of Theodor-Stern-Kai 1, 6, Frankfurt/Main 70, Germany, do hereby declare the invention, for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement:—

The present invention relates to the display of channel numbers identifying the transmitter to which a telecommunications receiver, for example a superheterodyne radio receiver, is tuned. The invention is particularly, though not exclusively, related to the identification of such transmitters by a system of channel numbers such as that known for radio frequencies in the Federal Republic of Germany.

It is known (Radio-Mentor 1973, pp 389—390 and Funk-Technik 1971, pp 157—159) to provide in superheterodyne radio receivers a digital display of the received frequencies. In some countries, for example Germany, it is also known to identify transmitters by the provision of a channel number.

It is an object of the present invention to provide an arrangement providing automatic digital display of such channel identifying members.

According to the invention there is provided an apparatus for identifying the frequency of transmissions, to which a superheterodyne receiver is tuned, by one of a plurality of channel numbers, each respective to a different transmission frequency, by counting, within a predetermined counting period, oscillations provided at the local oscillator frequency of said receiver, the system including means for effectively subtracting from or adding to the count of said oscillations a count corresponding to the intermediate frequency of said receiver, means for further effectively subtracting a count corresponding to a reference frequency asso-

ciated with the lowest of said channel numbers, counting means for providing an output related to the frequency resulting from said further subtraction and indicator means for displaying the said output to provide said channel number.

In order that the invention may be clearly understood and readily carried into effect examples thereof will now be described with reference to the accompanying drawings of which:—

Figure 1 shows a block diagram of the apparatus according to the invention.

Figure 2 shows a practical example of the apparatus.

Figure 3 is a timing diagram used in explaining the system shown in Figure 2, and

Figure 4 shows another practical example.

The examples of the invention will be described in terms of the channel number system known in the Federal Republic of Germany.

In present day allocation of transmitter frequencies in the VHF band in Germany the channel figure 0 corresponds to the frequency of 87.0 MHz. Therefore if this frequency is additionally subtracted from the frequency of the receiver oscillator from which the IF has already been subtracted the correct channel figure 0 is obtained.

However, in the allocation of transmitter frequencies in the VHF band in Germany the following situation exists. The channels allocated are spaced by intermediate steps of 300 kHz. The transmitter frequencies are however only spaced by 100 kHz steps, so that the mere giving of a channel figure is not sufficient to identify a transmitter. It is therefore customary in Germany to provide the figure of the transmitter concerned with a "+" or "-" as index. For example: channel 13=90.9 MHz; channel 13₋=90.8 MHz; channel 13₊=91.0 MHz. The lowest channel identifier occurring is thus channel 0₋=86.9 MHz.

Referring now to the drawings, in Figure 1 the received signal passes via an antenna

1 to a superheterodyne receiver 2. This includes inter alia an oscillator for a mixer stage, an intermediate frequency (IF) amplifier, a demodulator and an LF amplifier which feeds the loudspeaker 3. The oscillator output, which differs in frequency from the received signal by the number of oscillations of the IF, is amplified by a wide band amplifier (not shown) and converted into rectangular oscillations 10 (counting pulses). These pulses serve to control an electronic counter 8. By means of a frequency divider (initial divider) 9 the counting pulses are divided before they are counted. The division ratio may be different for AM and FM operation, and may for example be 100:1 for FM operation. Then only each hundredth pulse is counted. This is however unimportant, since with suitable gating periods a five place and sufficiently exact count is nevertheless still obtained.

The divider 9 is connected to a gate 4, which is controlled by a time base in such manner that it is periodically opened for a period of 10ms and then closed for a period of 10ms. Other opening and closing periods are also possible. The period during which gate 4 is opened is called the gating period or the counting period, since only during this period the counting pulses are counted. However, the actual counting action of the electronic counter 8 must not start at the beginning of the gating period, since the frequency of the oscillator differs from the received frequency by the IF. Normally in the superheterodyne receivers the oscillator frequency is above the received frequency, so that it is necessary to subtract the IF since only the received frequency is of interest. In the case in which the oscillator frequency is below the received frequency, a suitable addition must be performed. For channel display however this step of subtraction or addition is not alone sufficient. It is also necessary to take from the oscillator frequency the frequency corresponding to the lowest channel. Only then may the electronic counter 8 begin to count the channels. In Figure 1 this is effected by an additional counter 6, the input of which is connected to the gate 4 and the output of which is connected to the electronic counter 8. The additional counter 6 has the effect, by pre-counting, of allowing the counting pulses to reach the electronic counter 8, so that this counter begins again to count from "0", only when the counting condition of the additional counter 6 corresponds to the sum of the IF and the frequency of the lowest channel. The beginning of the counting of the channels by the electronic counter 8 is therefore shifted within the gating period by a time corresponding to this sum. The counting condition of the electronic counter 8 at the end of the gating period is trans-

mitted in response to a pulse from a time base 7 to the store, is decoded and displayed on an indicator 5.

It is also possible to omit the additional counter 6, the electronic counter 8 itself counting the said sum at the beginning of the gating period, being set to the zero counting condition upon attainment of the corresponding condition, and thereupon counting the channels.

As has also been described above, the present channel spacing is 300 kHz, i.e. at the output of the electronic counter associated with the counting there must always be available, after counting 300 kHz, the number that follows the preceding number. The necessary triple rhythm of the counting operation is achieved by arranging that the additional counter 6, after counting the above-mentioned sum, is set to the zero counting condition and is connected up as a 3:1 divider stage. Only each third counting pulse on the input of the additional counter 6 then passes to the electronic counter 8. After the additional counter 6 has counted three counting pulses, it is set to the zero counting condition again and begins to count the next three pulses and so on. At the end of the counting time the counting condition of the additional counter 6 is either "0", "1" or "2". The additional counter 6 is connected to the indicator 5, on a panel of which is represented the symbol "-" for the counting condition "0", and the symbol "+" for the counting condition "2". For the counting condition "1" there is no display in the associated indicator panel. By means of this additional feature as described it is possible to take into account each of the three possible transmitters located in one channel.

In Figure 2 there is illustrated a practical example of the invention which will be described below in more detail with the aid of the time diagram shown in Figure 3. The practical example shown permits both a digital channel display and a digital frequency display and is particularly advantageous when using digital counters of a high degree of circuit integration. It will first be assumed that the frequency for AM operation is to be displayed, i.e. the rectangular pulses 10 originate from the AM oscillator (not shown). In a first divider 13 there is effected a division of the frequency of the oscillations 10 in the ratio 2:1. Since the display in MHz is selected differently for FM and AM operation, in order to obtain accuracy corresponding to the band (4 places for FM, e.g. 102.4 MHz; 5 places for AM, e.g. 11.830 MHz), different divisions of the frequency are necessary. For AM operation a selector circuit 16 is so controlled by means of a voltage U, that the oscillations 10 divided in the ratio 2:1 bypass a divider 14 and pass directly by a path 15 to a gate 4, 130

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where a further division in the ratio 5:1 takes place. The total division ratio is therefore 10:1.

In Figure 3 the gating period of the gate 4 is shown at the top. The gate 4 is opened every 20 ms for a period of 10 ms. It is connected to a decade counting stage 19. This includes the actual counter, a store, a decoder and is provided for counting the last place, that is the least significant place, of the frequency to be displayed on the indicator 5. To the counting stage 19 are connected a further selector circuit 20 which is controlled by a voltage U_1 , and the counter 6 for counting the IF. If a display of the frequency and not the channels is required, a selector circuit 20 is controlled by the voltage U_1 in such manner that pulses from the output of the counting stage 19, for the four most significant places, pass to the counting stage 8, which similarly includes a counter, a store and decoder and counts up to four places. These four most significant places are those which are to be counted when the channel number is required.

Together with the counting stage 8 the counter 6 begins to count the pulses coming from the counting stage 19. Via a suitable designed programme circuit 28 a pulse then passes to a selector switch 29 when the counting condition of the counter 6 has attained the IF corresponding to the type of operation (AM or FM). Via the selector switch 29 the pulse comes to a store 30, where it is stored. The store 30 is connected to a gate 26, which is thereby opened during the storage period of the store 30. The store pulse corresponds to a logical 1, which via the gate 26 and an OR gate 27 is fed to the counter 6 which is thereby set to zero (reset) after its counting condition corresponds to the particular IF. From a beat generator 24 controlled by the time base 7 pulses at the spacing of 20 ms pass to the OR gate 27 so as to set the counter 6 to zero before the beginning of the following counting period, such that the next following counting of the IF can begin from the zero counting condition.

The store 30 is also connected to a differentiating member 31, which shapes the stored pulse into a short pulse. This pulse has the effect that the counting stage 8 is set to zero (reset) and begins to count again after the counter 6 has counted the IF. In Figure 3 four of these pulses are shown in the third series from the top. They are located within the gating period of the gate 4. In the time intervals between these pulses and the end of the gating times, the received frequency is counted by the counting stage 8. The particular counting condition at the end of the gating period of the gate 4 is then taken before the commencement of a new counting operation, hence within the period

for which the gate 4 is closed, by means of the beat pulse taken from the beat generator 24 (Figure 3, lowest row) into the store of the counting stage 8. There follows a decoding which is followed by the display of the frequency on the indicator 5. This occurs fifty times a second.

In FM operation the path 15 in the upper part of Figure 2 is closed by suitably operating the selector switch 16, so that divisions of 2:1, 10:1 and 5:1 take place successively. Furthermore, instead of the IF related to AM operation, a pulse is given to the store 30 via the programme circuit 28 only after counting of the IF for FM. The corresponding reset pulse occurs as in AM operation.

If, instead of the frequency, the channel is to be displayed, the direct path from the counting stage 19 to the counter 8 is closed by suitably operating the selector circuit 20, since the counter 8 must count at a different rhythm corresponding to the channel spacing of 300 kHz. The selector switch 29 is now so operated via the voltage U_1 that a pulse is taken from the programme circuit 28 and fed into the store 30 only for a counting condition of the counter 6 that corresponds to the sum of the IF for FM operation and the frequency of the lowest channel (86.9 MHz, channel 0.). The counter 8 is set to zero upon attainment of the said sum via the differentiating member 31, and the counter 6 is set to zero via the gate 26 and the OR gate 27. The counter 8 can now begin to count beginning at channel 0.. However, it does not receive the counting pulses directly from the preceding counting stage 19. The indicator of stage 19 is also not necessary in this case, since the least significant digit of the frequency is not needed for the channel count, and it is made ineffective, by for example, blanking out the corresponding display tube (not shown).

The counting pulses for the counter 8, necessary for counting the channels are obtained as follows:— an output 32 for the counter 6 is provided. The output 32 which is connected to the selector circuit 20 and the gate 26, is so selected that a pulse occurs at that point when the counter 6 has counted three pulses. The counter 6 is thereupon again set to the zero counting condition via the gate 26, which is closed during the counting and is opened only for the pulses coming from the output 32 of the counter 6, and the OR gate 27. If a further three pulses are counted by the counter 6, the next pulse occurs at the output 32 and the counter 6 is again set to zero, and so on. In this way it is arranged that the counter 8 receives the counting pulse via the selector circuit 20 after each three pulses at the input of the counter 6. In comparison with the mode of counting further described

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above for frequency display, the counting now takes place in accordance with the FM channel spacing of 300 kHz. The counter 6, which at the beginning of the gating period of the gate 4 first serves for initial counting, is thus brought into use, in advantageous manner, for counting the channels by the counting stage 8, in that it now acts as a 3:1 divider stage.

The counting condition arising at the end of the gating period of the gate 4 (see Figure 3), which corresponds to the received channel, is, prior to the commencement of the next gating period and hence prior to the commencement of the next counting operation, taken up by the pulse shown in the lowest row in Figure 3 into the store, decoded and displayed.

For the complete indication of the received transmitter there is still missing the above-described indicating of the channel number with an index "+" or "-" or with no index. For this purpose the indicator 5 is operated by a further output 33 of the counter 6 via a gate 22. From the output 33 is taken the end condition of the counter 6 counting in triple rhythm, at the end of the gating period of the gate 4, via the gate 22. The passage of the gating period of this gate 22 is illustrated in Figure 3 in the fourth row. It is opened for 10 ms. fifty times a second by the beat generator 24, in fact whenever the gate 4 is closed. This is necessary because no store is provided for storing the end condition of the counter 6. During the counting period (gating period of gate 4) the gate 22 must therefore be closed so that the counting conditions between "0" and "2" occurring continuously at the output 33 are not displayed. At the end of the counting operation and hence at the end of the gating period of the gate 4 three final conditions of the counter 6 are possible. At the final condition "0" a "-" is displayed by a suitable decoding, and in the final condition "2" a "+" is displayed, whilst in the final condition "1" no display occurs in the associated display field. The display takes place fifty times a second. Owing to the integration action of the human eye the impression of a flicker-free picture results.

In digital channel display it is also possible to perform the said additional 3:1 division during the said counting period. Instead of the sum of the IF and the frequency of the lowest channel, a third part of this sum must then be counted, before the electronic counter 8, counts the channels, beginning with channel 0. A corresponding practical example is illustrated in Figure 4. This practical example permits the use of digital counters of a relatively low degree of circuit integration, which are capable of being programmed. As a 3:1 dividing stage there is provided a frequency divider 34, which is

effective only for digital display of the channel number, since the path shown at 38 is then ineffective owing to suitable operation of a selector circuit 35. In digital frequency display, in contrast, the pulses coming from the counting stage 19 pass directly via the path 38 and the selector circuit 35 to the counter 8.

The divider 34 must be included at the place at which it receives a pulse after each 100 kHz, and therefore counts the 100 kHz steps, so that, like the additional counter 6 in Figure 2, it serves also to additionally identify the channel figure with the index "+" or "-", by being connected to the indicator 5 via a gate 36 (corresponding to the gate 22 in Figure 2).

As above mentioned, owing to the provision of the divider 34 only a third part of the sum formed from the IF and the frequency of the lowest channel is counted. Here, the case may then arise in which this sum is not exactly divisible by three and therefore a remainder occurs. What is done in this case will now be explained by a numerical example. Considering the sum of the IF and the frequency of the lowest channel to be $10.7 \text{ MHz} + 86.9 \text{ MHz} = 97.6 \text{ MHz}$. Division by three then gives a value of 32.5 MHz with a remainder 1. The frequency divider 34, which also operates as a counter, is therefore programmed by a programming unit 37 to the counting condition "2". The value to which the frequency divider 34 must be programmed is obtained from the 3:1 divider by subtracting from "3" the remainder, which here is $3 - 1 = 2$. The first pulse then sets the frequency divider 34 to zero, whereby the remainder has been taken care of. The pulse number that then follows is thus divisible by three without remainder. The electronic counter is programmed by the programming unit 37 to 32.5 MHz and therefore begins to count the channels only after it has counted this value. At which point its counting condition is set to zero).

There is also the possibility of obviating the additional divider 34 and of using the electronic counter 8 itself as a divider, with its first counting stage directly following the counting stage 19 being formed as a 3:1 divider in channel display. This possibility exists when there are counting stages of the counter 8 which can be changed over as regards division ration. Under some circumstances the last place (last counting stage of the counter 8) may indeed run over, since the counting stage connected up as a 3:1 divider gives a pulse of the following stage after each third counting pulse—instead of after each tenth counting pulse. This however is unimportant since the figure corresponding to this last counting stage is not required for channel display and the associated display field of the indicator 5 is switched

out. The display of the said indices "+" or "-" again occurs corresponding to the possible counting conditions "0", "1" or "2" of the 3:1 divider.

5 In frequency display—instead of channel display—the selector circuit 35 in Figure 4 is so controlled that the counting pulses from the counting stage 19 pass via the path 38 to the counter 8, bypassing the unrequired divider 34. This counter 8 is programmed to the complement of the IF (to the value "zero" IF). This is achieved by causing its counting condition to assume the value zero after the counting of a number of pulses corresponding to the IF, and subsequently counting the received frequency. As already described with reference to Figure 2, in Figure 4 also after the end of the gating period of the gate 4 the counting condition is decoded and taken into the indicator 5 by means of the pulse taken from the beat generator 24 and optically displayed. Both in Figure 2 and in Figure 4 the display fields, not required at any time, are rendered ineffective by being blanked out.

WHAT WE CLAIM IS:—

1. An apparatus for identifying the frequency of transmissions, to which a superheterodyne receiver is tuned, by one of a plurality of channel numbers, each respective to a different transmission frequency, by counting, within a predetermined counting period, oscillations provided at the local oscillator frequency of said receiver, the system including means for effectively subtracting from or adding to the count of said oscillations a count corresponding to the intermediate frequency of said receiver, means for further effectively subtracting a count corresponding to a reference frequency associated with the lowest of said channel numbers, counting means for providing an output related to the frequency resulting from said further subtraction and indicator means for displaying the said output to provide said channel number.

2. An apparatus according to Claim 1 including means for applying to said counting means a predetermined proportion of the counts representing the frequency resulting from said further subtraction, means for deriving from said counts a further indication individually identifying one or more different transmissions having the same channel number, and further indicator means for displaying said further indication.

3. An apparatus according to Claim 2 wherein said first and further indicator means are provided as a single indicator.

4. An apparatus according to any of the preceding claims wherein said means for subtracting or adding and said means for further subtracting together comprise a coun-

ter arranged to count the local oscillator frequency oscillation up to the sum of the intermediate frequency and said reference frequency and upon the attainment of that counting condition set a second counter to the zero counting condition and thereafter applies counting pulses to said second counter at a rate related to said local oscillator frequency and wherein said second counter is said counting means.

5. An apparatus according to Claim 2 as limited by Claim 4 wherein said counter is arranged to provide a counting pulse to said second counter for every three pulses of said local oscillator frequency oscillations received by said counter after attaining said condition.

6. An apparatus according to Claim 5 wherein an output of said counter having an output pulse for every three input pulses, is connected, via a gate and an OR gate, to a resetting input of said counter and to the input of said second counter and wherein the output of said second counter is displayed by said indicator means at the end of the counting period.

7. An apparatus according to either of Claims 5 and 6 wherein the counting condition of said counter at the end of the counting period is applied to said further indicator means via a gate which is open for a predetermined time interval and is displayed as the sign "-" for the "0" counting condition, the sign "+" for the "2" counting condition and is not displayed for the "1" counting condition.

8. An apparatus according to Claim 2 including a frequency divider arranged to divide its input pulses in the ratio 3:1, so that only a third part of the sum of the intermediate frequency and the reference frequency is subtracted from the local oscillator frequency oscillations and wherein said counting means is set to the zero counting condition after counting the said third part.

9. An apparatus according to Claim 8 wherein the frequency divider is arranged to receive a counting pulse after each number of pulses corresponding to the separation frequency between said different transmissions.

10. An apparatus according to either of Claims 8 or 9 wherein, if said sum is not exactly divisible by three the frequency divider is arranged to attain the counting condition given by the subtraction of the remainder from the number three, so that it attains a zero counting condition after counting a number of pulses given by the remainder and the following count is exactly divisible by three and wherein the counting means is synchronised to the said value divisible by three.

11. An apparatus according to Claim 8 wherein the frequency divider may be

out. The display of the said indices "+" or "-" again occurs corresponding to the possible counting conditions "0", "1" or "2" of the 3:1 divider.

5 In frequency display—instead of channel display—the selector circuit 35 in Figure 4 is so controlled that the counting pulses from the counting stage 19 pass via the path 38 to the counter 8, bypassing the unrequired divider 34. This counter 8 is programmed to the complement of the IF (to the value "zero" IF). This is achieved by causing its counting condition to assume the value zero after the counting of a number of pulses corresponding to the IF, and subsequently counting the received frequency. As already described with reference to Figure 2, in Figure 4 also after the end of the gating period of the gate 4 the counting condition is decoded and taken into the indicator 5 by means of the pulse taken from the beat generator 24 and optically displayed. Both in Figure 2 and in Figure 4 the display fields, not required at any time, are rendered ineffective by being blanked out.

WHAT WE CLAIM IS:—

30 1. An apparatus for identifying the frequency of transmissions, to which a superheterodyne receiver is tuned, by one of a plurality of channel numbers, each respective to a different transmission frequency, by counting, within a predetermined counting period, oscillations provided at the local oscillator frequency of said receiver, the system including means for effectively subtracting from or adding to the count of said oscillations a count corresponding to the intermediate frequency of said receiver, means for further effectively subtracting a count corresponding to a reference frequency associated with the lowest of said channel numbers, counting means for providing an output related to the frequency resulting from said further subtraction and indicator means for displaying the said output to provide said channel number.

50 2. An apparatus according to Claim 1 including means for applying to said counting means a predetermined proportion of the counts representing the frequency resulting from said further subtraction, means for deriving from said counts a further indication individually identifying one or more different transmissions having the same channel number, and further indicator means for displaying said further indication.

60 3. An apparatus according to Claim 2 wherein said first and further indicator means are provided as a single indicator.

65 4. An apparatus according to any of the preceding claims wherein said means for subtracting or adding and said means for further subtracting together comprise a coun-

ter arranged to count the local oscillator frequency oscillation up to the sum of the intermediate frequency and said reference frequency and upon the attainment of that counting condition set a second counter to the zero counting condition and thereafter applies counting pulses to said second counter at a rate related to said local oscillator frequency and wherein said second counter is said counting means.

5. An apparatus according to Claim 2 as limited by Claim 4 wherein said counter is arranged to provide a counting pulse to said second counter for every three pulses of said local oscillator frequency oscillations received by said counter after attaining said condition.

6. An apparatus according to Claim 5 wherein an output of said counter having an output pulse for every three input pulses, is connected, via a gate and an OR gate, to a resetting input of said counter and to the input of said second counter and wherein the output of said second counter is displayed by said indicator means at the end of the counting period.

7. An apparatus according to either of Claims 5 and 6 wherein the counting condition of said counter at the end of the counting period is applied to said further indicator means via a gate which is open for a predetermined time interval and is displayed as the sign "-" for the "0" counting condition, the sign "+" for the "2" counting condition and is not displayed for the "1" counting condition.

8. An apparatus according to Claim 2 including a frequency divider arranged to divide its input pulses in the ratio 3:1, so that only a third part of the sum of the intermediate frequency and the reference frequency is subtracted from the local oscillator frequency oscillations and wherein said counting means is set to the zero counting condition after counting the said third part.

9. An apparatus according to Claim 8 wherein the frequency divider is arranged to receive a counting pulse after each number of pulses corresponding to the separation frequency between said different transmissions.

10. An apparatus according to either of Claims 8 or 9 wherein, if said sum is not exactly divisible by three the frequency divider is arranged to attain the counting condition given by the subtraction of the remainder from the number three, so that it attains a zero counting condition after counting a number of pulses given by the remainder and the following count is exactly divisible by three and wherein the counting means is synchronised to the said value divisible by three.

11. An apparatus according to Claim 8 wherein the frequency divider may be



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switched off and the counting pulse from the stage preceding the divider input directly to the counting means.

- 5 12. An apparatus according to any of Claims 8 to 10 wherein the frequency divider is a component of the counting means and the first counting stage of said counter is, for that purpose, capable of being set to a

division ratio appropriate to the channel frequency spacing.

13. An apparatus substantially as herein described with reference to Figure 1 and either Figures 2 and 3 or Figure 4 of the accompanying drawings.

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