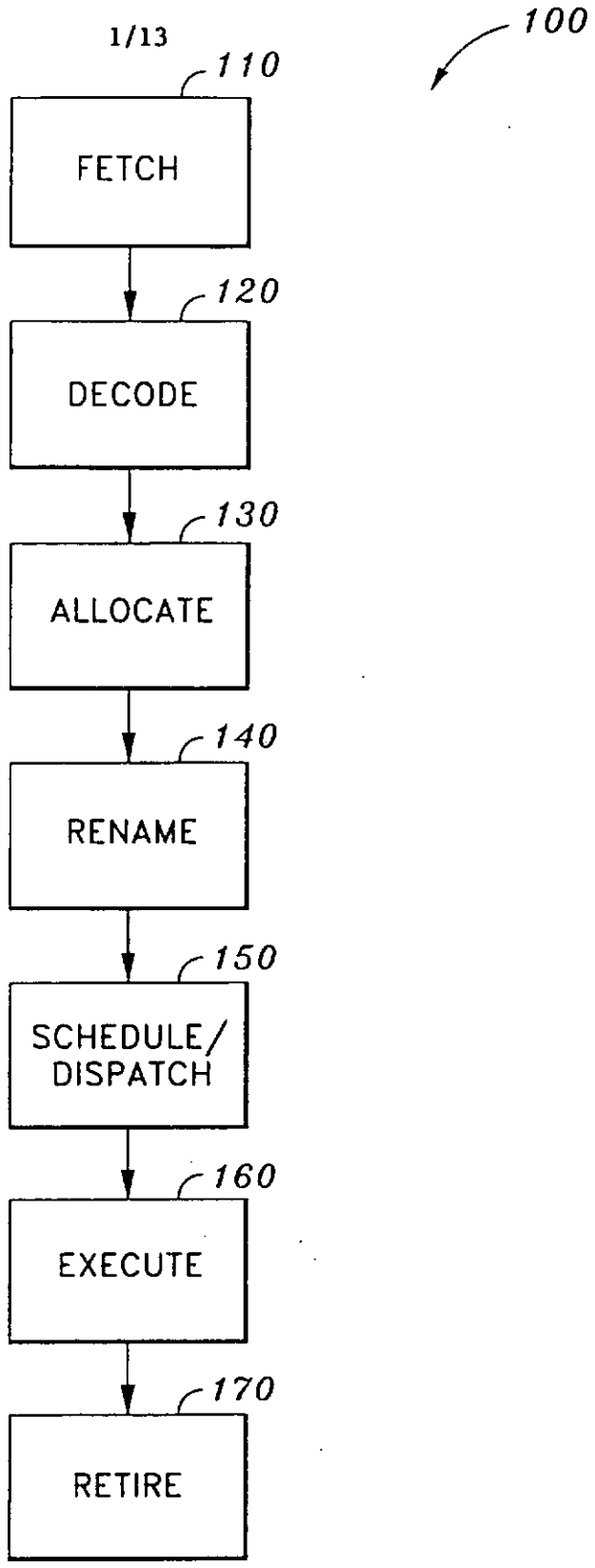

100
110
FETCH
120
DECODE
130
ALLOCATE
140
RENAME
150
SCHEDULE/
DISPATCH
160
EXECUTE
170
RETIRE

FIG. 1

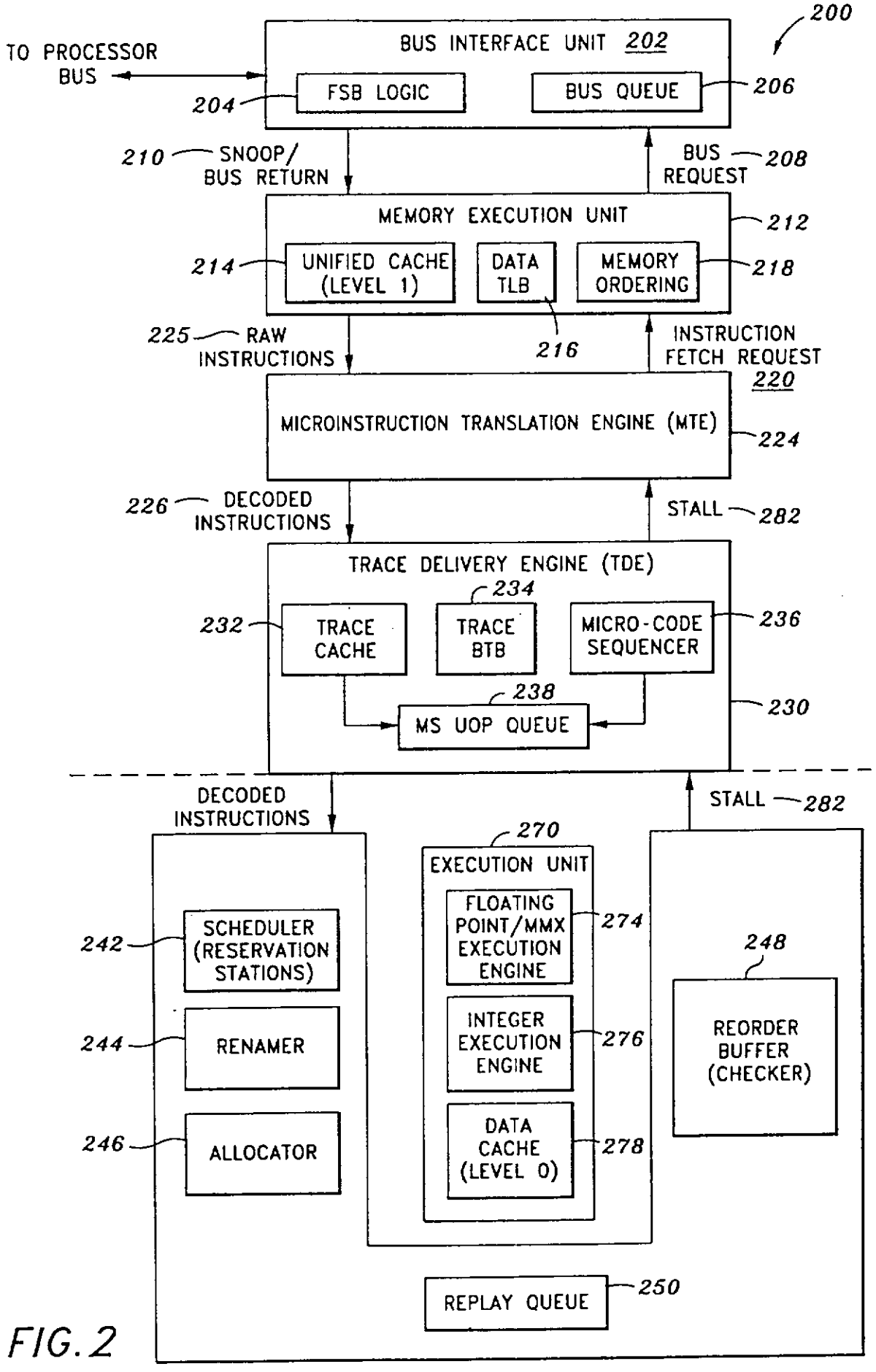

200
TO PROCESSOR BUS
BUS INTERFACE UNIT 202
FSB LOGIC
204
BUS QUEUE
206
210 SNOOP/ BUS RETURN
BUS REQUEST 208
MEMORY EXECUTION UNIT
212
214 UNIFIED CACHE (LEVEL 1)
DATA TLB
MEMORY ORDERING
218
216
225 RAW INSTRUCTIONS
INSTRUCTION FETCH REQUEST 220
MICROINSTRUCTION TRANSLATION ENGINE (MTE)
224
226 DECODED INSTRUCTIONS
STALL 282
TRACE DELIVERY ENGINE (TDE)
234
232 TRACE CACHE
TRACE BTB
MICRO-CODE SEQUENCER
236
238
MS UOP QUEUE
230
DECODED INSTRUCTIONS
STALL 282
270
EXECUTION UNIT
FLOATING POINT/MMX EXECUTION ENGINE
274
248
242 SCHEDULER (RESERVATION STATIONS)
244 RENAMER
INTEGER EXECUTION ENGINE
276
REORDER BUFFER (CHECKER)
246 ALLOCATOR
DATA CACHE (LEVEL 0)
278
REPLAY QUEUE
250

FIG. 2

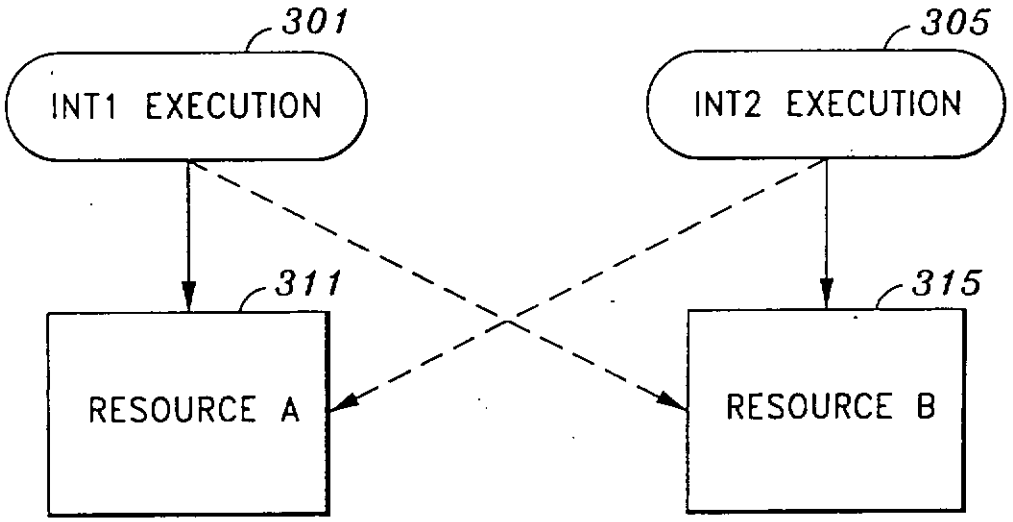

301
INT1 EXECUTION
305
INT2 EXECUTION
311
RESOURCE A
315
RESOURCE B

FIG. 3

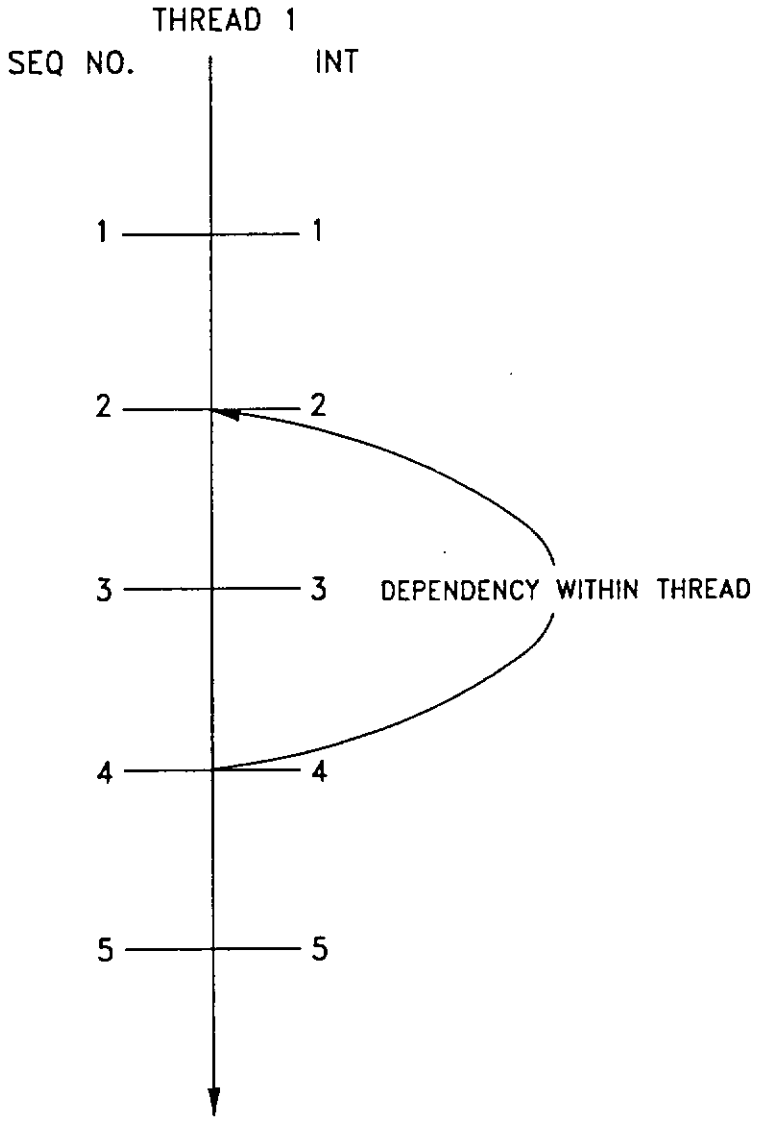



FIG. 4

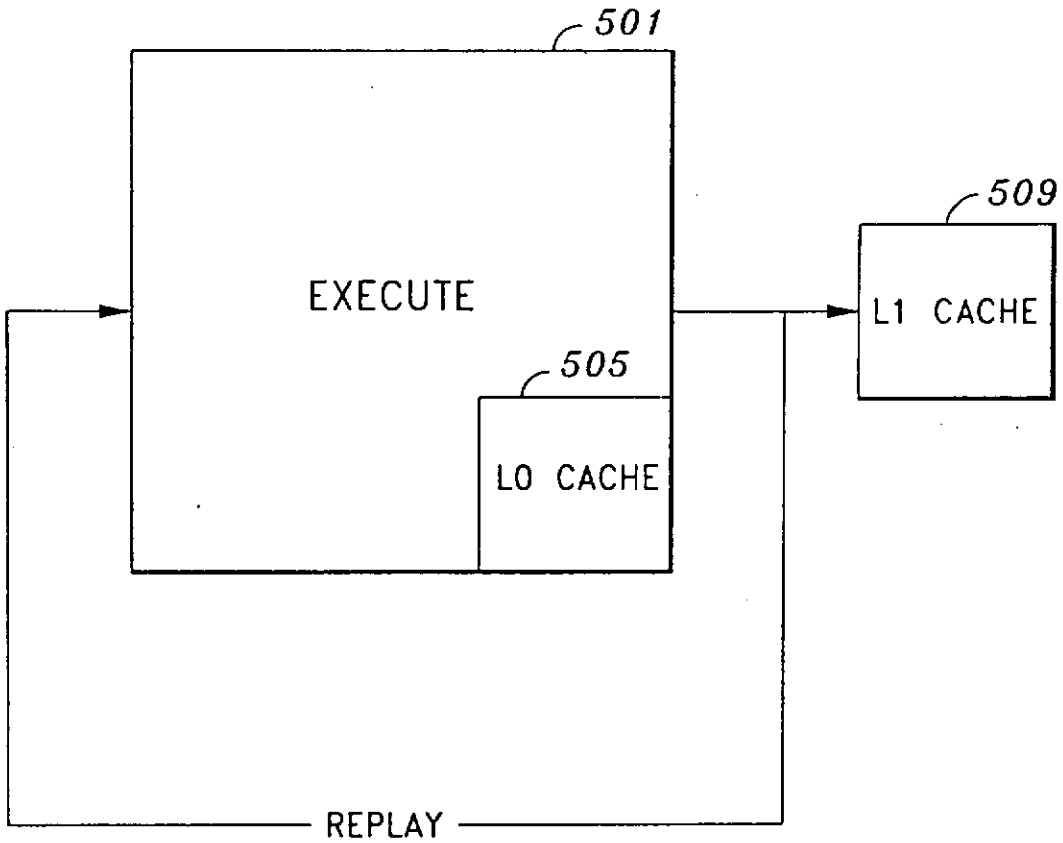



FIG. 5

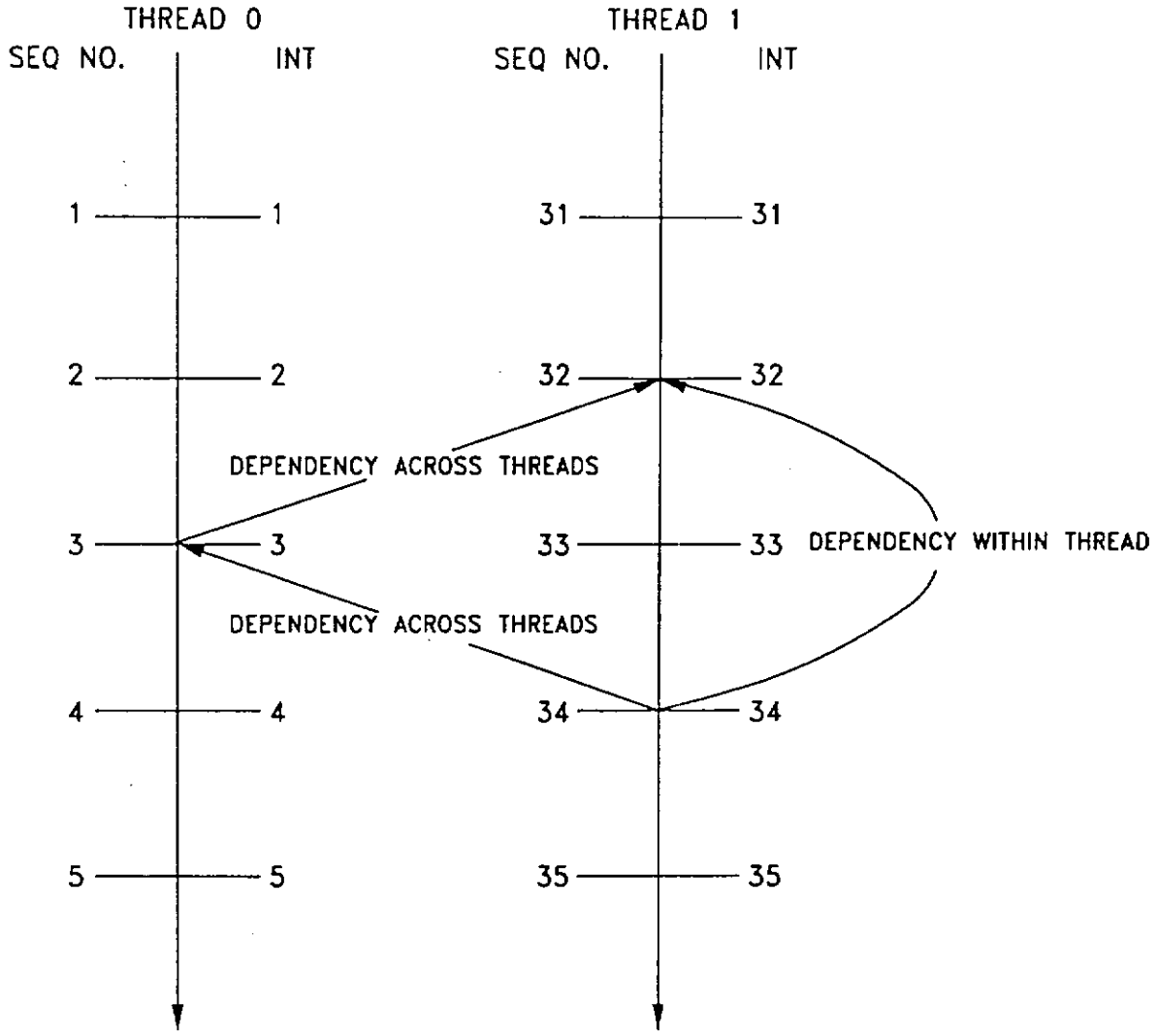

THREAD 0
SEQ NO.
INT
THREAD 1
SEQ NO.
INT
1
1
2
2
3
3
4
4
5
5
31
31
32
32
33
33
34
34
35
35
DEPENDENCY ACROSS THREADS
DEPENDENCY ACROSS THREADS
DEPENDENCY WITHIN THREAD

FIG. 6

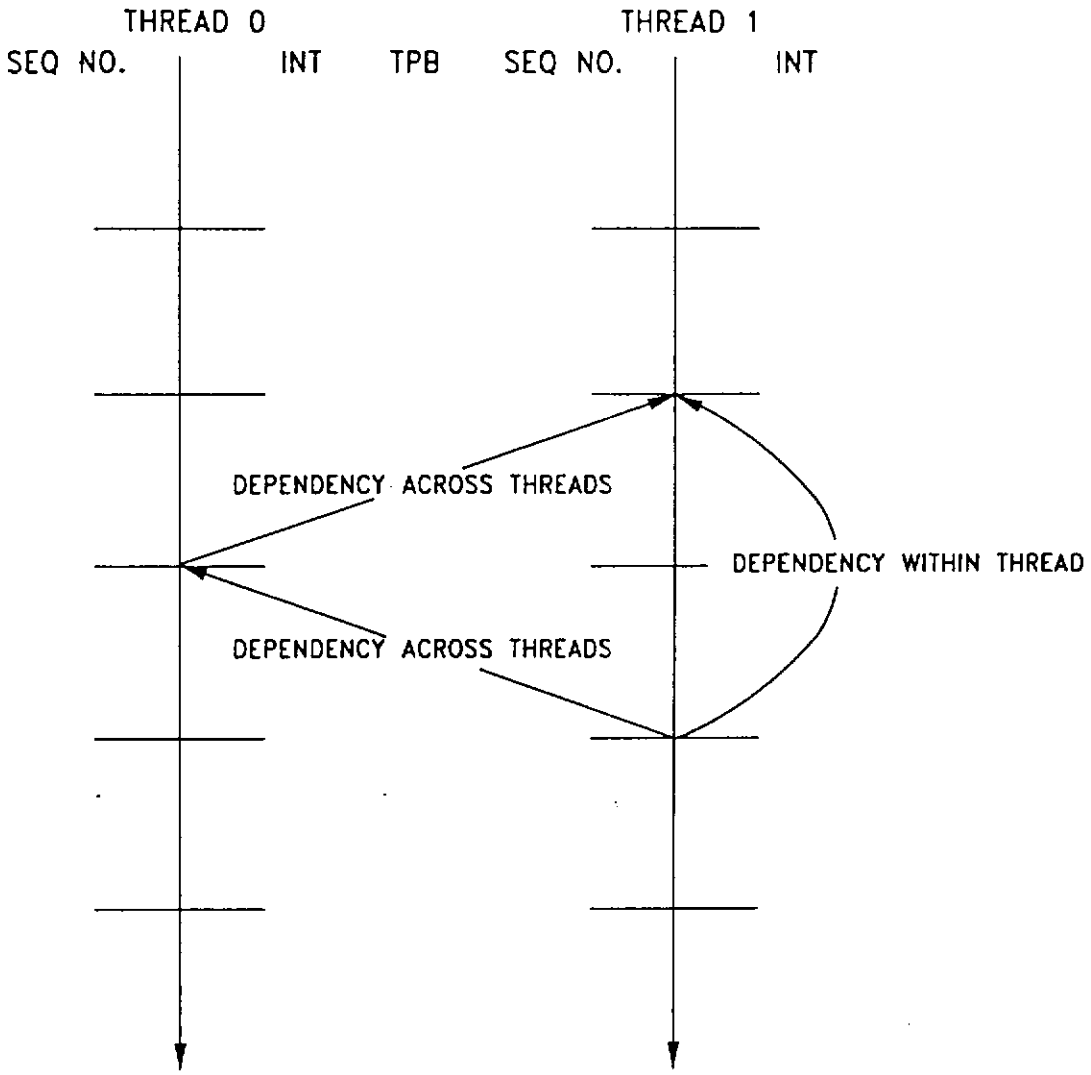

THREAD 0
THREAD 1
SEQ NO.
INT
TPB
SEQ NO.
INT
DEPENDENCY ACROSS THREADS
DEPENDENCY WITHIN THREAD
DEPENDENCY ACROSS THREADS

FIG. 7

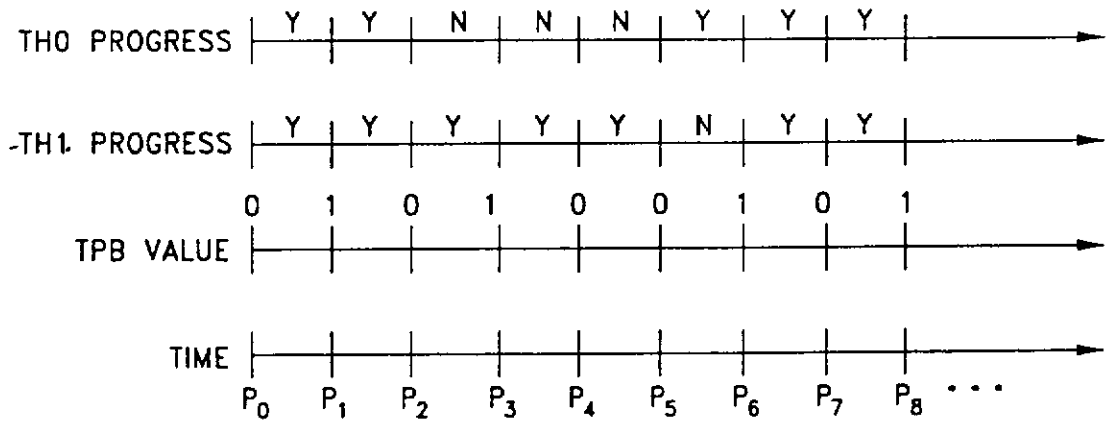

TH0 PROGRESS
Y Y N N N Y Y Y
TH1 PROGRESS
Y Y Y Y Y N Y Y
TPB VALUE
0 1 0 1 0 0 1 0 1
TIME
P0 P1 P2 P3 P4 P5 P6 P7 P8 . . .

FIG. 8

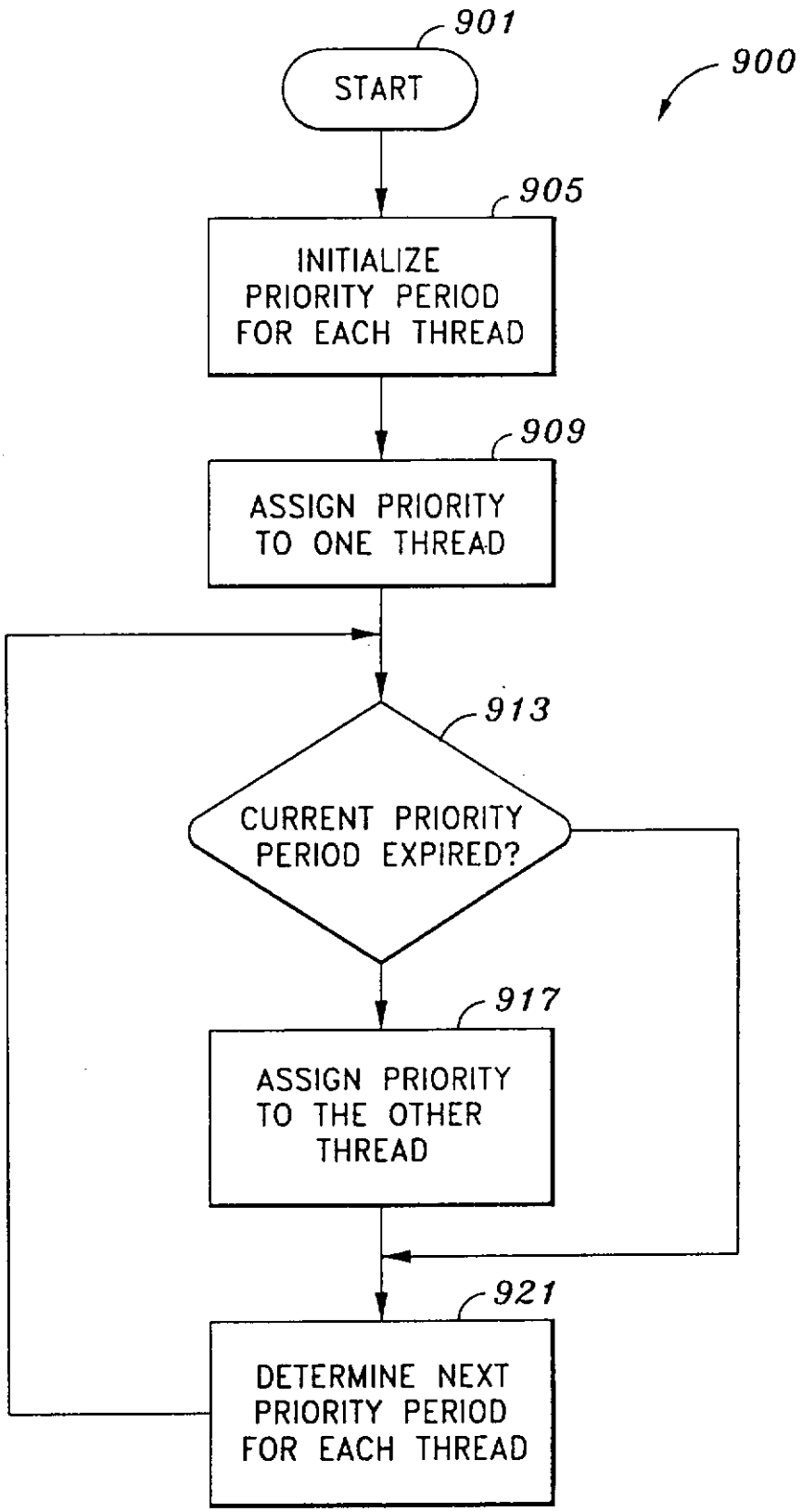

901
START
900
905
INITIALIZE PRIORITY PERIOD FOR EACH THREAD
909
ASSIGN PRIORITY TO ONE THREAD
913
CURRENT PRIORITY PERIOD EXPIRED?
917
ASSIGN PRIORITY TO THE OTHER THREAD
921
DETERMINE NEXT PRIORITY PERIOD FOR EACH THREAD

FIG. 9

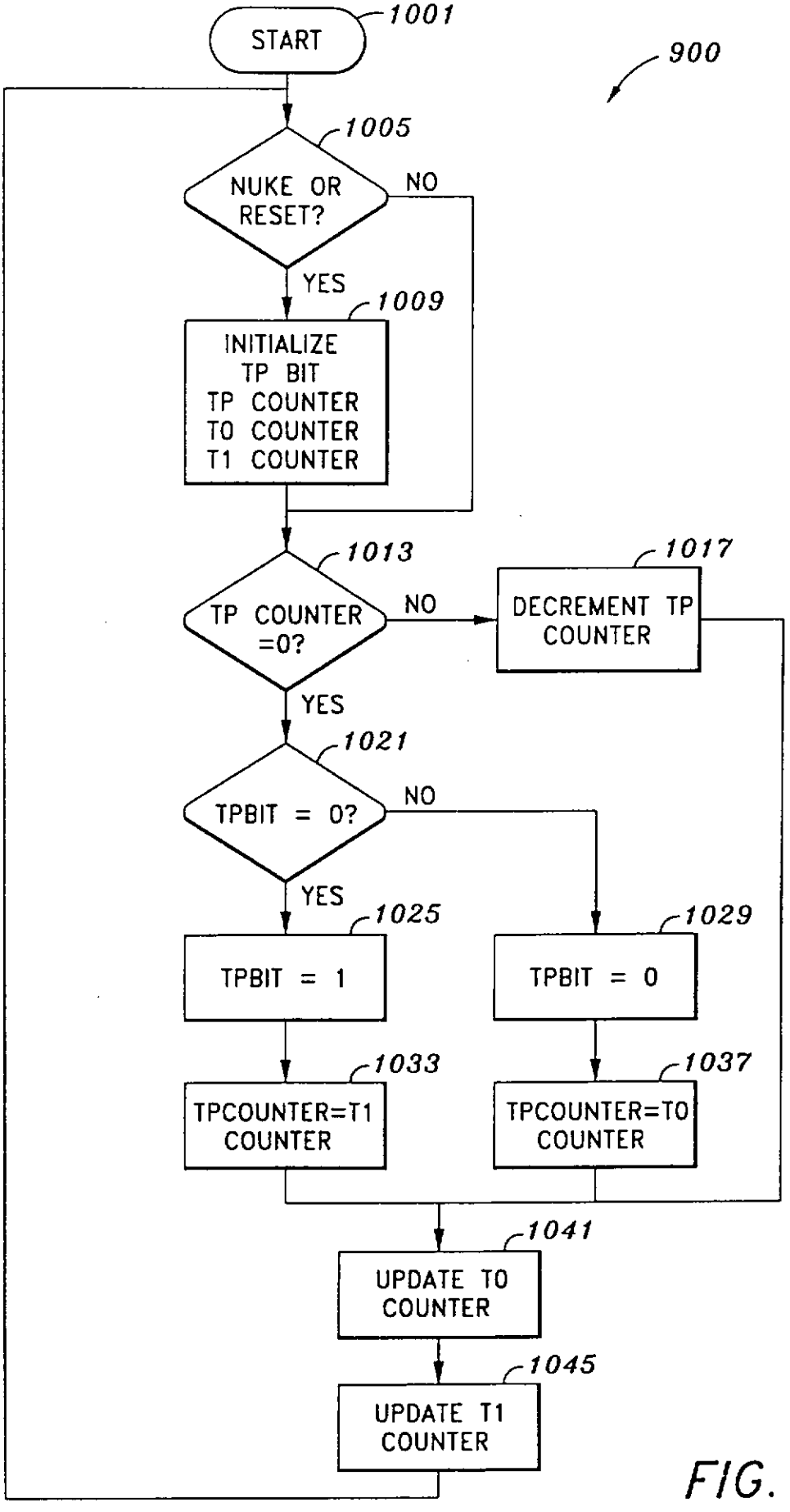

START
1001
900
NUKE OR RESET?
1005
NO
YES
INITIALIZE TP BIT TP COUNTER T0 COUNTER T1 COUNTER
1009
TP COUNTER =0?
1013
NO
DECREMENT TP COUNTER
1017
YES
TPBIT = 0?
1021
NO
YES
TPBIT = 1
1025
TPBIT = 0
1029
TPCOUNTER=T1 COUNTER
1033
TPCOUNTER=T0 COUNTER
1037
UPDATE T0 COUNTER
1041
UPDATE T1 COUNTER
1045

FIG. 10

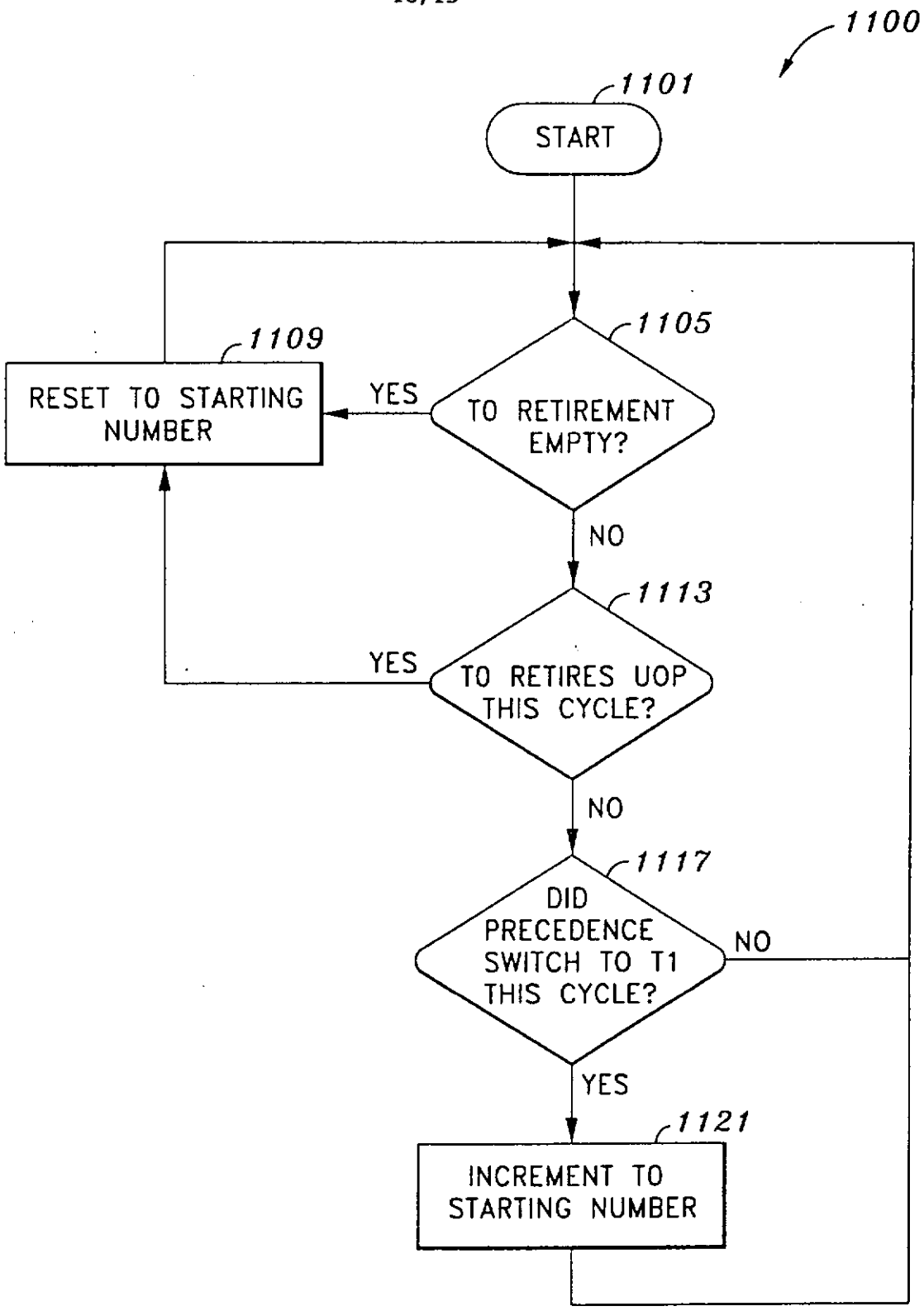

1100
1101
START
1105
TO RETIREMENT EMPTY?
YES
1109
RESET TO STARTING NUMBER
NO
1113
TO RETIRES UOP THIS CYCLE?
YES
NO
1117
DID PRECEDENCE SWITCH TO T1 THIS CYCLE?
NO
YES
1121
INCREMENT TO STARTING NUMBER

FIG. 11

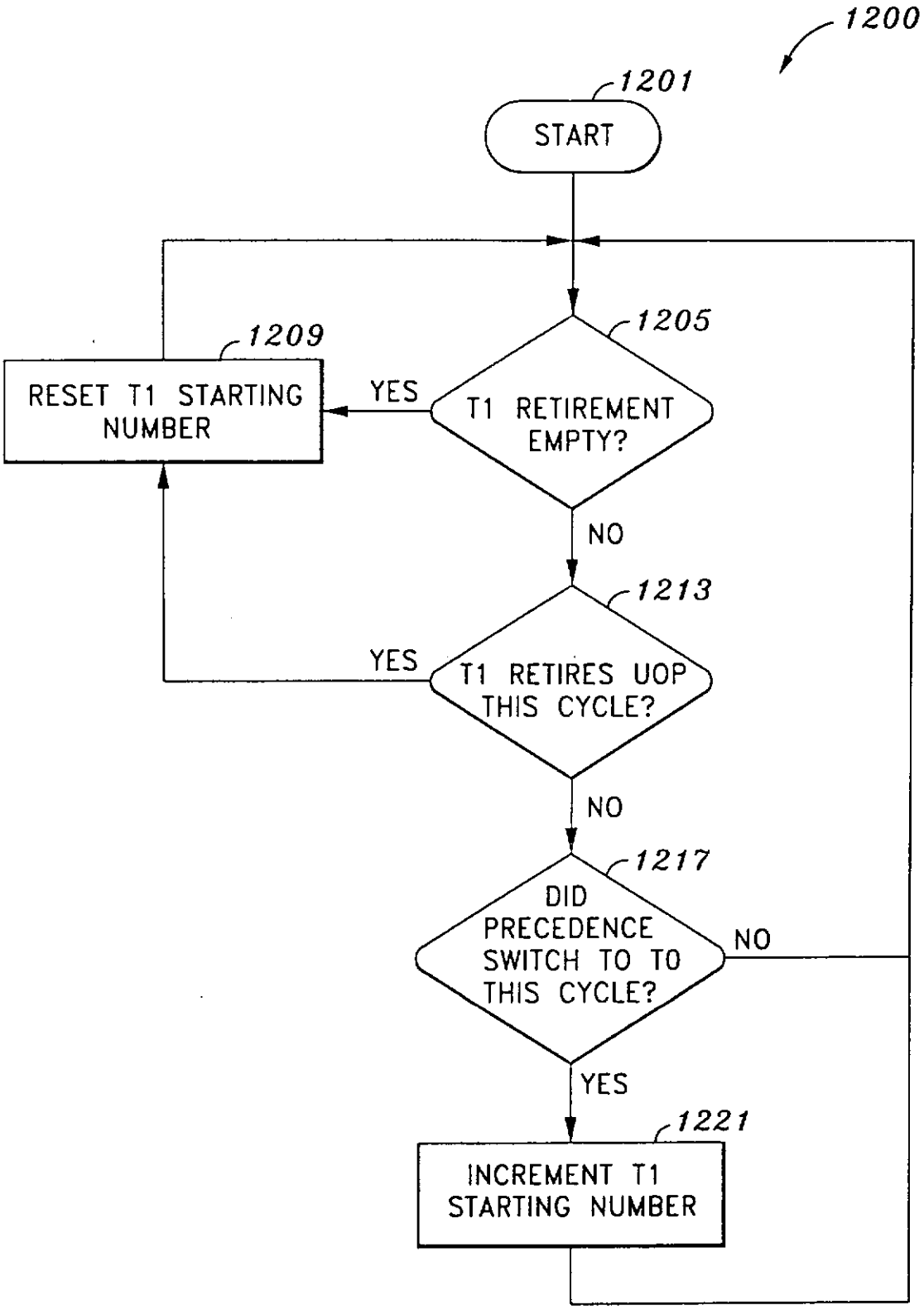

1200
1201
START
1205
T1 RETIREMENT EMPTY?
YES
1209
RESET T1 STARTING NUMBER
NO
1213
T1 RETIRES UOP THIS CYCLE?
YES
NO
1217
DID PRECEDENCE SWITCH TO TO THIS CYCLE?
NO
YES
1221
INCREMENT T1 STARTING NUMBER

FIG. 12

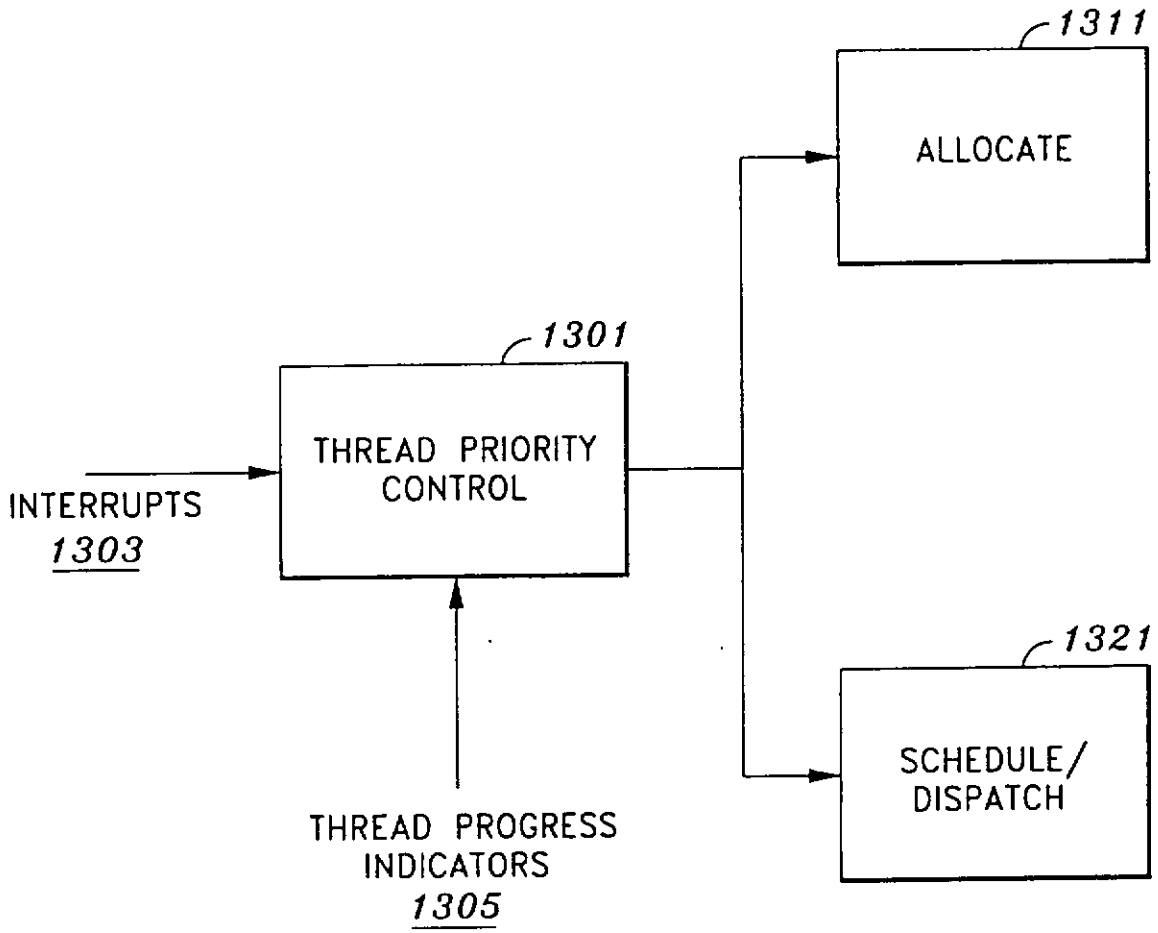

1311
ALLOCATE
1301
THREAD PRIORITY CONTROL
INTERRUPTS
1303
1321
SCHEDULE/ DISPATCH
THREAD PROGRESS INDICATORS
1305

FIG. 13

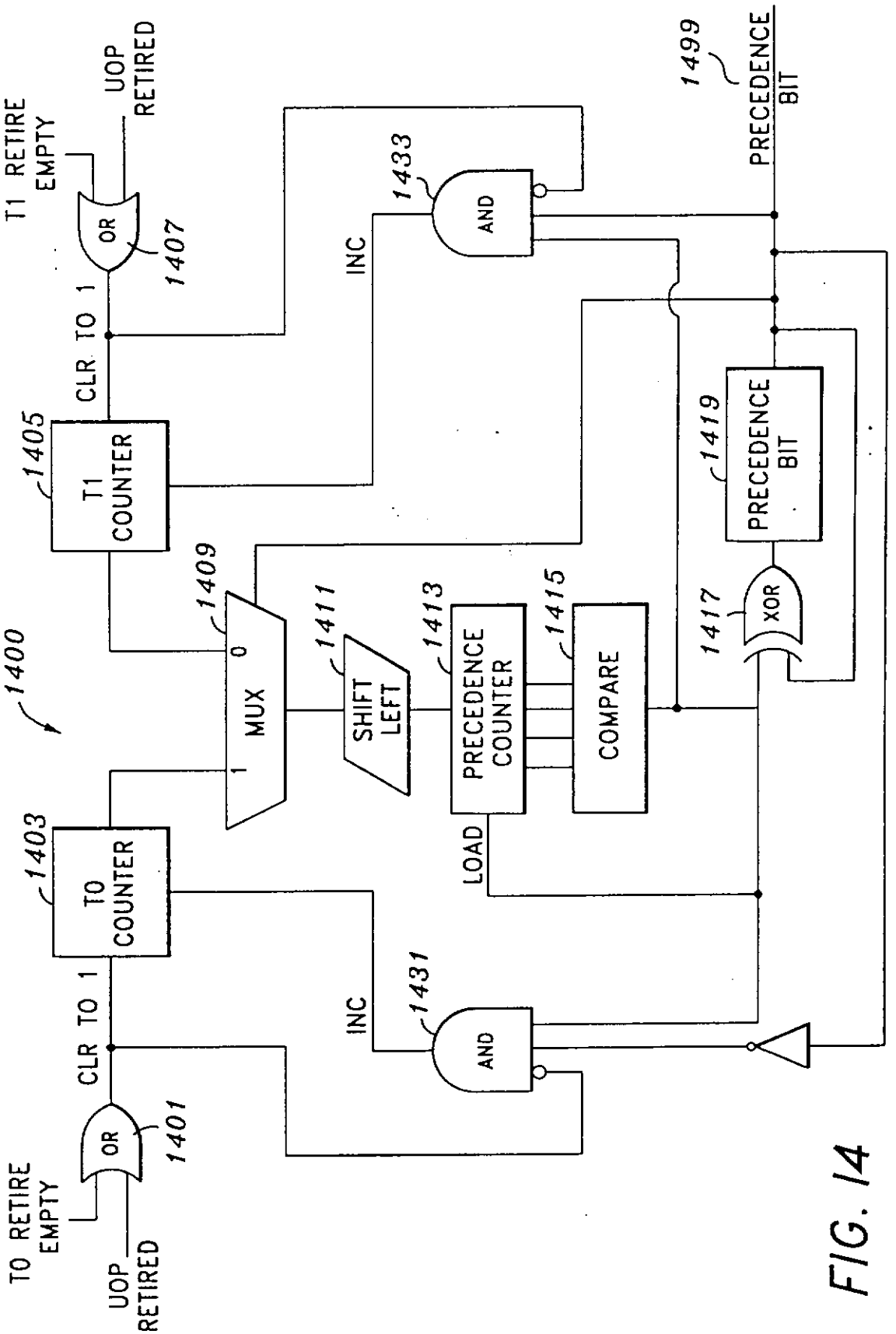

1400
T1 RETIRE EMPTY
UOP RETIRED
OR
1407
CLR TO 1
1405
T1 COUNTER
INC
1433
AND
1499
PRECEDENCE BIT
1409
MUX
0
1
1411
SHIFT LEFT
1413
PRECEDENCE COUNTER
1415
COMPARE
1419
PRECEDENCE BIT
1417
XOR
1403
TO COUNTER
LOAD
CLR TO 1
INC
1431
AND
OR
1401
TO RETIRE EMPTY
UOP RETIRED

FIG. 14