

ABSTRACT

A synchronous bus controller which provides a functional control link between one or more microprocessors and an asynchronous main input/output bus is provided. The bus controller includes a state machine and data bus width determining logic enabling the bus controller to initiate and control access operations between microprocessors and accessible devices on the main input/output bus when the microprocessor and the accessed device may have different data bus widths. The bus controller includes logic circuitry to determine the number of access cycles required to complete a requested access operation and detects the last access cycle of a current access operation to terminate an access operation and provide a ready signal to the microprocessor indicating that the bus controller is ready for the next access request.

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