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ABSTRACT

With the present invention, a synchronous processor circuit can be implemented with a simplified circuit by improving a display's synchronization stability, and by setting a pulse width
5 of a vertical synchronizing signal to be integral multiple of that of the frequency of the horizontal synchronizing signal.

In a synchronous processor circuit in FIG. 1, an LPF 1 receives an externally provided composite signal 5, and a vertical synchronization separating signal 6 is separated therefrom; a 1/2
10 frequency divider circuit 4 outputs a vertical phase detection signal 9 obtained by dividing the frequency synchronization separating signal 6 into 1/2; a phase delay part 2 receives the composite signal 5 and outputs a plurality of horizontal synchronizing signals 19 to 24 each differently delayed in phase;
15 and a vertical synchronizing signal reproduction circuit 3 uses the vertical synchronization separating signal 6 and the plurality of phase-delayed horizontal synchronizing signals 19 to 24 to output a vertical synchronizing signal 8 having the phase relationship determined with respect to the horizontal
20 synchronizing signal.



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