What is Claimed is:

1. A semiconductor package, comprising:

a processor disposed on a substrate;

a first memory including a plurality of first memory chips stacked on the substrate;

an interposer disposed over the processor and the first memory; and

a second memory disposed over the interposer, the second memory including a plurality of second memory chips,

wherein the interposer is disposed between the first memory and the second memory,

wherein the interposer comprises a first physical layer (PHY) transmitting and receiving a signal between the processor and the first memory and transmitting and receiving a signal between the processor and the second memory,

wherein the processor comprises a second PHY communicating with the first PHY,

wherein the processor comprises a first through silicon via (TSV) electrically connecting the first PHY to the second PHY,

wherein each of the plurality of first memory chips comprises:

a first data TSV receiving a data signal, received from the processor, through the first PHY; and

a first power TSV receiving a power signal from a first substrate, and

wherein each of the plurality of second memory chips comprises:

a second data TSV receiving a data signal, received from the processor, through the first PHY; and

a second power TSV receiving the power signal from the first power TSV.

2. The semiconductor package of claim 1, wherein a number of memory chips of the plurality of first memory chips of the first memory is the same as a number of memory chips of the plurality of second memory chips of the second memory.

3. The semiconductor package of claim 1, wherein a number of memory chips of the plurality of first memory chips of the first memory differs from a number of memory chips of the plurality of second memory chips of the second memory.

4. The semiconductor package of any one of claims 1 to 3, wherein the interposer further comprises a power TSV electrically connecting the first power TSV to the second power TSV.

5. The semiconductor package of any one of claims 1 to 4, wherein the interposer further comprises a data TSV electrically connecting the first data TSV to the second data TSV.

6. The semiconductor package of any one of claims 1 to 5, wherein the interposer further comprises:

a second substrate including the first PHY; and

a redistribution layer disposed on the second substrate, and

wherein the redistribution layer comprises:

a first redistribution pattern transferring the data signal between the second data TSV and the first PHY;

a second redistribution pattern transferring the data signal between the first data TSV and the first PHY;

a third redistribution pattern transferring the power signal between the first power TSV and the second power TSV; and

a passivation layer at least partially covering the first redistribution pattern, the second redistribution pattern, and the third redistribution pattern.

7. The semiconductor package of any one of claims 1 to 6, wherein the processor further comprises a second TSV receiving a power signal through the substrate.

8. The semiconductor package of claim 7, wherein the second TSV transfers the power signal to the second power TSV through the interposer.

9. The semiconductor package of any one of claims 1 to 8, wherein the interposer further comprises at least one repeater compensating for loss of signal integrity of the signal.

10. The semiconductor package of any one of claims 1 to 9, wherein the second PHY is disposed in an edge region adjacent to the first memory of the processor.

11. The semiconductor package of claim 10, wherein the first PHY vertically at least partially overlaps the second PHY.

12. The semiconductor package of claim 10 or claim 11, wherein the first TSV is disposed adjacent to the second PHY.

13. The semiconductor package of claim 12, wherein the first PHY at least

partially vertically overlaps the first TSV.

14. A semiconductor package, comprising:

a processor disposed on a substrate;

a lower memory including a plurality of lower memory chips stacked on the substrate;

an upper memory including a plurality of upper memory chips which are vertically stacked; and

an interposer disposed between the lower memory and the upper memory,

wherein the interposer comprises:

a first physical layer (PHY) transmitting and receiving a signal between the processor and the lower memory and transmitting and receiving a signal between the processor and the upper memory;

a power through silicon via (TSV) passing through the interposer, receiving a power signal from the lower memory, and transferring the power signal to the upper memory; and

a data TSV passing through the interposer, receiving a data signal from the lower memory or the upper memory, and transferring the data signal to the first PHY,

wherein the processor comprises:

a second PHY communicating with the first PHY; and

a TSV electrically connecting the first PHY to the second PHY, and

the first PHY vertically overlaps the second PHY.

15. The semiconductor package of claim 14, wherein the interposer further comprises:

an interposer substrate including the first PHY; and

a redistribution layer disposed on the interposer substrate and electrically connecting the first PHY to the data TSV.

16. The semiconductor package of claim 15, wherein the redistribution layer is disposed between the interposer substrate and the upper memory.

17. The semiconductor package of claim 15 or claim 16, wherein the redistribution layer is disposed between the interposer substrate and the lower memory.

18. A semiconductor package, comprising:

a processor disposed on a substrate;

a lower memory including a plurality of lower memory chips vertically stacked on the substrate;

an interposer disposed on the processor and the lower memory; and

a first upper memory disposed on the interposer, the first upper memory including a plurality of upper memory chips that are vertically stacked,

wherein the interposer comprises:

a first physical layer (PHY) electrically connected to the processor, the first upper memory, and the lower memory;

a redistribution layer electrically connecting the lower memory to the first PHY and electrically connecting the first upper memory to the first PHY; and

a power through silicon via (TSV) passing through the interposer, receiving a power signal from the lower memory, and transferring the power signal to the first upper memory,

wherein the processor comprises:

a second PHY communicating with the first PHY;

a first TSV electrically connecting the first PHY to the second PHY; and

a second TSV receiving a power signal from the substrate and transferring the power signal to the power TSV, and

wherein the first PHY at least partially vertically overlaps the second PHY.

19. The semiconductor package of claim 18, wherein

the first upper memory at least partially vertically overlaps the lower memory, and

the semiconductor package further comprises a second upper memory at least partially vertically overlapping the processor on the interposer.