TRI-GATE TRANSISTORS AND METHODS TO FABRICATE SAME

FIELD

[0001] Embodiments of the invention relate generally to the field of integrated circuit device fabrication and more specifically to tri-gate transistor fabrication.

BACKGROUND

[0002] The trend toward increasing the number of functions of an integrated circuit device (IC device) is continuing. As the size of transistors decreases, serious drawbacks in current transistor fabrication processes become evident. For example, typical silicon-on-insulator (SOI) transistors are fabricated by coating a substrate with an insulator (e.g., glass or silicon oxide) layer. A second silicon wafer is then bonded to the insulator layer and thinned to a desired thickness (i.e., as determined by the transistor dimensions). This thinning process is very difficult to control with great accuracy.

[0003] Figures 1A – 1D illustrate a portion of the fabrication process for creating a tri-gate SOI transistor in accordance with the prior art. As shown in Figure 1A, a carrier wafer 101, typically a silicon substrate, has an insulator layer 102, typically silicon dioxide, disposed upon it. For example, a silicon dioxide layer may be grown on a silicon substrate.

[0004] As shown in Figure 1B, a transfer wafer 103 is then bonded to the insulator layer 102, which may facilitate the bonding. The bonding of the carrier wafer to the insulator layer may be effected though a heat-induced hydrogen bonding process. The transfer wafer, which may be, for example, silicon, is approximately 600 microns thick.

[0005] The transfer wafer is then thinned to a desired thickness based upon the transistor dimensions. Typically, this thickness is approximately 50 – 100 nm. The thinning of the transfer wafer may be accomplished through one of several typical

processes. For example, a wet etch and polish process may be used to grind the transfer wafer to the desired thickness. An alternative method for thinning the transfer wafer includes hydrogen implantation of the transfer layer to create a weak section of the transfer wafer. The bonded pair is then heated to effect a high temperature cleave of the hydrogen-doped interface. Subsequently, the transfer wafer surface is polished or treated in other ways to planarize the surface or further reduce the thickness. These methods provide control of the thickness to within approximately several hundred angstroms. As shown in Figure 1C, the transfer wafer 103 has been thinned to a desired dimension for the silicon body of the transistor, resulting in film layer 104. The thickness of film layer 104 is determined by the desired height of the silicon body (H_{Si}). The film layer 104 is then selectively etched to create silicon bodies for the transistors. As shown in Figure 1D, selectively etching the film layer 104, using lithography techniques, results in silicon bodies 105 having a desired body width (W_{Si}) and body height (H_{Si}).

[0006] For typical transistor design architecture, gate length is proportional to H_{Si}, with H_{Si} equal to about one-third of gate length. For typical transistors with gate lengths of approximately 20 – 100 nm, the desired H_{Si} is greater than approximately 20 nm. Using the current fabrication method, it is possible to create adequate film layers. However, as the gate length, and hence, the desired H_{Si} decreases, current fabrication methods exhibit serious disadvantages.

[0007] The H_{Si} value must be uniform across a wafer in order to produce transistors with uniform characteristics. For example, the transistor threshold voltage, which is directly proportional to H_{Si}, should not vary by more than approximately 10%. Therefore, the film layer thickness that determines H_{Si}, should not vary by more than 10%.

[0008] The methods of thinning the transfer layer to obtain the film layer are capable of producing a film layer of approximately 20 nm thickness that does not vary by more

than approximately 10%. However, these methods fail to produce the required uniformity for thinner film layers. Therefore, current methods of fabricating SOI transistors are incapable of yielding transistors with gate lengths smaller than approximately 50 nm.

[0009] Moreover, the process of bonding the carrier wafer and transfer wafer, and the process of thinning the transfer wafer to the desired thickness, are costly and difficult to control.

BRIEF DESCRIPTION OF THE DRAWINGS

[0010] The invention may be best understood by referring to the following description and accompanying drawings that are used to illustrate embodiments of the invention. In the drawings:

[0011] Figures 1A – 1D illustrate a process for creating a tri-gate SOI transistor in accordance with the prior art;

[0012] Figure 2 illustrates a process for providing increased uniformity in silicon body height, H_{Si}, in accordance with one embodiment of the invention; and

[0013] Figures 3A – 3G illustrate the fabrication of a tri-gate transistor in accordance with one embodiment of the invention.

DETAILED DESCRIPTION

[0014] In the following description, numerous specific details are set forth. However, it is understood that embodiments of the invention may be practiced without these specific details. In other instances, well-known circuits, structures and techniques have not been shown in detail in order not to obscure the understanding of this description.

[0015] Reference throughout the specification to "one embodiment" or "an embodiment" means that a particular feature, structure, or characteristic described in connection with the embodiment is included in at least one embodiment of the present invention. Thus, the appearance of the phrases "in one embodiment" or "in an

embodiment" in various places throughout the specification are not necessarily all referring to the same embodiment. Furthermore, the particular features, structures, or characteristics may be combined in any suitable manner in one or more embodiments.

[0016] Moreover, inventive aspects lie in less than all features of a single disclosed embodiment. Thus, the claims following the Detailed Description are hereby expressly incorporated into this Detailed Description, with each claim standing on its own as a separate embodiment of this invention.

[0017] Figure 2 illustrates a process for providing increased uniformity in silicon body height, H_{Si}, in accordance with one embodiment of the invention. Process 200, shown in Figure 2, begins with operation 205 in which a trench layer is disposed upon a substrate layer. For one embodiment, the trench layer may be disposed upon the substrate layer using a chemical vapor deposition (CVD) process. For one embodiment, the substrate layer is silicon. For alternative embodiments, the substrate layer may be another semiconductor material such as germanium (Ge) or gallium arsenide (GaAs). For one embodiment, the trench layer thickness is determined based upon the specification of the transistor's gate length. That is, the trench layer thickness is selected to be equal to a desired H_{Si} value.

[0018] At operation 210, selected portions of the trench layer are removed, thus forming trenches. For one embodiment, the trench layer is a material that can be selectively etched using conventional etching processes. For various alternative embodiments, the trench layer may be multiple layers of different materials with each material. In one such embodiment, the multiple layers of the trench layer are susceptible to different etching processes.

[0019] At operation 215, the trenches formed by operation 210, are filled with a semiconductor material (e.g., silicon). For one embodiment, the trenches are filled with

epitaxial silicon using a selective epitaxial process. In an alternative embodiment, the trenches are filled in some other manner. For example, the trenches may be filled with polysilicon using a blanket deposition process.

[0020] At operation 220, the excess semiconductor material is removed. That is, semiconductor material filling the trench that extends above the surface of the remainder of the trench layer is removed. For one embodiment, a chemical-mechanical polish (CMP) is employed to planarize the surface of the semiconductor material.

[0021] At operation 225, the remainder of the trench layer is removed exposing semiconductor fins (i.e., the semiconductor material filling the trenches). For one embodiment, the height of the semiconductor fins is uniform to within less than 5%.

[0022] Figures 3A – 3G illustrate the fabrication of a tri-gate transistor in accordance with one embodiment of the invention. Figure 3A shows a silicon substrate 301. A multi-layer trench layer is disposed on the silicon substrate 301. The trench layer is comprised of a first oxide (e.g., SiO_2) layer 302, a nitride (e.g., Si_3N_4) layer 303, and a second oxide (e.g., SiO_2) layer 304. Eventually the tri-gate body thickness, H_{Si}, will be determined by the thickness of the second oxide layer, which is a very controllable thickness.

[0023] Figure 3B illustrates the application of a photoresist mask layer 305 to define the transistor bodies. The patterning of the photoresist mask layer 305 determines the width of the silicon body, W_{Si}.

[0024] Figure 3C illustrates the etching of the trench layer to define trenches 306a and 306b. For one embodiment, a series of three distinct dry etch processes are employed. In such an embodiment, the second oxide layer 304 is etched using a selective dry etch process in which the nitride layer 303 acts as an etch stop. Then the nitride layer 303 is etched using a different selective dry etch process in which the first oxide layer 302 acts as

an etch stop. Finally, the first oxide layer 302 is etched using a dry etch process that is sufficiently selective to stop on the surface of the silicon substrate 301.

[0025] Figure 3D illustrates filling trenches 306a and 306b with silicon 307 after the photoresist layer 305 has been stripped away, as indicated. As noted above, the trenches may be filled with silicon through various alternative methods including epitaxial growth or blanket deposition of polysilicon.

[0026] Figure 3E illustrates the silicon 307 planarized to the level of the second oxide layer 304. For one embodiment, the planarization is effected using a CMP process. For one embodiment, the polishing process is used to remove the second oxide layer 304 and the nitride layer 303 is used as a polish stop. For such an embodiment, the polish has a high selectivity between oxide and nitride. For an alternative embodiment, the second oxide layer 304 is selectively etched to the nitride layer 303. Subsequently, the nitride layer 303 is etched using a wet etch process using, for example, phosphoric acid. The first oxide layer 302 acts as an etch stop for such a process.

[0027] Figure 3F illustrates the silicon bodies for the tri-gate transistors exposed with the removal of the trench layer (e.g., second oxide layer 304 and the nitride layer 303). As shown in Figure 3F, a portion of the trench layer (e.g., first oxide layer 302) may be retained to effect beneficial properties of the transistor as explained below. The silicon 307 forming the gate bodies has a uniform height to within a specified tolerance. For one embodiment, the height, H_{Si}, of silicon 307 is approximately 10 nm and is uniform within 5%.

[0028] Figure 3G illustrates the tri-gate transistor fabricated by forming a gate 308 surrounding the silicon 307. The gate 308 may be, for example, metal or another suitable material as known in the art.

GENERAL MATTERS

[0029] Embodiments of the invention include various operations. Many of the methods are described in their most basic form, but operations can be added to or deleted from any of the methods without departing from the basic scope of the invention. For example, the trench layer, described in operation 205 of Figure 2, may be disposed on the substrate in various alternative matters and may be comprised of more than one layer as illustrated in Figure 3A. Furthermore, a portion of the trench layer may be retained to effect benefits. As shown in Figures 3F and 3G, a portion of the first oxide layer is retained to reduce fringe capacitance in the transistor.

[0030] As described above, the trenches formed in the trench layer may be filled with silicon in a number of ways including, for example, blanket deposition of polysilicon. For an embodiment in which a blanket deposition of polysilicon is used, an annealing process is employed after deposition to anneal the silicon into a single crystal.

[0031] While the invention has been described in terms of several embodiments, those skilled in the art will recognize that the invention is not limited to the embodiments described, but can be practiced with modification and alteration within the spirit and scope of the appended claims. The description is thus to be regarded as illustrative instead of limiting.

CLAIMS

What is claimed is:

1. A method comprising:

disposing a trench layer upon a semiconductor substrate;

selectively removing a portion of the trench layer such that a remainder of the trench layer forms one or more trenches, the removal of a portion of the trench layer exposing the semiconductor substrate;

filling the one or more trenches with a semiconductor material;

removing any excess semiconductor material from the one or more trenches; and

removing an additional portion of the trench layer to expose the semiconductor material as one or more semiconductor fins.

2. The method of claim 1 wherein the trench layer is comprised of a plurality of layers.

3. The method of claim 2 wherein the plurality of layers include a first oxide layer disposed upon the semiconductor substrate, a nitride layer disposed upon the first oxide layer, and a second oxide layer disposed upon the nitride layer.

4. The method of claim 3 wherein removing an additional portion of the trench layer comprises removing any remaining portion of the second oxide layer, any remaining portion of the nitride layer, and retaining at least some portion of any remaining portion of the first oxide layer.

5. The method of claim 1 wherein the one or more trenches have a depth of approximately 10 nm.

6. The method of claim 5 wherein the one or more semiconductor fins have a height of approximately 10 nm that is uniform to within 5%.

7. The method of claim 1 wherein removing any excess semiconductor material from the one or more trenches includes planarizing the semiconductor material to a surface of the trench layer.

8. The method of claim 7 wherein the planarizing is effected through a chemical-mechanical polishing process.

9. The method of claim 1 wherein filling the one or more trenches with a semiconductor material includes epitaxially growing the semiconductor material within the one or more trenches.

10. The method of claim 1 wherein filling the one or more trenches with a semiconductor material includes a blanket deposition of semiconductor material.

11. An integrated circuit device comprising:

a substrate; and

one or more transistors formed upon the substrate, each transistor having a semiconductor body, each semiconductor body having a height of less than 20 nm, the

height of each semiconductor body uniform to within a tolerance of 5% of a specified height.

12. The integrated circuit device of claim 11 wherein the one or more transistors are tri-gate transistors.

13. The integrated circuit device of claim 12 wherein each semiconductor body has a height of approximately 10 nm.

14. A method comprising:

disposing a first oxide layer on a semiconductor substrate;

disposing a nitride layer upon the first oxide layer;

disposing a second oxide layer upon the nitride layer;

selectively etching a portion of the second oxide layer and the nitride layer to define one or more trenches;

filling the one or more trenches with a semiconductor material;

removing the excess semiconductor material from the one or more trenches; and

selectively etching a remainder of the second oxide layer and the nitride layer such that one or more semiconductor bodies are formed.

15. The method of claim 14 wherein the one or more trenches have a depth of approximately 10 nm.

16. The method of claim 14 wherein the one or more semiconductor bodies have a height of less than 20 nm that is uniform to within 5%.

17. The method of claim 16 wherein the one or more semiconductor bodies have a height of approximately 10 nm.

18. The method of claim 14 wherein removing any excess semiconductor material from the one or more trenches includes planarizing the semiconductor material to a surface of the second oxide layer.

19. The method of claim 18 wherein the planarizing is effected through a chemical-mechanical polishing process.

20. The method of claim 14 wherein filling the one or more trenches with a semiconductor material includes epitaxially growing the semiconductor material within the one or more trenches.

21. The method of claim 14 wherein filling the one or more trenches with a semiconductor material includes a blanket deposition of semiconductor material.

22. The method of claim 14 wherein the semiconductor substrate is comprised of a semiconductor material selected from the group consisting of silicon, germanium, and gallium arsenide.

23. The method of claim 14 wherein the semiconductor substrate is comprised of silicon, the first oxide layer is comprised of SiO_2, the nitride layer is comprised of Si_3N_4, and the second oxide layer is comprised of SiO_2.