HIGH SHRINKAGE STRESS SILICON NITRIDE (SiN) LAYER FOR NFET IMPROVEMENT

ABSTRACT

A method (and semiconductor device) of forming a high shrinkage stressed silicon nitride layer for use as a contact etch stop layer (CESL) or capping layer in a stress management technique (SMT) provides increased tensile stress to a channel of an nFET device to enhance carrier mobility. A spin-on polysilazane-based dielectric material is applied to a semiconductor substrate and baked to form a film layer. The film layer is cured to remove hydrogen from the film which causes shrinkage in the film when it recrystallizes into silicon nitride. The resulting silicon nitride stressed layer introduces an increased level of tensile stress to the transistor channel region.

FIG. 2B