Patent claims:

1. A method for producing a monolithic template comprising a Si wafer with a layer of a III/V semiconductor epitaxially applied on a surface of the Si wafer, the III/V semiconductor having a lattice constant, which differs by less than 10% from that of Si, comprising the following steps:

A) optionally, the surface of the Si wafer is deoxidized,

B) optionally, a Si layer is epitaxially grown on the surface of the deoxidized Si wafer,

C) optionally, the surface of the Si wafer or the surface of the Si layer is subjected to an etching step and/or a baking-out step,

D) a layer of a III/V semiconductor is epitaxially grown on the surface of the Si wafer or a surface formed during one of steps A) to C) at a wafer temperature from 350 to 650 °C, a growth rate from 0.1 to 2 µm/h, and a layer thickness from 1 to 100 nm,

E) a layer of a III/V semiconductor, identically with or differently from the III/V semiconductor applied in step D), is epitaxially grown on the layer obtained in step D) at a wafer temperature from 500 to 800 °C, a growth rate from 0.1 to 10 µm/h, and a layer thickness from 10 to 150 nm.

2. The method according to claim 1, wherein the surface of the Si wafer is a (001) Si surface,

with 0 to 6° in the direction <110>, wherein at a dislocation of ≤ 1° the direction of the dislocation can differ from <110>.

3. The method according to claim 1 or 2, wherein step A) is carried out by baking-out to a wafer temperature from 800 to 1,200 °C for a time from 1 s to 30 min in an inert gas atmosphere.

4. The method according to one of claims 1 to 3, wherein in step B) the Si layer is grown at a wafer temperature from 600 to 1,200 °C, a growth rate from 0.01 to 20 µm/h, and a layer thickness from 0 to 5 µm.

5. The method according to one of claims 1 to 4, wherein in step C) an active gas, in particular a Cl-containing gas and/or hydrogen, is conducted over the surface at a wafer temperature from 600 to 1,200 °C for a time from 0 to 60 min at an etching rate from 0 to 5 µm/h, and/or an inert gas is conducted over the surface at a wafer temperature from 600 to 1,200 °C for a time from 0 to 60 min.

6. The method according to one of claims 1 to 5, wherein in step D) a $Ga_xB_yAl_zP$ or a GaN_wP_v semiconductor is grown, wherein x = 0 - 1, y = 0 - 0.1 and z = 0 - 1, or w = 0 - 0.1 and v = 1 - w, wherein the sum of x, y and z for $Ga_xB_yAl_zP$ is always 1.

7. The method according to one of claims 1 to 6, wherein in step E) a $Ga_xB_yAl_zP$ or a GaN_wP_v semiconductor is grown, wherein x = 0 - 1, y = 0 - 0.1 and z = 0 - 1, or w = 0 - 0.1 and v = 1 - w, wherein the sum of x, y and z for $Ga_xB_yAl_zP$ is always 1.

8. A monolithic template, obtainable by means of a method according to one of claims 1 to 7.

9. The use of a template according to claim 8 for the monolithic integration of III/V-based semiconductor components such as transistors, laser diodes, LEDs, detectors, and solar cells on a Si substrate, in particular on a Si substrate, optionally with a mask structure having a diameter of more than 6 cm, preferably more than 10 cm, in particular more than 20 cm.

10. The use according to claim 9, wherein subsequently to step E), further III/V semiconductor layers are epitaxially grown, and electronic components comprising III/V semiconductor are formed.

Claims:

1. A method for producing a monolithic template comprising a Si wafer with a layer of a III/V semiconductor epitaxially applied on a surface of the Si wafer, the III/V semiconductor having a lattice constant, which differs by less than 10% from that of Si, comprising the following steps:

A) the layer of the III/V semiconductor is epitaxially grown on the surface of the Si wafer at a wafer temperature from 350 to 650 °C, a growth rate from 0.1 to 2 µm/h, and a layer thickness from 1 to 100 nm wherein the layer deposited in this step is deposited by Atomic Layer Deposition (ALD),

B) a layer of a III/V semiconductor, identically with or differently from the III/V semiconductor applied in step A), is epitaxially grown on the layer obtained in step A) at a wafer temperature from 500 to 800 °C, a growth rate from 0.1 to 10 µm/h, and a layer thickness from 10 to 150 nm.

2. The method according to claim 1, further including an etching step (before step A), wherein a Cl-containing gas is conducted over the surface at a wafer temperature from 600 to 1,200 °C for a time from 0 to 60 min at an etching rate from 0 to 5 µm/h.

3. The method according to claim 2, wherein prior to the etching step, the method further includes a deoxidizing step whereby the surface of the Si wafer is deoxidized, by tempering the wafer at a temperature from 800

to 1,200 °C for a time from 1 s to 30 min in an inert gas atmosphere.

4. The method according to claim 3, wherein prior to the etching step and after the deoxidizing step, a Si layer is epitaxially grown on the surface of the deoxidized Si wafer at a wafer temperature from 600 to 1,200 °C, at a growth rate from 0.01 to 20 µm/h, and wherein the layer thickness is from 0 to 5 µm.

5. The method according to any one of claims 1 to 4, wherein the surface of the Si wafer is a (001) Si surface, with 0 to 6° misorientation in the direction <110>, wherein at a dislocation of ≤ 1° the direction of the dislocation can differ from <110>.

6. The method according to any one of claims 1 to 5, wherein in step A) the III/V semiconductor is a $Ga_xB_yAl_zP$ semiconductor, wherein x = 0 - 1, y = 0 - 0.1 and z = 0 - 1, wherein the sum of x, y and z is always 1.

7. The method according to any one of claims 1 to 5, wherein in step A) the III/V semiconductor is a GaN_wP_v semiconductor, wherein w = 0 - 0.1 and v = 1 - w.

8~~7~~. The method according to any one of claims 1 to 6, wherein in step B) the III/V semiconductor is a $Ga_xB_yAl_zP$ semiconductor, wherein x = 0 - 1, y = 0 - 0.1 and z = 0 - 1, wherein the sum of x, y and z is always 1.

9. The method according to any one of claims 1 to 7, wherein in step B) the III/V

semiconductor is a GaN_wP_v semiconductor, wherein w = 0 - 0.1 and v = 1 - w.

10. The method according to any one of claims 1 to 9, wherein in step B) doping with Zn, Te, S, C, Mg and/or Si takes place in a p- or n-doping concentration of 10^{15} to 10^{21} cm^{-3}.

11. The method according to any one of claims 1 to 10, wherein in step B) doping with Zn, Te, S, C, Mg and/or Si takes place in a p- or n-doping concentration of 10^{15} to 10^{21} cm^{-3}.

12. The method according to any one of claims 1-11, wherein the Substrate has a diameter of 6 cm.

13. The method according to any one of claims 1-11, wherein the Substrate has a diameter of 10 cm.

14. The method according to any one of claims 1-11, wherein the Substrate has a diameter of 20 cm.

15. A monolithic template on Si substrate with an epitaxially grown layer of a III/V semiconductor on a suface of the Si substrate, obtainable by means of a method according to any one of claims 1 to 14.

16. The use of a template according to claim 15 in the manufacture of monolithic integration of III/V-based semiconductor components such as transistors, laser diodes, LEDs, detectors, and solar cells on a Si substrate, in particular on a Si substrate

17. The use according to claim 16, wherein subsequently to step B), further III/V semiconductor layers are epitaxially grown, and electronic components comprising III/V semiconductor are formed.