WHAT IS CLAIMED IS:

1. A semiconductor memory device, comprising:

a first data input/output (I/O) pad to receive a test signal;

an X-ray detector connected to the first data I/O pad, the X-ray detector including a bipolar junction transistor (BJT) having a voltage between an input end and an output end that changes according to a cumulative X-ray dosage to the semiconductor memory device, the X-ray detector to generate a test result signal indicating the voltage between the input and output ends of the BJT based on the test signal; and

a second data I/O pad connected to the X-ray detector and to output the test result signal.

2. The semiconductor memory device as claimed in claim 1, wherein the BJT is an NPN BJT that includes:

a first N-type semiconductor region connected to an emitter electrode;

a P-type semiconductor region connected to a base electrode, a second N-type semiconductor region connected to a collector electrode;

a first junction between the first N-type semiconductor region and the P-type semiconductor region; and

a second junction between the P-type semiconductor region and the second N-type semiconductor region.

3. The semiconductor memory device as claimed in claim 2, wherein the voltage between the input and output ends of the BJT increases as the cumulative X-ray dosage increases.

4. The semiconductor memory device as claimed in claim 2 or claim 3, wherein the voltage between the input and output ends of the BJT is a voltage between the collector electrode and the emitter electrode of the NPN BJT.

5. The semiconductor memory device as claimed in claim 1, wherein the BJT is a PNP BJT that includes:

a first P-type semiconductor region connected to an emitter electrode;

an N-type semiconductor region connected to a base electrode;

a second P-type semiconductor region connected to a collector electrode;

a first junction between the first P-type semiconductor region and the N-type semiconductor region; and

a second junction between the N-type semiconductor region and the second P-type semiconductor region.

6. The semiconductor memory device as claimed in claim 1, wherein the X-ray detector further includes:

a current source to generate a first current applied to a collector electrode of the BJT based on the test signal; and

a voltage measurer to generate the test result signal based on a voltage between the collector electrode and an emitter electrode of the BJT when the first current is applied to the collector electrode of the BJT.

7. The semiconductor memory device as claimed in claim 6, wherein a level of the first current generated from the current source is fixed.

8. The semiconductor memory device as claimed in any one of claims 1 to 7, further comprising a memory cell array connected to the first data I/O pad and the second data I/O pad, the memory cell array including a plurality of memory cells.

9. The semiconductor memory device as claimed in claim 8, wherein:

the memory cell array is to store first data based on a first data signal received from at least one of the first and second data I/O pads or to output stored second data as a second data signal through the at least one of the first and second data I/O pads during a first operation mode, and

the X-ray detector is to generate the test result signal based on the test signal received from the first data I/O pad and to output the test result signal through the second data I/O pad during a second operation mode.

10. The semiconductor memory device as claimed in claim 9, wherein:

the memory cell array is disabled during the second operation mode, and

the X-ray detector is disabled during the first operation mode.

11. The semiconductor memory device as claimed in claim 9 or claim 10, wherein one of the first operation mode and the second operation mode is selected based on a command received from an external device.

12. The semiconductor memory device as claimed in any one of claims 8 to 11, wherein:

the memory cell array is in a memory area on a semiconductor substrate, and

the X-ray detector is in a peripheral area surrounding the memory area on the semiconductor substrate.

13. The semiconductor memory device as claimed in any one of claims 1 to 12, further comprising a delay circuit to receive at least one signal and to delay the at least one signal, wherein the X-ray detector is included in the delay circuit.

14. The semiconductor memory device as claimed in any one of claims 1 to 12, further comprising:

a ring oscillator to generate an oscillation signal, and

wherein the X-ray detector is included in the ring oscillator.

15. The semiconductor memory device as claimed in any one of claims 1 to 14, wherein the semiconductor memory device is a dynamic random access memory (DRAM).

16. An X-ray detector, comprising:

a current source connected to a first data input/output (I/O) pad of a semiconductor memory device, the current source to generate a first current based on a test signal received from the first data I/O pad;

a bipolar junction transistor (BJT) connected to the current source, the BJT including an emitter electrode, a base electrode, and a collector electrode to which the first current is applied; and

a voltage measurer connected to the BJT and a second data I/O pad of the semiconductor memory device, the voltage measurer to generate a test result signal based on a voltage between the collector electrode and the emitter electrode of the BJT, and to output the test result signal through the second data I/O pad when the first current is applied to the collector electrode of the BJT,

wherein the voltage between the collector electrode and the emitter electrode of the BJT changes according to a cumulative X-ray dosage to the semiconductor memory device.

17. The X-ray detector as claimed in claim 16, wherein the voltage between the collector electrode and the emitter electrode of the BJT increases as the cumulative X-ray dosage increases.