LED STRUCTURE AND FABRICATION PROCESSES THEREOF

BACKGROUND

Field

[0001] Embodiments of the present disclosure generally relate to devices and methods of fabricating devices.

Description of the Related Art

[0002] Light emitting diode (LED) devices use an array of LEDs with individual LEDs that are individually controllable. Such a device can be used for a computer, touch panel device, personal digital assistant (PDA), cell phone, television monitor, photodiodes and the like. LED devices that use micron-scale LEDs based on III-V semiconductor technology (also called micro-LEDs) would have a variety of advantages as compared to organic light emitting diodes (OLEDs), e.g., higher energy efficiency, brightness, and lifetime, as well as fewer material layers in the display stack which can simplify manufacturing. However, there are challenges to fabrication of micro-LED devices. Accordingly, what is needed in the art are LED devices and methods of fabricating LED devices.

SUMMARY

[0003] In on embodiment, a device is provided. The device includes a light-emitting diode (LED) panel and a photodetector array. The LED panel including a backplane including backplane electrodes disposed in or on the backplane, a plurality of LEDs each including an LED electrode wherein the backplane electrodes are coupled to the LED electrodes, and a reflective layer disposed on sidewalls of each LED. The photodetector array include a plurality of photodetectors.

[0004] In another embodiment, a device is provided. The device includes a backplane, a plurality of LEDs, a plurality of photodetectors, and a reflective layer. The backplane including backplane electrodes disposed on or in the backplane. Each LED including an LED electrode, each LED electrode is coupled to a respective backplane electrode. Each photodetector including a detector electrode, each detector electrode is coupled to the respective backplane electrode. The reflective layer a detector electrode, each detector electrode is coupled to the respective backplane electrode.

[0005] In yet another embodiment, a method is provided. The method including: bonding a plurality of LEDs to a backplane, each LED including a reflective layer disposed on sidewalls of each LED and an LED electrode, wherein the plurality of LEDs are coupled to backplane electrodes on or in the backplane, forming a subpixel isolation (SI) structure layer disposed on an upper surface of the plurality of LEDs, and patterning the SI structure layer to form a plurality of SI structures defining wells above each LED.

BRIEF DESCRIPTION OF THE DRAWINGS

[0006] FIG. 1A is a schematic, cross-sectional view of an interconnect device according to embodiments.

[0007] FIG. 1B is a schematic, cross-sectional view of a interconnect device according to embodiments.

[0008] FIGS. 2A-2C are schematic, cross-sectional views of an LED panel according to embodiments.

[0009] FIG. 3 a flow diagram of a method of fabricating an LED panel according to embodiments.

[0010] FIGS. 4A-4J are schematic, cross-sectional views of a backplane during a method for forming an LED panel according to some embodiments.

[0011] FIG. 5 is a cross-sectional view of an LED panel according to embodiments.

[0012] FIG. 6 is a flow diagram of a method of fabricating an LED panel according to embodiments.

[0013] FIGS. 7A-7E are schematic, cross-sectional views of a backplane during a method of fabricating an LED panel according to embodiments.

[0014] FIG. 8 is a flow diagram of a method of fabricating an LED panel according to embodiments.

[0015] FIGS. 9A-9C are schematic, cross-sectional views of a backplane during a method of fabricating an LED panel according to embodiments.

[0016] To facilitate understanding, identical reference numerals have been used, where possible, to designate identical elements that are common to the figures. It is contemplated that elements and features of one embodiment may be beneficially incorporated in other embodiments without further recitation.

DETAILED DESCRIPTION

[0017] Embodiments of the present disclosure generally relate to devices and methods of fabricating devices. The device includes a light-emitting diode (LED) panel and a photodetector array. The LED panel including a backplane including backplane electrodes disposed in or on the backplane, a plurality of LEDs each including an LED electrode wherein the backplane electrodes are coupled to the LED electrodes, and a reflective layer disposed on sidewalls of each LED. The photodetector array include a plurality of photodetectors.

[0018] FIG. 1A is a schematic, cross-sectional view of an interconnect device 100a. The interconnect device 100a may be a photonic interconnect device. A photonic interconnect device is a component that allows for high-density communication between a microprocessor system and memory. In some embodiments, the integrated circuit includes one interposer 101. In some embodiments, the integrated circuit includes at least two separate interposers 101 with various electrical devices disposed thereon. In some embodiments, the interposer 101 is made of silicon. However, it is also contemplated that the interposer 101 may also be made of an organic material. The interconnect device 100a includes an application-specific integrated circuit (ASIC) 102 disposed on each interposer 101. In addition to the ASIC 102, each interposer 101 also includes an LED panel disposed thereon. The LED panel 200 includes a plurality of LEDs 204 disposed on a backplane 205. The LEDs 204 may be micro-LEDs (hereinafter, “micro-LEDs”). The LEDs 204 described herein in this disclosure are LEDs or Micro-LEDs. In some embodiments, the plurality of LEDs 204 is disposed in an array on the backplane 205. Further, a transimpedance amplifier (TIA) 106 is disposed on each interposer 101. An array of photonic detectors (or “photodetectors”) 207 are disposed on the TIA 106 to form a photodetector array. Each photodetector 207 disposed on one of the interposers 101 is coupled to a corresponding LED 204 disposed on a different interposer 101 of the interconnect device 100a. The photodetectors 207 may be coupled to the LEDs 204 via at least one of a waveguide or an optical fiber bundle 108. In some embodiments,

the photodetectors 207 may be directly deposited between the LEDs 204 on the backplane 205, as shown in FIG. 1B. Thus, rather than connecting the LEDs 204 to a different backplane or TIA 106 with photodetectors 207, the LEDs 204 connect to the photodetectors 207 via the same backplane 205. In some embodiments, each photodetector 207 may be disposed between LEDs 204 on the same backplane 205, as illustrated in FIG. 1B.

[0019] FIG. 1B is a schematic, cross-sectional view of a interconnect device 100b. The interconnect device 100b includes an LED panel 200 with photodetectors 207 disposed between the LEDs 204 on the same backplane 205. The interconnect device 100b may further include an optical fiber bundle 108.

[0020] The LED panel 200 includes the backplane 205. The backplane 205 can include one or more backplane electrodes 213. The backplane 205 can further include one or more integrated circuits, such as driver circuits 209 and transimpedance amplifiers (TIAs) 210. In some embodiments, the backplane 205 includes an electrode layer 211 and an integrated circuit layer 212. The electrode layer 211 is disposed on top of the integrated circuit layer 212. The electrode layer 211 includes the backplane electrodes 213. In some embodiments, the backplane electrodes 213 are disposed in the backplane 205, as illustrated in FIG. 1B. In some embodiments, the backplane electrodes 213 are disposed on the backplane 205. The integrated circuit layer 212 includes the one or more integrated circuits.

[0021] A plurality of LEDs 204 are coupled to the backplane electrodes 213 by LED electrodes 214. The LEDs 204 may be micro-LEDs (hereinafter, “micro-LEDs”). A plurality of photodetectors 207 can also be coupled to the backplane electrodes 213 by photodetector electrodes 215. In some embodiments, the interconnect device 100b may further include SI structures 216 disposed between the LEDs 204 and the photodetectors 207. The optical fiber 108 is configured to receive light emitted from the LEDs 204 and transmit light to the photodetectors 207 on the same backplane 205. A reflective layer 222 is formed over the sidewalls of the LEDs 204. The reflective layer 222 disposed on the sidewalls of the LEDs 204 is reflective to reduce and/or eliminate cross talk between the LEDs 204 and the photodetectors 207. The reflective layer 222 includes a reflective metal. The reflective layer 222 including the

reflective metal has a reflectivity of greater than 90%. The reflective metal includes, but is not limited to, aluminum, silver, gold, copper, or combinations thereof.

[0022] FIGs. 2A-2C are schematic, cross-sectional views of an LED panel 200. In some embodiments, the LED panel 200 includes an arrangement 216a of SI structures 216, as shown in FIGs. 2B and 2C. In some embodiments, the LED panel 200 does not include SI structures 216 as shown in FIG. 2A. In some embodiments, the LED panel 200 includes color conversion materials 218 disposed in wells 219 between the SI structures 216, as shown in FIG. 2C.

[0023] The LED panel 200 includes LEDs 204. Although illustrated as only having LEDs 204, it is understood that the LED panel 200 may include photodetectors 207 similar to what is illustrated in FIG. 1B. The LEDs 204 may be LEDs or micro-LEDs (hereinafter “micro-LEDs”). Micro-LEDs has diameters ranging from 1 micrometer (μm) to 100 μm. The LED panel 200 may be fabricated on a backplane 205. The backplane 205 can include a backplane surface 205a. The backplane surface 205a can include one or more pairs of backplane electrodes 213 disposed thereon. A plurality of LEDs 204 can be coupled to the pairs of backplane electrodes 213 disposed on the backplane 205. In some embodiments, a first backplane electrode and a second backplane electrode, can be coupled to a micro-LED via the backplane surface 205a, via a lateral chip or “flip-chip” configuration. Although the figures may illustrate a lateral chip or "flip-chip" configuration, other embodiments may mount the first backplane electrodes to the backplane surface 205a while mounting the second backplane electrode to an opposite side of the micro-LED, referred to as a "vertical-chip" orientation, which is compatible with the all the embodiments described herein that utilize a reflective layer and/or dielectric material.

[0024] In some embodiments, the LEDs 204 include can at least one LED electrode 214 coupled to at least one backplane electrode 213 disposed on or in the backplane 205. The LEDs 204 may be Patterned Sapphire Substrate (PSS) micro-LEDs or planar micro-LEDs. The LEDs 204 of the LED panel 200 are depicted as planar micro-LEDs. The PSS micro-LEDs and planar micro-LEDs can be interchangeable in the LED panel 200.

[0025] In some embodiments, a dielectric material 220 is disposed on the LEDs 204, *e.g.,* an emitting surface 221 of the LEDs 204 or on a side wall of the LEDs 204,

or on the backplane 205 between one or more LEDs 204. In some embodiments, the dielectric material 220 can absorb one or more wavelengths of light, *e.g.,* UV light, IR light, blue light, or a combination thereof, that are generated by the LEDs 204. In some embodiments, the dielectric material 220 can also absorb other wavelengths, while passing the visible light emitted from the LEDs 204 to prevent cross-color contamination in the LED panel 200. Without being bound by theory, the dielectric material 220 disposed on the emitting surface 221 of the LEDs 204 can also provide for enhanced protection of the LEDs 204. Moreover, without being bound by theory, the dielectric material can prevent shorting between the reflective layer 222 and the LED 204. In some embodiments, the dielectric material includes SiN_x, SiO_2, SiOxNy, Al_2O_3, AlN, HfO_2, or a combination thereof.

[0026] In some embodiments, such as those illustrated in FIGs. 2B-2C, the LED panel 200 includes subpixel isolation (SI) structures 216 disposed on an upper surface of a reflective layer 222, as described in the present disclosure, in which the SI structures 216 are disposed between the LEDs 204. The SI structures 216 have an reflection greater than 90%. The high optical density of the SI structures 216 provides for light isolation between each of the LEDs 204. The SI structures 216 define wells 219 of the subpixels 223.

[0027] In some embodiments, such as those illustrated in FIG. 2C, the subpixels 223 have the color conversion material 218 disposed in the wells 219. The subpixels 223 include a red subpixel 218a with a red color conversion material 218a disposed in the well 219a of the red subpixel 223a, a green subpixel 223b with a green color conversion material 218b disposed in the well 219b of the green subpixel 223b, and a blue subpixel 223c with a blue color conversion material 218c disposed in the well 219c of the blue subpixel 223c. When a LED 204 of the red subpixel 223a is turned on the red color conversion material will convert the light emitted from LED 204 into red light. When a LED 204 of the blue subpixel 223c is turned on the blue color conversion material 218c will convert the light emitted from LED 204 into blue light.

[0028] In some embodiments, the SI structures 216 can extend above a height of the LED 204, in each of the LEDs 204 of the LED panel 200. In some embodiments, the SI structures 216 may extend adjacent to and below the contact regions for the electrodes 214 of the LED 204 and may further extend down to the backplane 205 of

the LED panel 200. In some embodiments, the SI structures 216 can be fabricated with reflective and/or conductive materials (e.g., a metal), and may be surrounded by electrically insulating dielectric materials to prevent the SI structures 216 from shorting any of the electrodes of the micro-LED structures. For example, the SI structures 216 may include a dielectric material. The dielectric material may include one or more of silicon oxide, silicon nitride, silicon carbide, a photoresist material, or a dielectric organic-polymer material, among other dielectric materials.

[0029] The SI structures 216 may have a height of greater than or about 2.5 μm, greater than or about 5 μm, greater than or about 7.5 μm, greater than or about 10 μm, greater than or about 12.5 μm, greater than or about 15 μm, greater than or about 17.5 μm, greater than or about 20 μm, or more. The SI structures 216 may have a width of greater than or about 1 μm, greater than or about 2 μm, greater than or about 3 μm, greater than or about 4 μm, greater than or about 5 μm, greater than or about 6 μm, greater than or about 7 μm, greater than or about 8 μm, greater than or about 9 μm, greater than or about 10 μm, or more. The SI structures 216 may have a height-to-width aspect ratio that is greater than or about 1.5: 1, greater than or about 2: 1, greater than or about 2.5: 1, greater than or about 3:1, greater than or about 3.5:1, greater than or about 4:1, greater than or about 4.5:1, greater than or about 5:1, or more.

[0030] In some embodiments, a reflective layer 222 is disposed over the SI structures 216 or on the backplane 205 between one or more LEDs 204. In some embodiments, the reflective layer 222 may substantially cover the sidewalls of the SI structures 216 to prevent light leakage out of the sidewalls. For example, substantially covering the sidewalls of the SI structures 216 may include covering greater than or about 80% of the surface area of the sidewalls of the SI structures 216. In other embodiments, the reflective layer 222 may cover about 100% of the surface area, greater than or about 90% of the surface area, greater than or about 70% of the surface area, greater than or about 60% of the surface area, greater than or about 50% of the surface area, greater than or about 40% of the surface area, and so forth.

[0031] In some embodiments, the reflective layer 222 may be disposed over the dielectric material 220 such that the reflective layer 222 restricts light emission through the lateral portion of the dielectric material 220 and/or the conversion material 218,

thereby allowing emission through a central portion of the conversion material 218. For example, the reflective layer 222 may cover lateral portions of the dielectric material 220 that are proximal to the SI structures 216, while leaving an emitting surface 221 of the LED 204 exposed to allow for light emission through a central portion of the conversion material 218. In some embodiments, the reflective layer 222 may be disposed on the dielectric material 220 disposed on one or more side walls 224 of the LED 204. Without being bound by theory, the reflective layer 222 covering the SI structures 216 and/or the one or more side walls 224 of the LED 204 can reduce the light leakage and/or cross-color contamination. The reflective layer 222 disposed on the sidewalls of the LEDs 204 is reflective to reduce and/or eliminate cross talk between the LEDs 204 and the photodetectors 207. The reflective layer 222 includes a reflective metal. The reflective layer 222 including the reflective metal has a reflectivity of greater than 90%. The reflective metal includes, but is not limited to, aluminum, silver, gold, copper, or combinations thereof.

[0032] FIG. 3 a flow diagram of a method of fabricating an LED panel 200. FIGS. 4A-4J are schematic, cross-sectional views of the backplane 205 during the method 300 for forming the LED panel 200. At operation 302, as shown in FIG. 4A, a dielectric material 220 is formed over a LED 204 of the LED panel 200. In some embodiments, the dielectric material 220 may be formed over the LED 204 using a plasma enhanced chemical vapor deposition (PECVD) process. The PECVD process can deposit a dielectric material including SiN_x, SiO_2, or a combination thereof. In some embodiments, the dielectric material 220 may be formed over the LED 204 using an atomic layer deposition (ALD) process. The ALD process can deposit a dielectric material including Al_2O_3, SiO_2, HfO2, or a combination thereof.

[0033] At operation 304, as shown in FIG. 4B, a first reflective layer 222a is formed over the LED 204. In some embodiments, the first reflective layer 222a may be formed on the sidewalls of the LED 204. The first reflective layer 222a can be formed over the dielectric material 220 using a physical vapor deposition (PVD) process. The PVD process can deposit a reflective metal. The reflective layer 222 including the reflective metal has a reflectivity of greater than 90%. The reflective metal includes, but is not limited to, aluminum, silver, gold, copper, or combinations thereof. The first reflective layer 222a disposed on the sidewalls of the LEDs 204 is reflective to reduce and/or eliminate cross talk between the LEDs 204.

[0034] In some embodiments, the first reflective layer 222a is disposed over the dielectric material 220 disposed over the backplane 205, which is exposed between the LEDs 204. In some embodiments, at operation 304 an anti-reflective layer may be deposited over the first reflective layer 222a. The anti-reflective layer can include chromium nitride. Without being bound by theory, the anti-reflective layer can enhance selectivity during one or more lithography processes, thereby reducing complexity during manufacturing.

[0035] At operation 306, as shown in FIG. 4C, SI structures 216 are formed over the backplane 205. The SI structures 216 can include negative tone resist structures. In some embodiments, the pixel isolation structures can be transparent. At operation 308, as shown in FIG. 4D, one or more positive tone resists 425 are formed along an outer edge of the pixel isolation structures 216. The positive tone resists 425 can provide for contact protection from etching during method 300. Moreover, the positive tone resists 425 can protect one or more subsequent devices from being processed during operations 308-312. In some embodiments, the positive tone resist can include a polymerized phenolic resin formed by a reaction product of formaldehyde and phenol

[0036] At operation 310, as shown in FIG. 4E, the first reflective layer 222a is etched from the SI structures 216 and the LEDs 204. In some embodiments, the first reflective layer 222 can be etched to expose a top surface and/or one or more side walls of the SI structures 216. Moreover, the first reflective layer 222a can be etched to expose the dielectric material 220 disposed over the emitting surface 221 of the LED 204. In some embodiments, the first reflective layer 222a can remain along a side of the LED 204 that is in contact with the SI structures 216. Moreover, the first reflective layer 222a can remain over the dielectric material 220 disposed on the backplane 205 between each LED 204 of the plurality of LEDs 204.

[0037] At operation 312, as shown in FIG. 4F, a second reflective layer 222b is formed over the SI structures 216 and the dielectric material 220 disposed on the LED 204. In some embodiments, the material in the second reflective layer 222b is the same as the material in the reflective layer 222. In other embodiments, the material of the second reflective layer 222b is different from the material of the reflective layer 222. The material of the second reflective layer 222b includes, but is not limited to,

aluminum, silver, gold, copper, or combinations thereof. In some embodiments, the positive tone resist 425 may be removed prior to operation 312. In some embodiments, the second reflective layer 222b may be formed on the sidewalls of the SI structures 216. The second reflective layer 222b can be formed over the SI structures 216 and the dielectric material 220 using PVD process. The PVD process can deposit a reflective metal. The reflective layer 222 including the reflective metal has a reflectivity of greater than 90%. The reflective metal includes, but is not limited to, aluminum, silver, or combinations thereof. The second reflective layer 222b reduces and/or eliminate cross talk between the LEDs 204.

[0038] At operation 314, as shown in FIG. 4G, a second positive tone resist 427 is formed over the second reflective layer 222b. The second positive tone resist 427 can provide for contact protection from etching during method 300. In some embodiments, the positive tone resist can include a polymerized phenolic resin formed by a reaction product of formaldehyde and phenol.

[0039] At operation 316, as shown in FIG. 4H, the second positive tone resist 427 is patterned. The second positive tone resist can be patterned to expose the second reflective layer 222 that is disposed over the dielectric material 220, while maintaining the second positive tone resist 427 over the SI structures 216. At operation 318, as shown in FIG. 4I, the second reflective layer 222 is etched to expose the dielectric material 220 disposed over the emitting surface 221 of the LED 204. In some embodiments, the second reflective layer 222 can remain along a sidewall of the SI structures 216. At operation 320, as shown in FIG. 4J, the second positive tone resist 427 is removed from the SI structures 216. In some embodiments, operation 320 can include removing the second positive tone resist and filling each subpixel 223a, 223b, and 223c with a color conversion material 218. For example, each subpixel 223a, 223b, and 223c can be filled with a red color conversion material 218a, green color conversion material 218b, and blue color conversion material 218c, respectively, as shown in FIG. 2C.

[0040] FIG. 5 is a cross-sectional view of an LED panel. The second isolation arrangement 216b can include one or more a backplane 205. The backplane 205 can include a backplane surface 205a, which can include one or more pairs of backplane electrodes 213 disposed thereon. A plurality of LEDs 204 can be coupled to the pairs

of backplane electrodes 213 disposed on the backplane 205. In some embodiments, a first backplane electrode and a second backplane electrode, can be coupled to a micro-LED via the backplane surface 205a, via a lateral chip or “flip-chip” configuration. Although FIG. 5 illustrates a lateral chip or "flip-chip" configuration, other embodiments may mount the first backplane electrodes to the backplane surface 205a while mounting the second backplane electrode to an opposite side of the micro-LED, referred to as a "vertical-chip" orientation, which is compatible with the all the embodiments described herein that utilize a reflective layer and/or dielectric material.

[0041] In some embodiments, the LEDs 204 include can include pairs of LED electrodes 214 coupled to the pairs of backplane electrodes 213 disposed on the backplane 205. The LEDs 204 may be Patterned Sapphire Substrate (PSS) micro-LEDs or planar micro-LEDs. The LEDs 204 of the LED panel 200 are depicted as planar LEDs 204. The PSS micro-LEDs and planar LEDs 204 can be interchangeable in the second isolation arrangement 216b.

[0042] In some embodiments, a dielectric material 220 is disposed on an emitting surface 221 of the LEDs 204. In some embodiments, the dielectric material 220 can absorb one or more wavelengths of light, *e.g.,* UV light, IR light, blue light, or a combination thereof, that are generated by the LEDs 204. In some embodiments, the dielectric material 220 can also absorb other wavelengths, while passing the visible light emitted from the LEDs 204 to prevent cross-color contamination in the LED panel 200. Without being bound by theory, the dielectric material 220 disposed on the emitting surface 221 of the LEDs 204 can also provide for enhanced protection of the LEDs 204.

[0043] SI structures 216 are disposed on an upper surface of a reflective layer 222, as described in the present disclosure, between the LEDs 204. The SI structures 216 have an UV reflection greater than 90%. The optical density of the SI structures 216 provides for color isolation between each of the LEDs 204. The SI structures 216 define wells 219 of the subpixels 223. The subpixels 223 have the color conversion material 218 disposed in the wells 219. The subpixels 223 include a red subpixel 223a with a red color conversion material 218a disposed in the well 219a of the red subpixel 223a, a green subpixel 223b with a green color conversion material 218b

disposed in the well 219b of the green subpixel 223b, and a blue subpixel 223c with a blue color conversion material 218c disposed in the well 219c of the blue subpixel 223c. When a LED 204 of the red subpixel 223a is turned on the red color conversion material will convert the light emitted from LED 204 into red light. When a LED 204 of the blue subpixel 223c is turned on the blue color conversion material 218c will convert the light emitted from LED 204 into blue light.

[0044] In some embodiments, the SI structures 216 can extend above a height of the LED 204, in each of the LEDs 204 of the LED panel 200. In some embodiments, the SI 216 may extend adjacent to and below the contact regions for the electrodes 214 of the LED 204 and may further extend down to the backplane 205. In some embodiments, the SI structures 216 can be fabricated with reflective and/or conductive materials (e.g., a metal), and may be surrounded by electrically insulating dielectric materials to prevent the SI structures 216 from shorting any of the electrodes of the micro-LED structures. For example, the SI structures 216 may include a dielectric material. The dielectric material may include one or more of silicon oxide, silicon nitride, silicon carbide, a photoresist material, or a dielectric organic-polymer material, among other dielectric materials.

[0045] The SI structures 216 may have a height of greater than or about 2.5 μm, greater than or about 5 μm, greater than or about 7.5 μm, greater than or about 10 μm, greater than or about 12.5 μm, greater than or about 15 μm, greater than or about 17.5 μm, greater than or about 20 μm, or more. The SI structures 216 have a width that is narrowed than the distance between adjacent LEDs 204, in which a gap exists between a first LED 204, an SI structure 216, and a second LED 204. In some embodiments, the SI structures 216 may have a width of greater than or about 1 μm, greater than or about 2 μm, greater than or about 3 μm, greater than or about 4 μm, greater than or about 5 μm, greater than or about 6 μm, greater than or about 7 μm, greater than or about 8 μm, greater than or about 9 μm, greater than or about 10 μm, or more, in which the width of the SI structures 216 does not exceed the total distance between adjacent LEDs 204. The SI structures 216 may have a height-to-width aspect ratio that is greater than or about 1.5: 1, greater than or about 2: 1, greater than or about 2.5: 1, greater than or about 3:1, greater than or about 3.5:1, greater than or about 4:1, greater than or about 4.5:1, greater than or about 5:1, or more.

[0046] In some embodiments, a reflective layer 222 is disposed over the SI structures 216. In some embodiments, the reflective layer 222 may substantially cover the sidewalls of the SI structures 216 to prevent light leakage out of the sidewalls. For example, substantially covering the sidewalls of the SI structures 216 may include covering greater than or about 80% of the surface area of the sidewalls of the SI structures 216 In other embodiments, the reflective layer 222 may cover about 100% of the surface area, greater than or about 90% of the surface area, greater than or about 70% of the surface area, greater than or about 60% of the surface area, greater than or about 50% of the surface area, greater than or about 40% of the surface area, and so forth.

[0047] In some embodiments, the reflective layer 222 may be disposed over the SI structures 216 such that the reflective layer 222 extends to the backplane 205**.** For example, the reflective layer 222 extend down to the backplane 205, in which the backplane 205 is coated with the reflective layer 222. Ion some embodiments, the reflective layer 222 can be disposed along a side wall of the LED 204 and/or along a lateral portion of the dielectric material 220 disposed on the upper surface 221 of the LED 204 while leaving an opening where a portion of the LED 204 exposed to allow for light emission through the color conversion material 218. Without being bound by theory, the reflective layer 222 can reduce the light leakage and/or cross-color contamination.

[0048] FIG. 6 is a flow diagram of a method of fabricating an LED panel 200. FIGS. 7A-7E are schematic cross-sectional views of the backplane 205 during the method 600 for forming the LED panel 200. At operation 602, as shown in FIG. 7A, a dielectric material 220 is formed over a LED 204 of the LED panel 200. At operation 602, as shown in FIG. 7A, pairs of LED electrodes 214 are bonded to pairs of backplane electrodes 213. The pairs of LED electrodes 214 are bonded to the pairs of backplane electrodes 213 via a melting process. The melting process forms an alloy. The alloy may be between the LED electrodes 214 and the backplane electrodes 213. A carrier substrate 728 can include the pairs of micro-LEDs electrodes 214. The pairs of backplane electrodes 213 are disposed on the backplane 205. The carrier substrate 728 can be disposed to contact the pairs of micro-LEDs electrodes 214 with the pairs of backplane electrodes 213. The LEDs 204 can be bonded to the carrier substrate 728.

[0049] The carrier substrate 728 may be made of a ceramic material. The ceramic material may include sapphire, SiN, AlN, Si, SiO_2, GaN, or combinations thereof. The carrier substrate can have an underside surface, which includes the LEDs 204. The LED electrode pairs 214 are coupled to the LEDs 204.

[0050] At operation 604, as shown in FIG. 7B, a UV blocking material 729 is disposed on the backplane 205. The UV blocking material 729 is also disposed between the backplane surface 205a and the underside surface 728a of the carrier substrate 728. In some embodiments, the UV blocking material 729 is disposed by flowing the UV blocking material 729 between the backplane surface 205a, the underside surface 728a, the gaps between the pairs of LED electrodes 214, the pairs of backplane electrodes 213, and the gaps between the LEDs 204. The UV blocking material 729 may be disposed from a corner of the LED panel 200. In some embodiments, the UV blocking material 729 is disposed in the corner with a syringe or a glue dispenser. The UV blocking material 729 may be disposed in a vacuum environment. At operation 606, the UV blocking material 729 is cured. In some embodiments, the UV blocking material 729 is cured with light. In some embodiments, the UV blocking material 729 is cured thermally.

[0051] At operation 608, as shown in FIG. 7C, the carrier substrate 728 is removed. The carrier substrate 728 may be removed via a laser. In one embodiment, the laser removes the carrier substrate 728 by rastering a single spot across the entire carrier substrate 728. In another embodiment, the laser removes the carrier substrate 728 by using a multi beam spot system that rasters across the carrier substrate 728. In yet another embodiment, a broad laser removes the carrier substrate 728 by directing light through a physical chrome mask with openings.

[0052] At operation 610, as shown in FIG. 7D, a plurality of SI structures 216 are formed. As shown in FIG. 7D, the SI structures 216 are disposed on the UV blocking material 729. In some embodiments, the dielectric material 220 is disposed on the LED 204 emitting surface 221. The SI structures 216 and the emitting surface 221 form the wells 219. The wells 219 are configured to contain the color conversion material as described in the present application.

[0053] At operation 612, as shown in FIG. 7E, a reflective layer 222 is formed over the SI structures 216 and the dielectric material 220 disposed on the LED 204. In

some embodiments, the reflective layer 222 may be formed on the sidewalls of the SI structures 216. The reflective layer 222 can be formed over the SI structures 216 and the dielectric material 220 using PVD process. The PVD process can deposit a reflective metal such as aluminum, silver, or any other metal having a reflectivity of greater than 90%. In some embodiments, the second reflective layer 222 can provide a uniform coating of metal, *e.g.,* aluminum or silver, over the pixel 200.

[0054] In some embodiments, operation 612 can include forming a positive tone resist over the reflective layer 222, and patterning the positive tone resist. The positive tone resist can be patterned to expose the reflective layer 222 over the dielectric material 220 while maintaining the positive tone resist over the SI structures 216. The reflective layer 222 can then be etched to expose the dielectric material 220 disposed over the emitting surface 221 of the LED 204. In some embodiments, the reflective layer 222 can remain along a sidewall of the SI structures 216. The positive tone resist can then be removed from the SI structures 216. In some embodiments, operation 610 can include removing the second positive tone resist and filling each subpixel with a color conversion material. For example, each subpixel can be filled with a red color conversion material, green color conversion material or blue color conversion material.

[0055] FIG. 8 is a flow diagram of a method 800 of fabricating an LED panel 200. FIGS. 9A-9C are schematic, cross-sectional views of the backplane 205 during the method 800 for forming the LED panel 200. At operation 802, at least one LED electrode 214 is bonded to at least one backplane electrode 213. The boding process may be a melting process. The melting process forms an alloy. The alloy may be between the LED electrode 214 and the backplane electrode 213. A reflective layer 222 is disposed over the sidewalls of the LEDs 204. The reflective layer 222 disposed on the sidewalls of the LEDs 204 is reflective to reduce cross talk between the LEDs 204. The reflective layer 222 includes a reflective metal. The reflective layer 222 including the reflective metal has a reflectivity of greater than 90%. The reflective metal includes, but is not limited to, aluminum, silver, gold, copper, or combinations thereof.

[0056] At operation 804, as shown in FIG. 9B, an SI layer 916 is deposited over the backplane 205. At operation 806, as shown in FIG. 9C, the SI layer 916 is

patterned. The SI layer 916 is pattered to form SI structures 216 and to expose the light emitting surfaces 221 of the LEDs 204. The SI structures 216 form wells 219. In some embodiments, the wells 219 are configured to contain color conversion materials as described in the present application. In some embodiments, the wells 219 do not include the color conversion material as described in the present application.

[0057] In some embodiments, after operation 806, the method 800 may further include the operation 610 as described in FIGs. 6 and 7E. In some embodiments, after operation 806, the method 800 may further include operations 312-320 as described in FIGs. 3 and 4F-4J.

[0058] Overall, the present disclosure provides pixel isolation structures and fabrication methods thereof, which can provide for reduced and/or eliminated color-cross talk display when using quantum dot color conversion pixels. Moreover, the pixel isolation structures can provide for enhanced quantum dot conversion efficiency and can shield or reflect light that could cross-talk among sub-pixels, thereby enhancing light out-coupling. The pixel isolation structures can be fabricated using one or more of lithography patterning, metal deposition and/or etching, thereby reducing manufacturing costs over conventional quantum dot conversion fabrication processes.

[0059] While the foregoing is directed to implementations of the present disclosure, other and further implementations of the disclosure may be devised without departing from the basic scope thereof, and the scope thereof is determined by the claims that follow.

What is claimed is:

1. A device, comprising:
a light-emitting diode (LED) panel, comprising:
a backplane, the backplane comprising backplane electrodes disposed on or in the backplane;
a plurality of LEDs, each LED comprising an LED electrode, wherein the backplane electrodes are coupled to LED electrodes; and
a reflective layer disposed on sidewalls of each LED of the plurality of LEDs; and
a photodetector array comprising a plurality of photodetectors.

2. The device of claim 1, further comprising subpixel isolation (SI) structures, the SI structures disposed between the each LED of the plurality of LEDs.

3. The device of claim 2, further comprising color conversion material disposed in wells defined by the SI structures.

4. The device of claim 2, wherein a second reflective layer is disposed on the SI structures.

5. The device of claim 2, wherein the SI structures are disposed on a third reflective layer.

6. The device of claim 1, further comprising a dielectric layer disposed between the reflective layer and the sidewalls of each LED of the plurality of LEDs.

7. The device of claim 6, wherein the dielectric layer is further disposed on a light emitting surface of each LED of the plurality of LEDs.

8. The device of claim 1, further comprising at least one of an optical fiber bundle or a waveguide, wherein the plurality of photodetectors are coupled to the plurality of LEDs by the at least one of the optical fiber bundle or the waveguide.

9. The device of claim 1, wherein the photodetector array is disposed on a transimpedance amplifier (TIA).

10. A device comprising:

a backplane, the backplane comprising backplane electrodes disposed on or in the backplane;

a plurality of LEDs, each LED comprising an LED electrode, each LED electrode is coupled to a respective backplane electrode;

a plurality of photodetectors, each photodetector comprising a detector electrode, each detector electrode is coupled to the respective backplane electrode; and

a reflective layer disposed on sidewalls of each LED of the plurality of LEDs.

11. The device of claim 10, further comprising at least one of an optical fiber or a waveguide disposed over the plurality of LEDs and the plurality of photodetectors, wherein the at least one of the optical fiber or the waveguide is configured to receive light emitted from the LEDs and transmit light to the photodetectors.

12. The device of claim 10, wherein the backplane includes an electrode layer and an integrated circuit layer

13. The device of claim 10, further comprising subpixel isolation (SI) structures, the SI structures disposed between the plurality of LEDs and the plurality of photodetectors.

14. A method of fabricating a device, comprising

bonding a plurality of LEDs to a backplane, each LED comprising:

a reflective layer disposed on sidewalls of each LED; and

an LED electrode, wherein the plurality of LEDs are coupled to backplane electrodes on or in the backplane;

forming a subpixel isolation (SI) structure layer disposed on an upper surface of the plurality of LEDs; and

patterning the SI structure layer to form a plurality of SI structures defining wells above each LED.

15. The method of claim 14, wherein the plurality of LEDs are bonded to the backplane by a carrier substrate.

16. The method of claim 14, wherein each LED of the plurality of LEDs further comprising a dielectric layer disposed between the reflective layer and the sidewalls of each LED.

17. The method of claim 14, further comprising disposing color conversion materials in the wells.

18. The method of claim 14, wherein each LED further comprises a dielectric layer disposed on an outer surface of the LED below the reflective layer.

19. The method of claim 14, further comprising disposing a second reflective layer over the SI structures and the plurality of LEDs.

20. The method of claim 19, further comprising etching the second reflective layer to expose the dielectric layer atop the light emitting surface of each LED of the plurality of LEDs.