INTEGRATED CIRCUIT COMPRISING A SUBSTRATE AND A WIRING LAYER WITH A BUFFER LAYER BETWEEN THE SUBSTRATE AND THE WIRING LAYER

BACKGROUND OF THE INVENTION

1. *Field of the Invention*

The present invention pertains to the field of wiring layers for integrated circuit devices and, more particularly, electrodes including buffer layers that compensate interlayer incompatibility problems, as well as methods of making these buffer layers. More specifically, the buffer layers are preferably used in the electrodes of ferroelectric capacitors.

2. *Description of the Prior Art*

Integrated circuit devices can fail or suffer performance degradation due to materials incompatibility problems. Surface irregularity problems can induce defects in successively stacked layers. Thin-film layers can be contaminated by diffusion from adjacent layers. Cracking, peeling, and surface irregularity problems can derive from different thermal coefficients of expansion or other growth in the respective layers, as it is often necessary to heat the devices in manufacture. These problems are intensified by the micro-thin nature of the circuit layers because it is impossible to predict the thermal performance of a given layer without also considering the substrate on which the layer is formed. Accordingly, circuit designers must carefully select the materials that will form the respective thin-film layers.

A common circuit failure mechanism includes shorting that is induced by the cracking or peeling of one thin-film layer away from another layer due to poor bonding between the adjacent layers. In silicon technology devices, a platinum wiring layer or electrode can bond poorly with a silicon dioxide or titanium dioxide isolation layer that separates the platinum electrode from the silicon wafer. Researchers have successfully reduced the incidence of cracking by applying a titanium metal adhesion layer to the isolation layer prior to sputtering the platinum electrode; however, the application of titanium metal proved to be problematic. The additional titanium served to contaminate other layers through titanium diffusion. Diffused titanium contamination is particularly problematic in integrated circuits because the titanium cations typically present a variety of valence states, i.e., +2,

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+3, and +4, which induce corresponding lattice defects. Metal nitride diffusion barrier layers have been constructed in attempts in attempts to isolate the adhesion layer metals. See for example the United States patent to Larson, 5,005,102, and Garceau et al, "TiN As A Diffusion Barrier Layer In The Ti-Pt-Au Beam Less Metal System", 60 Thin Solid Films, 237 - 247, No. 2, (1979), which both teach the use of a titanium nitride diffusion barrier layer. Annealing of metal nitrides can yield surface irregularities, e.g., hillocks, that induce shorting of dielectric or ferroelectric capacitors.

The magnitude of polarization that is available from a thin-film ferroelectric material is a limiting factor that controls the memory density for a given voltage. Larger polarizations can be used to make denser memories. Nevertheless, it is also necessary for the ferroelectrics to adhere well to a substrate, and reduced polarization can derive from the necessity of adding diffusible materials that promote adhesion between the proximal faces of two separate layers. Hence, a materials selection conflict arises between the need for adherance and the need for high polarization.

There remains a need for an effective bottom electrode structure that adheres well, does not have short-inducing surface irregularities, and has a high polarization.

SOLUTION TO THE PROBLEM

The present invention overcomes the problems that are outlined above by providing a buffer layer and an adhesion metal-containing electrode which is substantially free of surface irregularities. The addition of a buffer layer provides substantial improvements of up to 100% or more in the polarization performance of ferroelectric capacitors, as compared with similarly processed ferroelectric capacitors that lack the buffer layer.

The electrode structure broadly pertains to an integrated circuit device that includes a substrate, a metal electrode or wiring layer, and a layer sequence consisting of material interposed between the substrate and the wiring layer. The layer sequence includes at least one buffer layer made of a layered superlattice material, and is essentially free of additional wiring layers.

Particularly preferred forms of the electrode structure include the layered superlattice material being strontium bismuth tantalate. Other preferred layered

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superlattice materials include strontium bismuth niobate, and strontium bismuth niobium tantalate. The substrate preferably includes an uppermost silicon-based layer, e.g., silicon dioxide, proximal to the layer sequence. The most preferred substrate includes a silicon wafer. The wiring layer preferably includes an adhesion metal moiety, such as titanium or tantalum. This adhesion metal is preferably utilized in combination with a noble metal, which is most preferably platinum.

A ferroelectric capacitor may be constructed by forming a ferroelectric layer atop the electrode structure. This ferroelectric layer preferably includes a layered superlattice material, such as strontium bismuth tantalate, strontium bismuth niobate, or combinations thereof. The capacitor is preferably completed by forming a second electrode over the ferroelectric layer.

A preferred method is used to make integrated circuit devices having the above-described electrode structure. The method comprises the steps of providing a substrate having a nonmetallic uppermost surface, forming a layered superlattice material atop the substrate and depositing an electrode over the layered superlattice material.

Particularly preferred methods are those wherein the forming step includes a step of applying a liquid precursor on the substrate to form a thin precursor film. The precursor preferably includes polyoxyalkylated metal moieties in effective amounts for yielding the layered superlattice material upon thermal treatment of said precursor. The precursor film is thermally treating said film to yield the layered superlattice material.

The treating step preferably includes annealing the precursor at a temperature of at least 450°C, and more preferably a temperature of at least about 600°C. Additionally, the treating step may include drying the precursor at a temperature up to about 450°C for a period of time sufficient to remove substantially all volatile organic components from the thin precursor film.

The method is used to form a capacitor device by the further step of constructing a second layered superlattice material atop the electrode. Again, a liquid deposition technique is preferably used to deposit the layer. The layered superlattice material spontaneously generates from a liquid precursor solution of superlattice-forming moieties upon heating of the precursor solution.

As indicated above, the ferroelectric material is preferably a perovskite-like layered superlattice material. The term "perovskite-like" refers to a lattice that is formed of respective oxygen octahedra layers that are separated by superlattice generator layers including a trivalent metal such as bismuth. These materials are recognized as a broad class of ferroelectric materials, but have not historically been successfully applied in integrated circuit devices due to device reliability problems. The perovskite-like portion of the layered superlattice material is formed in discrete layers separated by bismuth oxide layers. The perovskite-like layers include a primary cell having an oxygen octahedral positioned within a cube that is defined by large A-site metals at the corners. The oxygen atoms occupy the planar face centers of the cube and a small B-site element occupies the center of the cube. In some instances, the oxygen octahedral structure may be preserved in the absence of A-site elements.

The most preferred layered superlattice material is strontium bismuth tantalate material having an average empirical formula of $SrBi_2Ta_2O_9$. The superlattice-generator layers are most preferably formed of $(Bi_2O_2)^{2+}$ materials, but may also contain thallium (III) as the metal. The most preferred oxygen octahedra structure layers, accordingly, have an average empirical formula of $(SrTa_2O_7)^{2-}$. The respective layers spontaneously generate a layered superlattice upon annealing of a metal organic precursor solution. The oxygen octahedra layers are ferroelectric and have an average empirical formula with an ionic charge that is offset by the superlattice generator layers to balance the overall crystal charge. The buffer layer serves to keep the layered superlattice material essentially free of point defects, which can degrade polarization.

Other features, objects, and advantages will be apparent to those skilled in the art upon reading of the following description and drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

FIGURE 1 depicts a thin-film ferroelectric capacitor device including a buffer layer formed of a layered superlattice material interposed between a bottom electrode and an underlying substrate;

FIG. 2 depicts a flow chart process diagram for use in making the capacitor of FIG. 1;

FIG. 3 depicts a flow chart process diagram for use in making a liquid precursor solution that may be used in the FIG. 2 process;

FIG. 4 depicts a faulty bottom electrode structure having large hillock structures on its uppermost surface; and

FIG. 5 is a bar graph comparing average polarization values obtained from capacitors that were processed under different conditions.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

FIG. 1 depicts capacitor 20 including substrate 22, buffer layer 24, bottom electrode 26, metal oxide layer 28, and top electrode 30. Substrate 22 preferably includes conventional silicon layer 32, which is capped by isolation layer 34. Silicon layer 32 may be a single crystal or polycrystalline silicon, and is commercially available from a variety of sources as a silicon wafer. Layer 32 may also be formed of other known substrate materials, such as gallium arsenide, indium antimonide, magnesium oxide, strontium titanate, sapphire, quartz and combinations of the forgoing as well as other materials. Isolation layer 34 is preferably made of thick silicon dioxide, which is formed on layer 32 by well-known processes, e.g., spin-on glass ("SOG") deposition or baking of layer 32 under oxygen in a diffusion furnace. As used herein, the term "substrate" specifically means a layer that provides support for any other layer. Substrate 22 serves to support all other layers, but the term substrate can also mean substrate 22 in combination with other layers. Accordingly, the combination of substrate 22, buffer layer 24, and bottom electrode 26 provides a substrate or support for metal oxide layer 28, which, in turn, provides support for top electrode 30.

Buffer layer 24 overlies substrate 22. Layer 24 is preferably a perovskite-like layered superlattice material. Particularly preferred layered superlattice materials include strontium bismuth tantalate, strontium bismuth niobate, and strontium bismuth niobium tantalate. The most preferred strontium bismuth tantalate has an average empirical formula of $SrBi_2Ta_2O_9$. Many perovskite-like layered superlattice ferroelectrics are also high dielectrics.

The use of buffer layer 24 provides significant polarization improvements for ferroelectric capacitors and, particularly, for capacitors that utilize layered superlattice ferroelectrics. Layered superlattice materials at least include all three

of the Smolenskii-type ferroelectric layered superlattice materials, namely, those having the respective average empirical formulae:

(1) $A_{m-1}S_2B_mO_{3m+3}$;

(2) $A_{m+1}B_mO_{3m+1}$; and

(3) $A_mB_mO_{3m+2}$,

wherein A is an A-site metal in the perovskite-like superlattice, B is a B-site metal in the perovskite-like superlattice, S is a trivalent superlattice-generator metal such as bismuth or thallium, and m is a number sufficient to balance the overall formula charge. Where m is a fractional number in the overall formula, the formula typically provides for a plurality of different or mixed perovskite-like layers each having a different integer value. The A-site metals and B-site metals may include mixtures of cations having similar ionic radii.

In layered superlattice materials according to Formula (1), thermodynamics favor the formation of oxygen octahedra structures in layers having a thickness of m octahedra according to the formula

(4) $(A_{m-1}B_mO_{3m+1})^{2-}$,

wherein m is an integer greater than one and the other variables are defined above. These layers are separated by bismuth oxide layers having the formula

(5) $(Bi_2O_2)^{2+}$,

wherein Bi is S of Formula (1).

The superlattice-generator layers, S, preferably include oxides of bismuth (III), and may also include other similarly sized trivalent metal cations such as thallium (III). Bismuth also functions as an A-site metal in the perovskite-like lattice if it is present in excess of the stoichiometrically required amount for generating the layered superlattice material according to Formula (I).

Bottom electrode 26 includes adhesion metal portion 36 and noble metal portion 38. Adhesion metal portion 36 is preferably made of titanium or tantalum sputtered, and is most preferably titanium. Portion 36 is preferably sputtered to a thickness that preferably ranges from about 50 Å to 250 Å, and is most preferably 200 Å thick. First noble metal portion 38 is preferably platinum, but may also be other noble metals such as gold, silver, palladium, iridium, rhenium, ruthenium, and osmium, as well as conductive oxides of these metals. First noble metal portion 38 is preferably deposited by sputtering platinum atop adhesion metal portion 36 to

a thickness ranging from three to fifteen times the thickness of adhesion metal portion 36, with the most preferred thickness being about 2000 Å when adhesion metal portion is from 100 Å to 200 Å thick. Thicknesses outside the preferred range of values are still useful, but a thinner first noble metal portion 38 increasingly permits diffusion of adhesion metal moieties to layers above portion 38. A thicker portion 38 is increasingly wasteful of the noble metal material.

Layer 28 is preferably a ferroelectric perovskite-like layered superlattice material. Particularly preferred layered superlattice materials include strontium bismuth tantalate, strontium bismuth niobate, and strontium bismuth niobium tantalate. The most preferred strontium bismuth tantalate has an average empirical formula of $SrBi_2Ta_2O_9$.

A top-wiring layer or electrode 30 is preferably a noble metal that is sputtered over metal oxide layer 30. The thickness of top electrode 28 will typically range from about 1000 Å to about 2000 Å, but the thickness can be a value outside of this range. Electrode 30 is most preferably made of platinum.

FIG. 2 depicts a flow chart of a process for making capacitor 20. The process shall be discussed in terms of the embodiment of FIG. 1, but those skilled in the art will understand its applicability to other embodiments.

In step P40, a silicon wafer is prepared as substrate 22 having silicon layer 32 and silicon dioxide layer 34. Silicon layer 32 can be baked under oxygen in a diffusion furnace at a temperature ranging from about 500°C to about 1100°C. This baking serves to eliminate surface impurities and water, and form oxide coating 34. Wafer or layer 32 can also be coated with a conventional spin-on glass to form oxide layer 34. Generally, depending upon the nature of the device sought to be constructed, step P40 may also include conventional procedures such as the etching of contact holes (not depicted) and the doping of layer 32 (generally, substrate 22) for transistor or memory circuits.

Step P42 includes the preparation of one or more liquid precursor solutions having a plurality of metal moieties in effective amounts for yielding buffer layer 24 and/or ferroelectric layer 28 upon drying and annealing of the precursor solution. Additional details pertaining to the preparation of the precursor solution will be provided below.

In step P44, the precursor solution from step P42 is applied to the substrate from step P42, which presents the uppermost surface of oxide layer 34 to receive the liquid precursor. This application is preferably conducted by dropping the liquid precursor solution at ambient temperature and pressure onto the uppermost surface of oxide layer 34 (generally, substrate 22) then spinning the substrate at from about 1500 RPM to 2000 RPM for about 30 seconds to remove any excess solution and, thus, leave a thin-film liquid residue. The most preferred spin velocity is 1500 RPM. Alternatively, the liquid precursor may be applied by a misted deposition technique, such as the technique described in US 5,456,945. The most preferred precursor solutions are those capable of yielding layered superlattice materials, such as strontium bismuth tantalate.

In step P46, the liquid precursor film from step P44 is preferably dried on a hot plate in a dry air atmosphere and at a temperature of from about 200°C to 500°C. The drying time and temperature should be sufficient to remove substantially all of the organic materials from the liquid thin film and leave a dried metal oxide residue. The drying time preferably ranges from about one minute to about thirty minutes. For single-stage drying, a 400°C drying temperature over a duration of about two to ten minutes in air is most preferred. It is more preferred, however, to dry the liquid film in stepped intervals. For example, the film can be dried for five minutes at 260°C and for five minutes at 400°C. Additionally, it is preferred to conclude the drying cycle with a brief rapid processing interval at a temperature exceeding 700°C, e.g., using a tungsten-nickel lamp to heat the substrate to 725°C for thirty seconds. The drying step P46 is essential in obtaining predictable or repeatable electronic properties in the final metal oxide crystal compositions.

Steps P44 and P46 can be repeated if it is desirable to increase the overall thickness of buffer layer 24, however, it will not normally be necessary or desirable to increase the thickness of layer 24 beyond that obtainable from a single coat of precursor liquid.

Optional step P48 includes sputtering titanium adhesion metal layer 36 atop buffer layer 24 to a preferred thickness ranging from about 50 Å to 250 Å according to conventional protocols as are known in the art. Sputtering layer 36 is preferably conducted for purposes of providing better adhesion to layer 24. This sputtering

prevents peeling and crackling of adjacent layers that can induce shorts in capacitor 20, however, the adhesion metal (preferably titanium) can contaminate other layers by diffusion. Step P50 includes sputtering noble metal portion 38 to a preferred thickness ranging from about 1000 Å to 2000 Å atop portion 36. Examples of preferred atomic sputtering protocols include radio frequency sputtering and DC magnetron sputtering.

In step P52, the substrate 22 from Step P50 is annealed to form the metal oxide of buffer layer 24. Step P52 is referred to as the "first anneal" to distinguish it from other anneal steps; however, it should be understood that other anneal steps can occur prior to this "first anneal." In step P52, the substrate including layers 36 and 38 is preferably heated in a diffusion furnace under an oxygen atmosphere to a temperature ranging from 450°C to 1000°C for a time ranging from 30 minutes to 2 hours. Step P52 is more preferably conducted at a temperature ranging from 600°C to 800°C, with the most preferred anneal temperature being about 600°C for eighty minutes. The first anneal of step P52 preferably occurs in a push/pull process including five minutes for the "push" into the furnace and five minutes for the "pull" out of the furnace. The indicated anneal times include the time that is used to create thermal ramps into and out of the furnace.This annealing step is referred to as the first anneal to distinguish it from other annealing steps.

Step P54 includes depositing a layered superlattice precursor from step P42 atop noble metal layer 38. This precursor is preferably a liquid precursor, but may also be sputtered from a solid target. The application is preferably conducted by dropping the liquid precursor solution at ambient temperature and pressure onto the uppermost surface of bottom electrode 26 then spinning the substrate at from about 1500 RPM to 2000 RPM for about 30 seconds to remove any excess solution and leave a thin-film liquid residue. The most preferred spin velocity is 1500 RPM. Preferred precursor solutions include those having metal moieties in effective amounts for yielding a layered superlattice material. The most preferred layered superlattice material is strontium bismuth tantalate.

In step P56, the liquid precursor film from step P54 is preferably dried on a hot plate in a dry air atmosphere and at a temperature of from about 200°C to 500°C. The drying time and temperature should be sufficient to remove

substantially all of the organic materials from the liquid thin film and leave a dried metal oxide residue. The drying time preferably ranges from about one minute to about thirty minutes. For single-stage drying, a 400°C drying temperature over a duration of about two to ten minutes in air is most preferred. It is more preferred, however, to dry the liquid film in stepped intervals. For example, the film can be dried for five minutes at 260°C and for five minutes at 400°C. Additionally, it is preferred to conclude the drying cycle with a brief heating interval at a temperature exceeding 700°C, e.g., using a tungsten-nickel lamp to heat the substrate to 725°C for thirty seconds. The drying step P56 is essential in obtaining predictable or repeatable electronic properties in the final metal oxide crystal compositions.

In step P58, if the resultant dried film from step P56 is not of the desired thickness, then steps P54, P56, and P58 are repeated until the desired thickness is attained. A thickness of about 1800 Å to 2000 Å typically requires two coats of a 0.130M to 0.200M precursor solution under the parameters disclosed herein.

In step P60, the dried precursor residue from steps P54 and P56 is annealed to form the layered superlattice material of layer 26. This annealing step is referred to as the second anneal to distinguish it from other annealing steps. This second anneal is preferably conducted under conditions that are identical to the conditions of the first anneal in step P52.

In step P62, top electrode 28 is preferably deposited by sputtering platinum atop layered superlattice material layer 26. Capacitor 20 may optionally be annealed at this time, preferably, under conditions that are identical to those in step P52.

The device is then patterned by a conventional photoetching process, e.g., including the application of a photoresist followed by ion etching lithography in step P64. This patterning preferably occurs before the third anneal of step P66 so that the third anneal will remove patterning stresses from capacitor 20 and correct any defects that are created by the patterning procedure.

The third anneal, Step P66, is preferably conducted in like manner with the first anneal in step P52.

Finally, in step P68 the device is completed and evaluated. The completion may entail the deposition of additional layers, ion etching of contact holes, and other procedures, as will be understood by those skilled in the art. Substrate or

wafer 22 may be sawed into separate units to separate a plurality of integrated circuit devices that have been simultaneously produced thereon.

A preferred general process for preparing the polyoxyalkylated metal precursors of step P42 is provided in US 5,514,822. The process preferably includes reacting a metal with an alkoxide (e.g., 2-methoxyethanol) to form a metal alkoxide, and reacting the metal alkoxide with a carboxylate (e.g., 2-ethylhexanoate) to form a metal alkoxycarboxylate according to one of the generalized formulae:

(6) $(R'\text{-}COO\text{-})_aM(\text{-}O\text{-}R)_n$, or

(7) $(R'\text{-}C\text{-}O\text{-})_aM(\text{-}O\text{-}M'(\text{-}O\text{-}C\text{-}R'')_{b-1})_n$,

wherein M is a metal cation having an outer valence of (a + n) and M' is a metal cation having an outer valence of b, with M and M' preferably being independently selected from the group consisting of tantalum, calcium, bismuth, lead, yttrium, scandium, lanthanum, antimony, chromium, thallium, hafnium, tungsten, niobium, vanadium, zirconium, manganese, iron, cobalt, nickel, magnesium, molybdenum, strontium, barium, titanium, and zinc; R and R' are respective alkyl groups preferably having from 4 to 9 carbon atoms and R" is an alkyl group preferably having from 3 to 8 carbon atoms. The latter formula, which has a central -O-M-O-M'-O- structure, is particularly preferred due to the formation in solution of at least 50% of the metal to oxygen bonds that will exist in the final solid metal oxide product.

The liquid precursor is preferably a metal alkoxide or metal carboxylate, and is most preferably a metal alkoxycarboxylate diluted with a xylene or octane solvent to a desired concentration. The use of an essentially anhydrous metal alkoxycarboxylate is particularly preferred due to the corresponding avoidance of water-induced polymerization or gelling, which can significantly reduce the shelf-life of solutions that contain alkoxide ligands. The presence of any hydrolysis-inducing moiety in solution is preferably avoided or minimized. Hydrolyzed precursors, such as conventional sol-gels, may also be utilized, but the increased solution viscosity tends to impair the uniformity of thickness derived from the preferred spin-on application process, and the quality of the hydrolyzed solution tends to degrade rapidly with time. As a consequence, made-ready hydrolyzed gels increasingly yield poor quality metal oxide films of inconsistent quality over a period of time.

The preferred method permits the preparation of precursor solutions well in advance of the time that they are needed.

The precursor solutions may be designed to yield corresponding layered superlattice materials, with the understanding that the formation of oxygen octahedra structures is thermodynamically favored where possible. Generally, in terms of either the perovskite-like octahedral structure or the perovskite octahedral structure, equivalent substitutions may be made between metal cations having substantially similar ionic radii, i.e. radii that vary no more than about 20% at the respective lattice sites. These substitutions are made by adding the alternative metal moieties to the precursor solution.

The preferred ingredients of the precursor solutions include the preferred metals of the desired layered superlattice material in a stoichiometrically balanced combination according to the empirical formula. The A-site portion is preferably formed by reacting with an alcohol or carboxylic acid at least one A-site element selected from an A-site group consisting of Ba, Bi, Sr, Pb, La, Ca, and mixtures thereof. The B-site portion is preferably derived by reacting an alcohol or carboxylic acid with at least one B-site element selected from a B-site group consisting of Zr, Ta, Mo, W, V, Nb, and mixtures thereof. The use of titanium as an equivalent radius B-site element, though possible, is less preferred in practice due to problems that derive from titanium diffusion into other integrated circuit components and point charge defects that arise from different valence states among the titanium ions. In the case of layered superlattice materials, there is also added a trivalent superlattice-generator metal, which is preferably bismuth. With heating, the bismuth content will spontaneously generate bismuth oxide layers in the layered superlattice materials, but an excess bismuth portion can also provide A-site elements for the perovskite-like lattice.

FIG. 3 depicts a flow chart of a generalized process according to the present invention for providing a liquid precursor solution to be prepared in step P42. The word "precursor" is often used ambiguously in this art. It may mean a solution containing one metal that is to be mixed with other materials to form a final solution, or it may mean a solution containing several metals made-ready for application to a substrate. In this discussion we shall refer to the made-ready type of precursor

as a "precursor," unless a different meaning is clear from the context. In intermediate stages the solution may be referred to as the "pre-precursor."

The preferred generalized reaction chemistry for the formation of liquid solutions of metal alkoxides, metal carboxylates, and metal alkoxycarboxylates for use in producing the initial metal precursor portions is as follows:

(8) alkoxides - $M^{+n} + n\ R\text{-}OH \rightarrow M(\text{-}O\text{-}R)_n + n/2\ H_2$

(9) carboxylates - $M^{+n} + n\ (R\text{-}COOH) \rightarrow M(\text{-}OOC\text{-}R)_n + n/2\ H_2$

(10) alkoxycarboxylates - $M(\text{-}O\text{-}R')_n + b\ R\text{-}COOH + \text{heat} \rightarrow (R'\text{-}O\text{-})_{n-b}M(\text{-}OOC\text{-}R)_b + b\ HOR$,

where M is a metal cation having a charge of n; b is a number of moles of carboxylic acid ranging from 0 to n; R' is preferably an alkyl group having from 4 to 15 carbon atoms and R is preferably an alkyl group having from 3 to 9 carbon atoms.

In step P70 a first metal, indicated by the term M in the equations above, is reacted with an alcohol and a carboxylic acid to form a metal-alkoxycarboxylate pre-precursor. The process preferably includes reacting a metal with an alcohol (e.g., 2-methoxyethanol) to form a metal alkoxide according to Equation (8), and reacting the metal alkoxide with a carboxylic acid (e.g., 2-ethylhexanoic acid) to form a metal alkoxycarboxylate according to Equation (10). A reaction according to Equation (9) is also observed in the preferred mode when the unreacted metal is simultaneously combined with the alcohol and the carboxylic acid. The simultaneous reactions are preferably conducted in a reflux condenser that is heated by a hot plate having a temperature ranging from about 120°C to about 200°C over a period of time ranging from one to two days to permit substitution of the alkoxide moieties by carboxylate ligands. At the end of the initial one to two day reaction period, the reflux condenser is preferably opened to atmosphere, and the solution temperature is monitored to observe a fractional distillation plateau that indicates the substantial elimination of all water and alcohol portions from the solution, i.e., a plateau exceeding at least about 100°C, at which time the solution is removed from the heat source. Distillation to atmospheric pressure is more preferably is conducted to a temperature of at least 115°C, and most preferably to a temperature of about 123°C to 127°C.

In the above equations, the metal is preferably selected from the group consisting of tantalum, calcium, bismuth, lead, yttrium, scandium, lanthanum, antimony, chromium, thallium, hafnium, tungsten, vanadium, niobium, zirconium, manganese, iron, cobalt, nickel, magnesium, molybdenum, strontium, barium, titanium, vanadium, and zinc. Alcohols that may be used preferably include 2-methoxyethanol, 1-butanol, 1-pentanol, 2-pentanol, 1-hexanol, 2-hexanol, 3-hexanol, 2-ethyl-1-butanol, 2-ethoxyethanol, and 2-methyl-1-pentanol, preferably 2-methoxyethanol. Carboxylic acids that may be used preferably include 2-ethylhexanoic acid, octanoic acid, and neodecanoic acid, preferably 2-ethylhexanoic acid.

The reactions of step P70 and subsequent steps are preferably facilitated by the use of a compatible solvent. Solvents that may be used include xylenes, 2-methoxyethanol, n-butyl acetate, n-dimethylformamide, 2-methoxyethyl acetate, methyl isobutyl ketone, methyl isoamyl ketone, isoamyl alcohol, cyclohexanone, 2-ethoxyethanol, 2-methoxyethyl ether, methyl butyl ketone, hexyl alcohol, 2-pentanol, ethyl butyrate, nitroethane, pyrimidine, 1, 3, 5 trioxane, isobutyl isobutyrate, isobutyl propionate, propyl propionate, ethyl lactate, n-butanol, n-pentanol, 3-pentanol, toluene, ethylbenzene, and octane, as well as many others. These solvents preferably have boiling points exceeding that of water for purposes of distilling the precursor to eliminate water therefrom prior to application of the precursor to a substrate. The cosolvents should be miscible with one another and may be compatibly mixed in differing proportions, especially between polar and apolar solvents, as needed to fully solubilize the precursor ingredients. Xylenes and octane are particularly preferred apolar solvents, and n-butyl acetate is a particularly preferred polar cosolvent.

Portions of step P70 can be skipped in the event that intermediate metal reagents can be obtained in research grade purity. For example, where tantalum isobutoxide is available, it will only be preferred to substitute the isobutoxide moiety with an acceptable carboxylate ligand by reacting the metal alkoxide with a carboxylic acid such as 2-ethylhexanoic acid according to Equation (10).

In a typical second step, P72, a metal-carboxylate, a metal-alkoxide or both may be added to the metal-alkoxycarboxylate in effective amounts to yield an intermediate precursor having a stoichiometrically balanced mixture of superlattice-

forming metal moieties that is capable of yielding a solid metal oxide for layer 26. At this time the mixture will preferably exclude bismuth compounds which, if needed, will be added later due to their relative thermal instability. Any of the metals listed above may be reacted with any of the carboxylic acids listed above to form the metal carboxylate, while any of the metals listed above may be reacted with any of the alcohols may form the alkoxide. It is particularly preferred to conduct this reaction in the presence of a slight excess amount of carboxylic acid for purposes of partially substituting alkoxide ligands with carboxylate ligands.

In step P74 the mixture of metal-alkoxycarboxylates, metal-carboxylates and/or metal-alkoxides is heated and stirred as necessary to form metal-oxygen-metal bonds and boil off any low-boiling point organics that are produced by the reaction. According to a generalized reaction theory, if a metal-alkoxide is added to the metal-alkoxycarboxylate, and the solution is heated, the following reactions occur:

(11) $(R\text{-}COO\text{-})_xM(\text{-}O\text{-}C\text{-}R')_a + M'(\text{-}O\text{-}C\text{-}R'')_b \longrightarrow (R\text{-}COO\text{-})_xM\text{-}O\text{-}M'(\text{-}O\text{-}C\text{-}R'')_{b-1})_a + a\ R'\text{-}C\text{-}O\text{-}C\text{-}R''$

(12) $(R\text{-}COO\text{-})_xM(\text{-}O\text{-}C\text{-}R')_a + x\ M'(\text{-}O\text{-}C\text{-}R'')_b \longrightarrow (R'\text{-}C\text{-}O\text{-})_aM(\text{-}O\text{-}M'(\text{-}O\text{-}C\text{-}R'')_{b-1})_x + x\ R\text{-}COO\text{-}C\text{-}R''$

where M and M' are metals; R and R' are defined above; R" is an alkyl group preferably having from about zero to sixteen carbons; and a, b, and x are integers denoting relative quantities of corresponding substituents corresponding to the respective valence states of M and M'. Generally the reaction of Equation (11) will occur first since metal alkoxides react more readily than metal carboxylates. Thus, ethers having low boiling points are generally formed. These ethers boil out of the pre-precursor to leave a final product having a reduced organic content and the metal-oxygen-metal bonds of the final desired metal oxide already partially formed. If the heating is sufficient, some of the reaction (12) will also occur, creating metal-oxygen-metal bonds and esters. Esters generally have higher boiling points and remain in solution. These high boiling point organics slow down the drying process after the final precursor is applied to a substrate, which tends to reduce cracking and defects; thus, in either case, metal-oxygen-metal bonds are formed and the final precursor performance is improved.

Step P74 is in essence a distillation to eliminate volatile moieties from solution as the reactions of equations (11) and (12) proceed. The elimination of volatile moieties from solution drives the reactions to completion, i.e., a high rate of efficiency. The elimination of volatile moieties from solution also serves to prevent film cracking and other defects that, otherwise, can be associated with the presence of volatile moieties in solution. Accordingly, the progress of reactions (11) and (12) can be monitored by the rate of solution heating as well as the volume of fluid exiting the solution. It is preferred to heat the solution to a boiling point plateau of at least 115°C, more preferably to 120°C, and most preferably from 123°C to 127°C.

If a metal-carboxylate is added to the metal-alkoxycarboxylate and the mixture is heated, the following reaction occurs:

(13) $(R\text{-}COO\text{-})_xM(\text{-}O\text{-}C\text{-}R')_a + x\ M'(\text{-}OOC\text{-}R'')_b \longrightarrow$

$(R'\text{-}C\text{-}O\text{-})_aM(\text{-}O\text{-}M'(\text{-}OOC\text{-}R'')_{b-1})_x + x\ R\text{-}COOOC\text{-}R'$

where R-COOOC-R' is an acid anhydride, and the terms are as defined above. This reaction requires considerably more heat than do the reactions (11) and (12) above, and proceeds at a much slower rate.

In addition to the above reactions which produce metal-alkoxycarboxylates, reactions occur such as:

(14) $M(\text{-}OR)_a + a\ HO_2C_8H_{15} + \text{heat} \longrightarrow M(\text{-}O_2C_8H_{15})_a + a\ HOR,$

where the terms are as defined above. This reaction, with heating in the presence of excess carboxylic acid, substitutes the alkoxide part of the intermediate metal-alkoxycarboxylate to form a substantially full carboxylate; however, it is now believed that a complete substitution of the alkoxides by the carboxylates does not occur with the parameters as disclosed herein. Full substitution of the carboxylates requires significantly more heating, and even then may not readily occur.

At the end of step P74, it is preferable to have formed in solution at least 50% of the metal to oxygen bonds of the metal oxide layer 26. The reactions are preferably conducted in a vessel that is open to atmospheric pressure and is heated by a hot plate preferably having a temperature ranging from about 120°C to about 200°C until the solution temperature is monitored to observe a fractional distillation plateau that indicates the substantial elimination of all water, alcohol, ether, and other reaction byproduct portions from the solution, i.e., a plateau at

least exceeding 100°C. At this time, extended refluxing can produce a potentially undesirable amount of an ester or acid anhydride byproduct that is often difficult to remove from the solution by fractional distillation. The potential complication of an excessive acid anhydride concentration can be entirely avoided by adding only metal carboxylates in step P72 to eliminate a possible need for refluxing the solution.

Step P76 is an optional solvent exchange step. The use of a common solvent in a variety of precursor solutions is advantageous due to the predictability of fluid parameters such as viscosity and adhesion tension, which influence the thickness of the liquid precursor film after it is applied to a substrate. These fluid parameters also affect the quality and the electrical performance of the corresponding metal oxide film after annealing of the dried precursor residue. In step P76, the standard solvent, which is preferably xylenes or n-octane, is added in an amount that is appropriate to adjust the intermediate precursor to a desired molarity of superlattice ingredients. This molarity preferably ranges from about 0.100M to about 0.400M in terms of the empirical formula for the metal oxide material, and is most preferably about 0.130M to 0.200M in terms of moles of metal oxide material that may be formed from a liter of solution. After the addition of the standard solvent, the solution is heated to a temperature that is sufficient to distill away any non-standard solvents and leave a solution having the desired molarity.

Step P78 is preferably used only in the case of precursors for layered superlattice materials that include bismuth. Bismuth (Bi^{3+}) is the most preferred superlattice-generator element, and the bismuth pre-precursor will most preferably be bismuth tri-2-ethylhexanoate. The addition of bismuth pre-precursors subsequent to the heating of step P74 is preferred due to the relative instability of these pre-precursors, i.e., substantial heating could disrupt coordinate bonds with potential deleterious effects upon the ability of the solution to yield superior thin-film metal oxides. It should be understood that step P78 is optional in the sense that bismuth pre-precursors can often be added in any of steps P70 and P74 without problems.

Special problems exist with regard to the potential for bismuth volatilization during heating of the precursor solution and, especially, during high temperature annealing of the dried precursor residue in forming a layered superlattice material

of the desired stoichiometric proportions. Accordingly, in step P78, it is preferred to add from about 5% to about 15% excess bismuth for purposes of compensating the precursor solution for anticipated bismuth losses. At annealing temperatures ranging from about 600°C to about 850°C for a period of about one hour, this excess bismuth moiety in the precursor solution will typically range from 5% to 15% of the amount that is required for a stoichiometrically balanced layered superlattice product. In the event that the excess bismuth is not fully volatilized during the formation of a metal oxide product, the remaining excess bismuth moiety can act as an A-site material and, thus, induce point defects in the resulting layered superlattice crystal.

In step P80, the solution is mixed to substantial homogeneity, and is preferably stored under an inert atmosphere of desiccated nitrogen or argon if the final solution will not be consumed within several days or weeks. This precaution in storage serves to assure that the solution is kept essentially water-free and avoids the deleterious effects of water-induced polymerization, viscous gelling, and precipitation of metallic moieties that water can induce in alkoxide ligands. Even so, the desiccated inert storage precaution is not strictly necessary when the precursor, as is preferred, primarily consists of metals bonded to carboxylate ligands and alkoxycarboxylates.

The exemplary discussion of the reaction process, as given above, above is generalized and, therefore, non-limiting. The specific reactions that occur depend on the metals, alcohols, and carboxylic acids used, as well as the amount of heat that is applied. Detailed examples will be given below.

The following non-limiting examples set forth preferred materials and methods for practicing the present invention.

EXAMPLE 1

PREPARATION OF

A LAYERED SUPERLATTICE PRECURSOR SOLUTION

The precursor ingredients of Table 1 were obtained from the indicated commercial sources and subdivided to obtain the portions shown.

TABLE 1

Ingredient	Formula Weight (g/mol)	Grams	mmole	Molar Equiv.	Vendor
tantalum pentabutoxide $Ta(OC_4H_9)_5$	546.52	43.722	80.001	2.0000	Vnipim
2-ethylhexanoic acid	144.21	72.684	504.01	12.600	Aldrich
strontium	87.62	3.5048	40.000	1.0000	Strem
bismuth tri-2-ethyl-hexanoate (in naptha) $Bi(O_2C_8H_{11})_5$	(765.50)	66.752	87.201	2.1800	Strem

In Table 1, "FW" indicates formula weight, "g" indicates grams, "mmoles" indicates millimoles, and "Equiv." indicates the equivalent number of moles in solution.

The tantalum pentabutoxide and 252.85 mmol portion of 2-ethylhexanoic acid were placed in a 250 ml Erlenmeyer flask with 40 ml of xylenes, i.e., about 50 ml xylenes for each 100 mmol of tantalum. The flask was covered with a 50 ml beaker to assist in refluxing and to isolate the contents from atmospheric water. The mixture was refluxed with magnetic stirring on a 160°C hot plate for 48 hours to form a substantially homogenous solution including butanol and tantalum 2-ethylhexanoate. It should be understood that the butoxide moiety in solution was almost completely substituted by the 2-ethylhexanoic acid, but full substitution did not occur within the heating parameters of this example. At the expiration of 48 hours, the 50 ml beaker was removed and the hot plate temperature was then raised to 200°C for distillation of the butanol fraction and water to eliminate the same from solution. The flask was removed from the hot plate when the solution first reached a temperature of 124°C, as a temperature indicator that substantially all butanol and water had exited the solution. The flask and its contents were cooled to room temperature.

The strontium and 50 ml of 2-methoxyethanol solvent were added to the cooled mixture for reaction to form strontium di-2-ethylhexanoate. A 100 ml portion of xylenes was added to the strontium mixture, and the flask and its contents were

returned to the hot plate at 200°C and refluxed for five hours with the 50 ml beaker again in place for reaction to form a predominant tantalum-strontium alkoxycarboxylate product according to Formula (6). The beaker was removed and the solution temperature was allowed to rise to 125°C for elimination of the 2-methoxyethanol solvent from solution, as well as any ethers, alcohols, or water in solution. After removal from the heat source, the flask was permitted to cool to room temperature. The bismuth tri-2-ethylhexanoate was added to the cooled solution, which was further diluted to 200 ml with xylenes to form a precursor solution that was capable of forming 0.200 moles of $SrBi_{2.18}Ta_2O_{9.27}$ in the absence of bismuth volatilization.

Accordingly, this example indicates that step P70, i.e., the reaction of strontium metal, an alcohol, and a carboxylic acid, can occur in solution with the tantalum alkoxycarboxylate derived from tantalum pentabutoxide and 2-ethylhexanoic acid. Therefore, steps P70 and P72 can be conducted in a single solution, and in reverse of the FIG. 3 sequence.

The precursor formulation was designed to compensate for bismuth volatilization during a process of manufacturing solid metal oxides from the liquid precursor. Specifically, the $Bi_{2.18}$ moiety included an approximate nine percent excess (0.18) bismuth portion. After accounting for the anticipated bismuth volatilization during the forthcoming annealing steps, the precursor solution would be expected to yield a stoichiometric m = 2 material according to Formula (3), i.e., 0.2 moles of $SrBi_2Ta_2O_9$ per liter of solution.

EXAMPLE 2

FORMATION OF FERROELECTRIC CAPACITORS HAVING A LAYERED SUPERLATTICE MATERIAL BUFFER LAYER AND NO ADHESION METAL LAYER

A wafer including numerous square ferroelectric capacitors of the general layered sequence depicted in FIG. 1 was produced according to the method of FIG. 2. Step P48 was not conducted and, consequently, the capacitors did not include adhesion metal layer 36 (FIG. 1). A conventional four inch diameter polycrystalline wafer or substrate 32 was prepared to receive the $SrBi_2Ta_2O_9$ solution of Example 1. The preparation process included diffusion furnace baking at 1100°C in oxygen

according to conventional protocols for yielding a thick layer of silicon oxide 34 (see FIG. 1).

A 2 ml volume of a 0.2M $SrBi_2Ta_2O_9$ precursor prepared according to Example 1 was adjusted to a 0.13M concentration by the addition of 1.08 ml n-butyl acetate and passed through a 0.2 µm filter. An eyedropper was used to apply 2 ml of precursor solution to the substrate, which was then spun at 1500 rpm in a conventional spin-coater machine. The precursor-coated substrate was dried on a hot plate in air for thirty minutes at 400°C.

The substrate including buffer layer 24 was cooled to room temperature, and inserted into a vacuum chamber for conventional DC magnetron sputtering. A discharge voltage of 130 volts and a current of 0.53 amperes was used to sputter a 2000 Å thickness of platinum atop the titanium metal. This sputtering completed step P50 of FIG. 2, with optional Step P48 being skipped.

The substrate including the liquid thin film was annealed for thirty minutes at a temperature of 600°C in a diffusion furnace under an oxygen atmosphere. This time included a five minute push into the furnace and a five minute pull out of the furnace. The resultant structure included buffer layer 24 as depicted in FIG. 1. These actions completed the process of FIG. 2 through Step P52.

A 2 ml volume of the 0.2M $SrBi_2Ta_2O_9$ precursor from Example 2 was adjusted to a 0.13M concentration by the addition of 1.08 ml n-butyl acetate and passed through a 0.2 µm filter. An eyedropper was used to apply 2 ml of precursor solution to the substrate, which was then spun at 1500 rpm in a conventional spin-coater machine as before. The precursor-coated substrate was removed from the spin-coating machine and dried in air for two minutes on a 140°C hot plate. The substrate was dried for an additional four minutes on a second hot plate at 260°C. The substrate was dried for an additional thirty seconds in oxygen at 725°C using a 1200 W tungsten-halogen lamp (visible spectrum; Heatpulse 410 by AG Associates, Inc., using J208V bulbs by Ushio of Japan). The spin-coating and drying procedure was repeated a second time to increase the overall thickness of layer 28 to about 1800 Å.

Substrate 22 including the two coats of dried precursor residue was annealed in a diffusion furnace under an oxygen atmosphere to a temperature of 800°C for seventy minutes including a five minute push into the furnace and a five

minute pull out of the furnace. These actions completed the process of FIG. 2 through step P58.

Platinum metal was sputtered as top electrode 28 to a 2000 Å thickness of platinum over layer 26. A photoresist was applied and ion etched according to conventional protocols including removal of the resist. The patterned device was annealed in a diffusion furnace under an oxygen atmosphere at 800°C for thirty minutes including a five minute push into the furnace and a five minute pull out of the furnace. These actions completed the process of FIG. 2 through step P68, and provided a ferroelectric capacitor 20 of the type depicted in FIG. 1 having strontium bismuth tantalate as layer 26. Buffer layer 24 had a thickness of 500 Å, and was overlain by platinum layer 38 having a thickness of 2000 Å.

EXAMPLE 3

FORMATION OF FERROELECTRIC CAPACITORS
HAVING A LAYERED SUPERLATTICE MATERIAL
BUFFER LAYER AND AN ADHESION METAL LAYER

A wafer including strontium bismuth tantalate capacitors having the layered sequence depicted in FIG. 1 was produced according to a method including Step P48 of FIG. 2. The procedure was identical to that of Example 2, except that Step P50 was performed -- the capacitors included adhesion metal layer 36. A discharge voltage of 95 volts and a current of 0.53 amperes was utilized at a sputter pressure of 0.0081 Torr to sputter a 200 Å thickness of titanium metal as adhesion metal portion 36 on buffer layer 24. The sputtering of adhesion metal occurred just prior to the sputtering of platinum layer 38 in Step P52. Buffer layer 24 had a thickness of 500 Å, and was overlain by titanium adhesion metal layer 36 (200 Å) and platinum layer 38 (2000 Å).

EXAMPLE 4

FORMATION OF FERROELECTRIC CAPACITORS
HAVING AN ADHESION METAL LAYER AND
NO LAYERED SUPERLATTICE MATERIAL BUFFER LAYER

A wafer including ferroelectric capacitors without a buffer layer 24 (FIG. 1) was produced according to the general method of FIG. 2. The procedure was identical to that of Example 3, except Steps P44 and P46 were not performed. The resultant capacitor 20 lacked layer 24, but included a 200 Å adhesion metal layer

36 and a 2000 Å platinum layer 38. In this wafer, bottom electrode 26 was subjected to a first anneal in Step P52.

EXAMPLE 5

FORMATION OF FERROELECTRIC CAPACITORS HAVING AN ADHESION METAL LAYER AND NO LAYERED SUPERLATTICE MATERIAL BUFFER LAYER WITHOUT ANNEALING OF THE BOTTOM ELECTRODE

A wafer including ferroelectric capacitors without a buffer layer 24 (FIG. 1) was produced according to the method of Example 4, except Step 52 was not performed. The resultant capacitor 20 had the same layer sequence as the device of Example 4, but the electrode was not subjected to a first anneal in Step P52 before Step P54 was performed. The resultant capacitor 20 lacked layer 24, but included a 200 Å adhesion metal layer 36 and a 2000 Å platinum layer 38.

EXAMPLE 6

FORMATION OF FERROELECTRIC CAPACITORS HAVING AN ADHESION METAL LAYER AND NO LAYERED SUPERLATTICE MATERIAL BUFFER LAYER WITHOUT ANNEALING OF THE BOTTOM ELECTRODE

A wafer including ferroelectric capacitors without a buffer layer 24 (FIG. 1) was produced according to the method of Example 5, except only a 100 Å (not 200 Å) thickness of adhesion metal was sputtered in Step P48. The resultant capacitor 20 lacked layer 24, but included a 200 Å adhesion metal layer 36 and a 2000 Å platinum layer 38.

EXAMPLE 7

SCANNING ELECTRON MICROSCOPE COMPARISON OF BOTTOM ELECTRODE SURFACE IRREGULARITY FEATURES

Some shorting was observed in the capacitor squares on the wafer of Example 4. A second device was, accordingly, constructed according to Example 4 through Step P52, i.e., omitting Steps P44 and P46. The electrode structure was studied under a scanning electron microscope (SEM) at a magnification of about 40,000X. FIG. 4 depicts the SEM observations. Electrode 24 included titanium adhesion metal layer 36 and platinum layer 38. Electrode 26 presented an uppermost surface 82, which was covered with covered with sharp, irregularly

spaced, upwardly pointing hillocks, e.g., hillocks 84 and 86, which rose above surface 82 for a distance of approximately 900 Å. These hillocks were caused by different relative rates of thermal contraction between bottom electrode 26 and the underlying substrate, which included layers 32 and 34. The respective layers expanded upon heating. Upon cooling, the contraction of silicon-based layers 32 and 34 was greater than the contraction of metalization layers 36 and 38. Layer 36 adhered to layer 34, and the resultant interlayer stresses induced the formation of hillocks.

A thin film ferroelectric layer is intended to be liquid-deposited on surface 82 as layer 24. These films will preferably range in thickness from 500 Å to 3000 Å. Hillocks like hillocks 82 and 84 serve to reduce process yields by shorting across layer 28 and, further, present long term device reliability problems.

Similar SEM observations were conducted on other device samples that were produced according to each of the Examples 2 and 3 through the first anneal of Step P52. No sharp hillocks were observed in the electrodes of other samples. Some surface irregularities were observed, i.e., small, rounded features, but these features were estimated to rise less than about 50 Å to 80 Å above surface 82. These smaller rolling structures were negligible because they posed no serious threat to device performance, i.e., the electrodes of Examples 2 and 3 were essentially free of hillocks.

EXAMPLE 8

COMPARATIVE EVALUATION OF CAPACITOR DEVICES

The wafers from Examples 2, 3, 4, 5, and 6, each included a ferroelectric $SrBi_2Ta_2O_9$ material of approximately 1800 Å in thickness. Selected capacitors from each wafer were subjected to polarization hysteresis measurements on an uncompensated Sawyer-Tower circuit including a Hewlitt Packard 3314A function generator and a Hewlitt Packard 54502A digitizing oscilloscope. Measurements were obtained at 20°C using a sine wave function having a frequency of 10,000 Hz and voltage amplitudes of 0.25, 0.5, 1.0, 1.5, 2.0, 2.5, 3.0, 4.0, 5.0, and 7.0V.

FIG. 5 depicts a bar graph of the 2Pr polarization values (in $\mu C/cm^2$) that were obtained from 3V switching measurements. Each bar represents a three point average of data obtained from selected capacitors on a given wafer. Each bar has

been labeled with a corresponding letter, A, B, C, D, and E, as well as descriptive information for easy reference to identify the sample.

Differences between bars A and B indicate that the addition of 200 Å titanium adhesion metal layer 36 to the buffered bottom electrode 24 provided a 5.6% reduction in 2Pr polarization determined with respect to bar B. The unshorted capacitors that produced bar C (without a buffer layer) suffered a 30% decline in 2Pr polarization determined with respect to bar B. Accordingly, the addition of buffer layer 26 is responsible for the observed increase in polarization with respect to bar C.

The addition of titanium adhesion metal induces a corresponding reduction in polarization. Bars D and E represent polarization measurements that were obtained from identical capacitors, except the capacitors of bar D contained a 200 Å thickness of adhesion metal and those of bar E contained a 100 Å thickness. The additional 100 Å thickness of titanium adhesion metal (bar D) caused a 43% decline in polarization determined with respect to bar E. The use of buffer layer 26 (bars A and B) overcomes the deleterious titanium effects.

The foregoing discussion can be utilized to provide less preferred variations of the present invention. For example, the adhesion metal can include titanium oxide, tantalum, tantalum oxide, or other known adhesion metals. Layer 26 may actually be formed of a plurality of different layers, and not all such layers must necessarily be the same type of layered superlattice material. Furthermore, the geometries and relative thicknesses that are depicted in FIGS. 1 and 4 are presented for illustrative purposes only. These figures are not intended to reflect scale models of the actual materials which may vary considerably in geometry and thickness.

Those skilled in the art will understand that the preferred embodiments, as described above, may be subjected to apparent modifications without departing from the true scope and spirit of the invention. Accordingly, the inventors hereby state their intention to rely upon the Doctrine of Equivalents for purposes of protecting their full rights in the invention.

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CLAIMS:

1. An integrated circuit device (20) comprising:

a substrate (22) and a metal wiring layer (26),

said integrated circuit device characterized by

a layer sequence (24) consisting of material interposed between said substrate and said metal wiring layer, said layer sequence including at least one buffer layer made of a layered superlattice material, said layer sequence being essentially free of additional wiring layers.

2. The device as set forth in Claim 1 wherein said layered superlattice material includes strontium bismuth tantalate.

3. The device as set froth in Claim 2 wherein said substrate includes an uppermost silicon-based layer (34) proximate said layer sequence.

4. The device as set forth in Claim 1 wherein said wiring layer includes an adhesion metal (36).

5. The device as set forth in Claim 4 wherein said metal wiring layer includes a noble metal (38).

6. The device as set forth in Claim 1 including a ferroelectric layer (28) atop said wiring layer.

7. The device as set forth in Claim 6 wherin said ferroelectric layer includes a layered superlattice material.

8. A method of making an integrated circuit device (20), said method including the step of providing (P40) a substrate (22) having a nonmetallic uppermost surface (34);

said method characterized by:

depositing (P44, P46) a layered superlattice material precursor (36) atop said substrate; and

depositing (P50) an electrode (38) over said layered superlattice material.

9. The method as set forth in Claim 14 wherein said depositng step includes a step of applying (P44) a liquid precursor on said substrate to form a thin precursor film, said liquid precursor including a plurality of metals in effective amounts for yielding said layered superlattice material upon thermal treatment of said precursor, and drying (P46) said thin precursor film to yield a layered superlattice material (36).

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10. The method as set forth in Claim 8 further characterized by annealing (P52) said integrated circuit device at a temperature of at least 450°C after said step of depositing said electrode.

11. The method as set forth in Claim 10 wherein said temperature is at least about 600°C.

12. The method as set forth in Claim 9 wherein said drying step includes drying said precursor at a temperature up to about 450°C for a period of time sufficient to remove substantially all volatile organic components from said film.

13. The method as set forth in Claim 8 further characterizd by a step of constructing (P54) a second layered superlattice material (28) atop said electrode.

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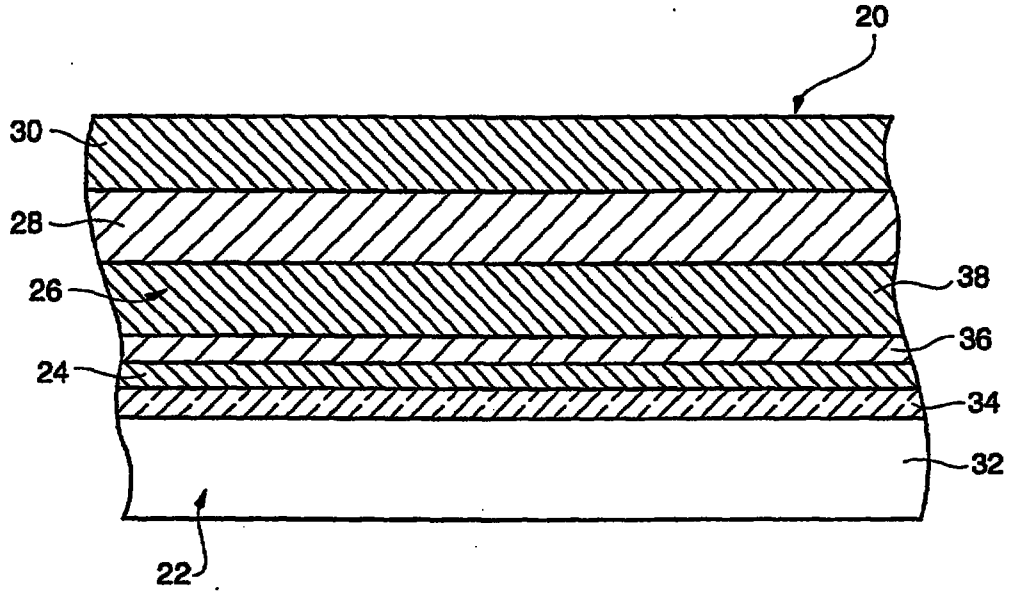


FIG. 1

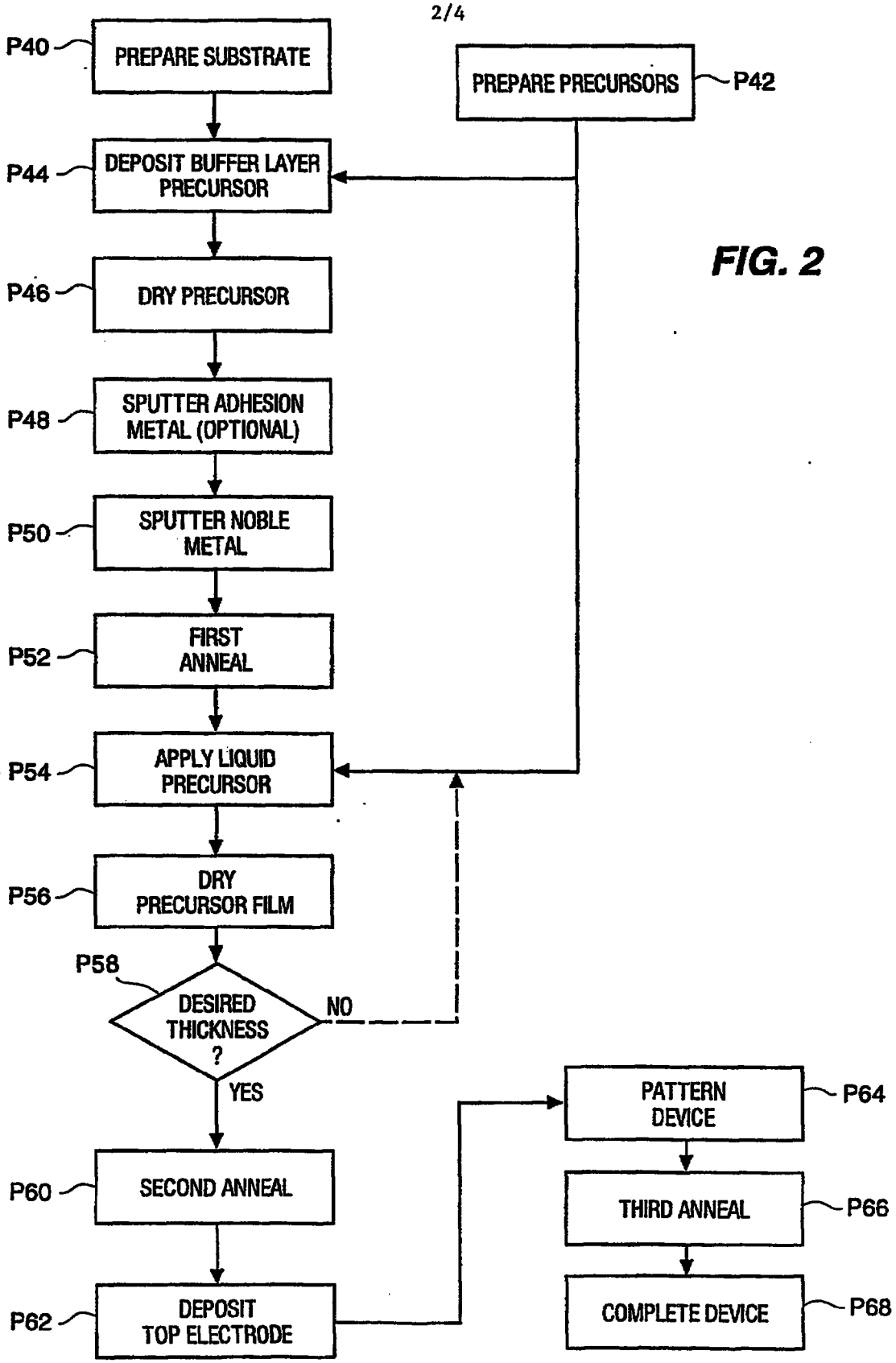
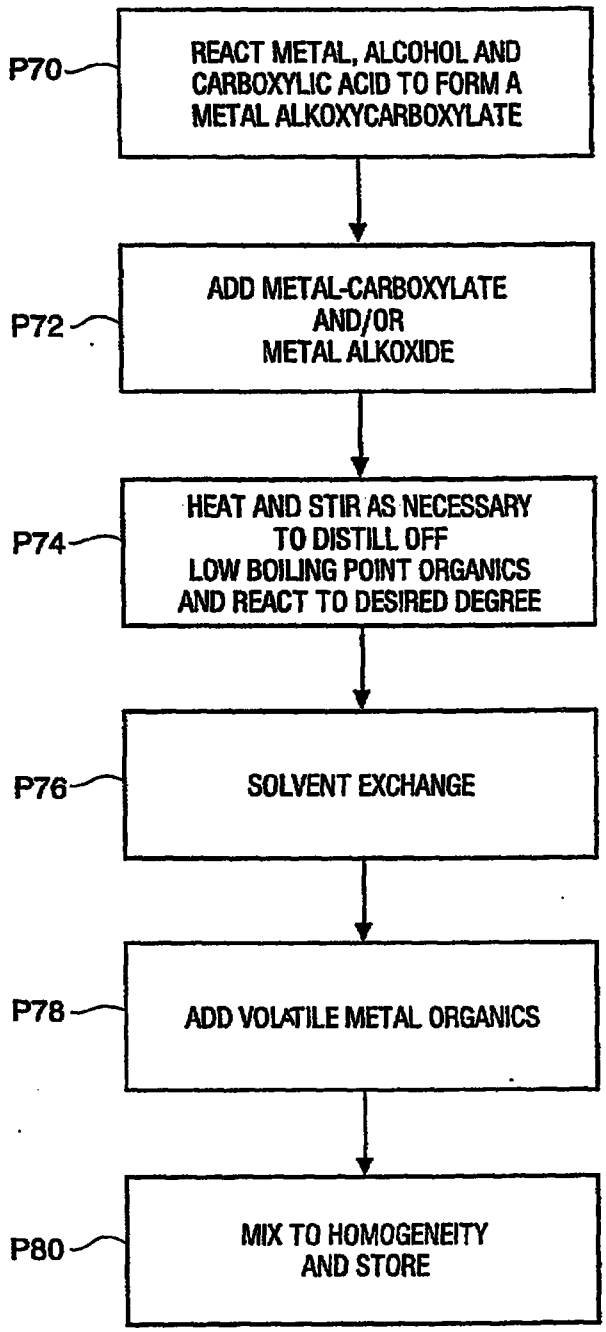

P40
PREPARE SUBSTRATE
PREPARE PRECURSORS
P42
P44
DEPOSIT BUFFER LAYER PRECURSOR
P46
DRY PRECURSOR
P48
SPUTTER ADHESION METAL (OPTIONAL)
P50
SPUTTER NOBLE METAL
P52
FIRST ANNEAL
P54
APPLY LIQUID PRECURSOR
P56
DRY PRECURSOR FILM
P58
DESIRED THICKNESS ?
NO
YES
P60
SECOND ANNEAL
P62
DEPOSIT TOP ELECTRODE
PATTERN DEVICE
P64
THIRD ANNEAL
P66
COMPLETE DEVICE
P68

FIG. 2

FIG. 3


P70
REACT METAL, ALCOHOL AND CARBOXYLIC ACID TO FORM A METAL ALKOXYCARBOXYLATE
P72
ADD METAL-CARBOXYLATE AND/OR METAL ALKOXIDE
P74
HEAT AND STIR AS NECESSARY TO DISTILL OFF LOW BOILING POINT ORGANICS AND REACT TO DESIRED DEGREE
P76
SOLVENT EXCHANGE
P78
ADD VOLATILE METAL ORGANICS
P80
MIX TO HOMOGENEITY AND STORE

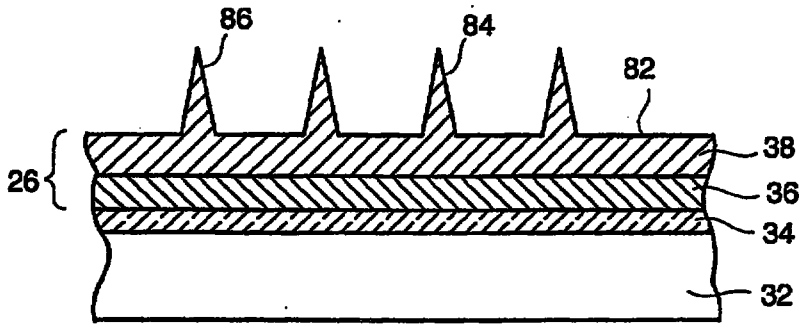

86
84
82
26
38
36
34
32

FIG. 4

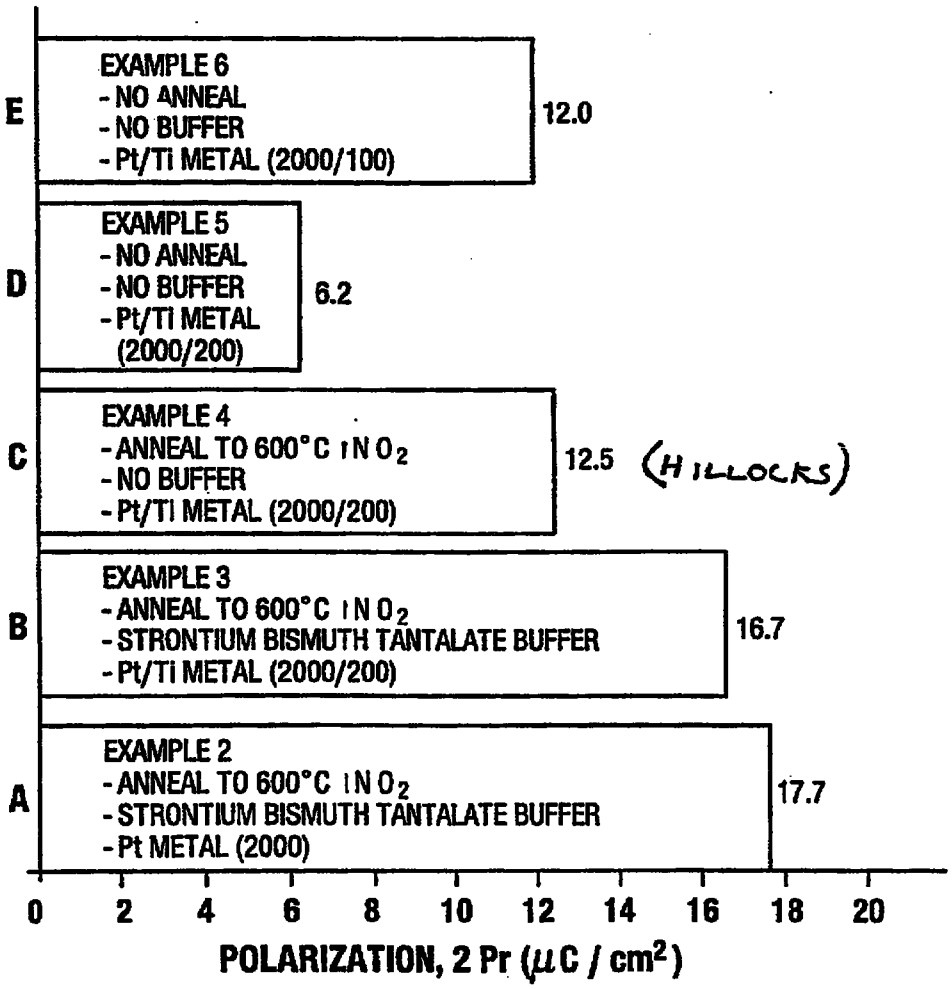

E
EXAMPLE 6
- NO ANNEAL
- NO BUFFER
- Pt/Ti METAL (2000/100)
12.0
D
EXAMPLE 5
- NO ANNEAL
- NO BUFFER
- Pt/Ti METAL (2000/200)
6.2
C
EXAMPLE 4
- ANNEAL TO 600°C IN O_2
- NO BUFFER
- Pt/Ti METAL (2000/200)
12.5 (HILLOCKS)
B
EXAMPLE 3
- ANNEAL TO 600°C IN O_2
- STRONTIUM BISMUTH TANTALATE BUFFER
- Pt/Ti METAL (2000/200)
16.7
A
EXAMPLE 2
- ANNEAL TO 600°C IN O_2
- STRONTIUM BISMUTH TANTALATE BUFFER
- Pt METAL (2000)
17.7
0 2 4 6 8 10 12 14 16 18 20
POLARIZATION, 2 Pr (μC / cm^2)

FIG. 5

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+3, and +4, which induce corresponding lattice defects. Metal nitride diffusion barrier layers have been constructed in attempts in attempts to isolate the adhesion layer metals. See for example the United States patent to Larson, 5,005,102, and Garceau et al, "TiN As A Diffusion Barrier Layer In The Ti-Pt-Au Beam Less Metal System", 60 Thin Solid Films, 237 - 247, No. 2, (1979), which both teach the use of a titanium nitride diffusion barrier layer. Annealing of metal nitrides can yield surface irregularities, e.g., hillocks, that induce shorting of dielectric or ferroelectric capacitors.

The magnitude of polarization that is available from a thin-film ferroelectric material is a limiting factor that controls the memory density for a given voltage. Larger polarizations can be used to make denser memories. Nevertheless, it is also necessary for the ferroelectrics to adhere well to a substrate, and reduced polarization can derive from the necessity of adding diffusible materials that promote adhesion between the proximal faces of two separate layers. Hence, a materials selection conflict arises between the need for adherance and the need for high polarization.

As shown in WO 93/12538, the layered superlattice materials discussed by G.A. Smolenskii, V.A. Isupov, and A.I. Agranovskaya (See Chapter 15 of the book, Ferroelectrics and Related Materials, ISSN 0275-9608, [V.3 of the series Ferroelectrics and Related Phenomena, 1984] edited by G. A. Smolenskii, especially sections 15.3 -15) are far better suited for ferroelectric and high dielectric constant integrated circuit applications than any prior ferroelectrics. These layered superlattice materials comprise complex oxides of metals, such as strontium, calcium, barium, bismuth, cadmium, lead, titanium, tantalum, hafnium, tungsten, niobium zirconium, bismuth, scandium, yttrium, lanthanum, antimony, chromium, and thallium. The metals oxidize in an anneal to form layered superlattice compounds, i.e. crystalline lattices including alternating layers of distinctly different sublattices. These sublattices are properly referred to as compounds because the sublattices are covalently bound to one another, as opposed to being a mixture of different sublayers that are deposited as different materials in separate deposition steps. Generally, each layered superlattice material will include two or more of the above metals; for example, strontium,

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bismuth and tantalum form the layered superlattice material strontium bismuth tantalate, $SrBi_2Ta_2O_9$.

Ramesh, in US 5,248,564, (see FIG. 2 and columns 3-4 thereof) describes an ultrathin layer of bismuth titanate layered perovskite material that is deposited to enhance the crystallinity of perovskites that are deposited on top of the bismuth titanate. A laser is pulsed to promote c-axis orientation in the bismuth titanate and temperatuyre is carefully controlled to promote eptiaxial crystal growth in the bismuth titanate. Thus, the perovskite that is deposited atop the bismuth titanate also has eptiaxial growth.

There remains a need for an effective bottom electrode structure that adheres well, does not have short-inducing surface irregularities, and has a high polarization.

SOLUTION TO THE PROBLEM

The present invention overcomes the problems that are outlined above by providing a buffer layer and an adhesion metal-containing electrode which is substantially free of surface irregularities. The addition of a buffer layer provides substantial improvements of up to 100% or more in the polarization performance of ferroelectric capacitors, as compared with similarly processed ferroelectric capacitors that lack the buffer layer.

The electrode structure broadly pertains to an integrated circuit device that includes a substrate, a metal electrode or wiring layer, and a layer sequence consisting of material interposed between the substrate and the wiring layer. The layer sequence includes at least one buffer layer made of a layered superlattice material, and is essentially free of additional wiring layers.

Particularly preferred forms of the electrode structure include the layered superlattice material being strontium bismuth tantalate. Other preferred layered

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REPLACEMENT SHEET
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CLAIMS:

1. An integrated circuit device (20) comprising:

a silicon substrate (22) and a metal wiring layer (26),

said integrated circuit device **characterized by**

a layer sequence (24) consisting of the entirety of material interposed between said silicon substrate and said metal wiring layer, said layer sequence including a buffer layer made of a layered superlattice material compound, said layer sequence being free of additional wiring layers.

2. The device as set forth in Claim 1 wherein said layered superlattice material includes strontium bismuth tantalate.

3. The device as set froth in Claim 2 wherein said substrate includes an uppermost silicon-based layer (34) proximate said layer sequence.

4. The device as set forth in Claim 1 wherein said wiring layer includes an adhesion metal (36).

5. The device as set forth in Claim 4 wherein said metal wiring layer includes a noble metal (38).

6. The device as set forth in Claim 1 including a ferroelectric layer (28) atop said wiring layer.

7. The device as set forth in Claim 6 wherein said ferroelectric layer includes a layered superlattice material.

8. A method of making an integrated circuit device (20), said method including the step of providing (P40) a silicon substrate (22) having an uppermost surface (34),

said method **characterized by**:

depositing (P44, P46) a layered superlattice material compound precursor (36) directly on said substrate;

forming (P46) a residue of said layered superlattice material compound precursor; and

depositing (P50) an electrode (38) directly over said residue.

9. The method as set forth in Claim 14 wherein said step of depositing a layered superlattice material compound precursor includes a step of applying (P44) a liquid precursor on said substrate to form a precursor film, said liquid

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precursor including a plurality of metals in effective amounts for yielding said layered superlattice material upon thermal treatment of said precursor, and drying (P46) said thin precursor film to yield a layered superlattice material (36).

10. The method as set forth in Claim 8 further characterized by annealing (P52) said integrated circuit device at a temperature of at least 450°C after said step of depositing said electrode.

11. The method as set forth in Claim 10 wherein said temperature is at least about 600°C.

12. The method as set forth in Claim 9 wherein said drying step includes drying said precursor at a temperature up to about 450°C for a period of time sufficient to remove substantially all volatile organic components from said film.

13. The method as set forth in Claim 8 further characterized by a step of constructing (P54) a second layered superlattice material (28) atop said electrode.

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+3, and +4, which induce corresponding lattice defects. Metal nitride diffusion barrier layers have been constructed in attempts in attempts to isolate the adhesion layer metals. See for example the United States patent to Larson, 5,005,102, and Garceau et al, "TiN As A Diffusion Barrier Layer In The Ti-Pt-Au Beam Less Metal System", **60** Thin Solid Films, 237 - 247, No. 2, (1979), which both teach the use of a titanium nitride diffusion barrier layer. Annealing of metal nitrides can yield surface irregularities, e.g., hillocks, that induce shorting of dielectric or ferroelectric capacitors.

The magnitude of polarization that is available from a thin-film ferroelectric material is a limiting factor that controls the memory density for a given voltage. Larger polarizations can be used to make denser memories. Nevertheless, it is also necessary for the ferroelectrics to adhere well to a substrate, and reduced polarization can derive from the necessity of adding diffusible materials that promote adhesion between the proximal faces of two separate layers. Hence, a materials selection conflict arises between the need for adherance and the need for high polarization.

There remains a need for an effective bottom electrode structure that adheres well, does not have short-inducing surface irregularities, and has a high polarization.

SOLUTION TO THE PROBLEM

The present invention overcomes the problems that are outlined above by providing a wiring layer on a silicon substrate with a buffer layer between the electrode and the substrate, which buffer layer causes the electrode to be substantially free of surface irregularities. Optionally, the electrode may contain an adhesion metal. In the preferred embodiment, the wiring layer is the bottom electrode of a capacitor. The addition of a buffer layer provides substantial improvements of up to 100% or more in the polarization performance of ferroelectric capacitors, as compared with similarly processed ferroelectric capacitors that lack the buffer layer.

The electrode structure broadly pertains to an integrated circuit device that includes a substrate, a metal electrode or wiring layer, and a layer sequence consisting of material interposed between the substrate and the wiring layer. The

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layer sequence includes at least one buffer layer made of a layered superlattice material, and is essentially free of additional wiring layers.

Particularly preferred forms of the electrode structure include the layered superlattice material being strontium bismuth tantalate. Other preferred layered

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CLAIMS:

1. An integrated circuit device (20) comprising:

a silicon substrate (22) and a metal wiring layer (26),

said integrated circuit device **characterized by**

a layer sequence (24) located directly on said silicon substrate, said metal wiring layer located directly on said layer sequence, said layer sequence including a buffer layer made of a layered superlattice material, said layer sequence being free of additional wiring layers.

2. The device as set forth in Claim 1 wherein said layered superlattice material includes strontium bismuth tantalate.

3. The device as set forth in Claim 2 wherein said silicon substrate includes an uppermost silicon-based layer (34) adjacent said layer sequence.

4. The device as set forth in Claim 1 wherein said wiring layer includes an adhesion metal (36) and a noble metal (38).

5. A method of making an integrated circuit device (20), said method including the step of providing (P40) a silicon substrate (22) having an uppermost surface (34),

said method **characterized by**:

depositing (P44, P46) a layered superlattice material precursor (36) directly on said substrate;

heating (P46) said layered superlattice material precursor to yield a residue of said layered superlattice material precursor; and

depositing (P50) a metal wiring layer (38) directly over said residue.

6. The method as set forth in Claim 5 further characterized by annealing (P52) said integrated circuit device at a temperature of at least 450°C after said step of depositing said metal wiring layer.

7. The method as set forth in Claim 6 wherein said temperature is at least about 600°C.

8. The method as set forth in Claim 7 wherein said step of heating said layered superlattice material precursor includes drying said precursor at a temperature up to about 450°C for a period of time sufficient to remove substantially all volatile organic components from said film.

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9. The integrated circuit as in Claim 1 or the method as set forth in Claim 5, further characterized in that said integrated circuit of Claim 1 includes a second layered superlattice material (28) atop said metal wiring layer or said method of Claim 5 includes a step of constructing (P54) a second layered superlattice material (28) atop said wiring layer.

SG 9705858-0
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International Bureau

INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(51) International Patent Classification 6 :
H01L 23/532, 21/3205, 29/92, 27/115

A1

(11) International Publication Number: WO 96/41375

(43) International Publication Date: 19 December 1996 (19.12.96)

(21) International Application Number: PCT/US96/09100

(22) International Filing Date: 6 June 1996 (06.06.96)

(30) Priority Data:
08/473,432 7 June 1995 (07.06.95) US

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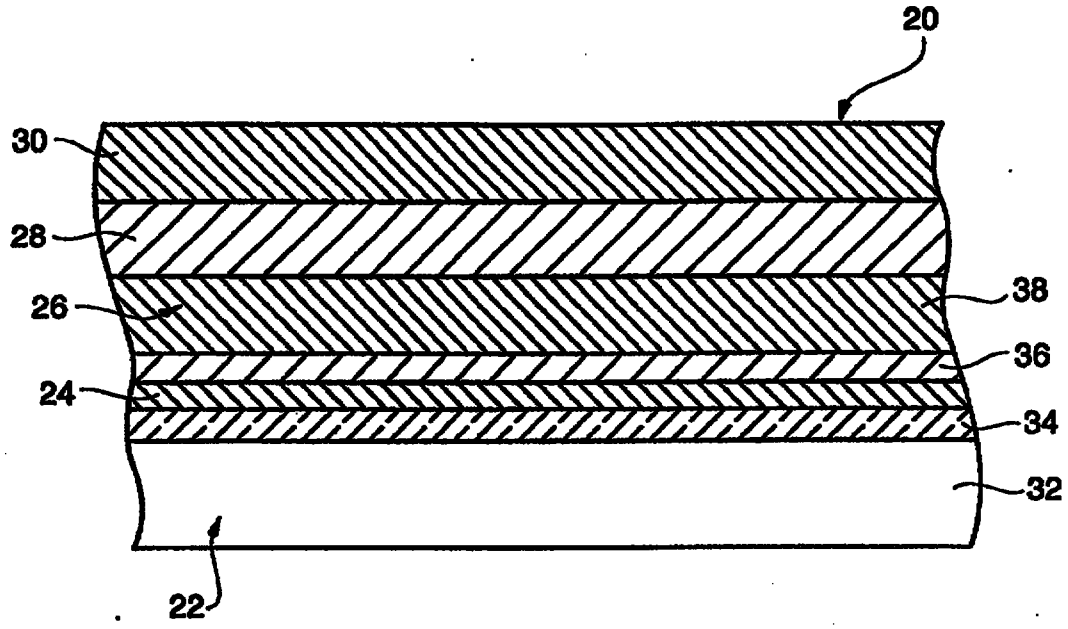
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(81) Designated States: CA, CN, JP, KR, SG, European patent (AT, BE, CH, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE).

Published
With international search report.

(54) Title: INTEGRATED CIRCUIT COMPRISING A SUBSTRATE AND A WIRING LAYER WITH A BUFFER LAYER BETWEEN THE SUBSTRATE AND THE WIRING LAYER



(57) Abstract

A thin-film ferroelectric capacitor (20) includes a bottom electrode structure (26) having an adhesion metal layer (36) and a noble metal portion (38). The electrode (26) is deposited over a thin-film buffer layer (24), which contains a layered superlattice material. The buffer layer is interposed between a substrate (22) and the bottom electrode (26). A process of manufacture includes deposition of a liquid precursor on the substrate (22) prior to formation of the bottom electrode (26).