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(21) International Application Number: PCT/US99/22946 (22) International Filing Date: 12 October 1999 (12.10.99) (30) Priority Data: 09/172,178 13 October 1998 (13.10.98) US (63) Related by Continuation (CON) or Continuation-in-Part (CIP) to Earlier Application US 09/172,178 (CON) Filed on 13 October 1998 (13.10.98) (71) Applicant (for all designated States except US): KULICKE & SOFFA HOLDINGS, INC. [US/US]; 2101 Blair Mill Road, Willow Grove, PA 19090 (US). (72) Inventors; and (75) Inventors/Applicants (for US only): LYKINS, James, L., II [US/US]; 2677 Norcross Drive, San Jose, CA 95148 (US). STRANDBERG, Jan, I. [SE/US]; 21327 Glen Place #6, Cupertino, CA 95014 (US). (74) Agents: SHAFFER, William, L. et al.; Townsend and Townsend and Crew LLP, 8th floor, Two Embarcadero Center, San Francisco, CA 94111-3834 (US).		(81) Designated States: AE, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, CA, CH, CN, CR, CU, CZ, DE, DK, DM, EE, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, NO, NZ, PL, PT, RO, RU, SD, SE, SG, SI, SK, SL, TJ, TM, TR, TT, TZ, UA, UG, US, UZ, VN, YU, ZA, ZW, ARIPO patent (GH, GM, KE, LS, MW, SD, SL, SZ, TZ, UG, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GW, ML, MR, NE, SN, TD, TG). Published <i>With international search report.</i> <i>Before the expiration of the time limit for amending the claims and to be republished in the event of the receipt of amendments.</i>
(54) Title: DEPOSITED THIN BUILD-UP LAYER DIMENSIONS AS A METHOD OF RELIEVING STRESS IN HIGH DENSITY INTERCONNECT PRINTED WIRING BOARD SUBSTRATES (57) Abstract The present invention provides a method for minimization of cracking due to the mechanical stresses at the interfaces of the metal and dielectric materials in the printed wiring substrates of high density interconnects. A high density interconnect printed wiring board substrate has a first patterned conductive layer (6) formed over an upper surface of the substrate. The patterned conductive layer (6) includes multiple conductive lines each having edges that define the boundaries of the conductive lines. The method of the invention forms a composite dielectric layer (2) over the first patterned conductive layer (6) and between the edges of the conductive layer (6). The composite dielectric layer (2) includes particles suspended in the layer in order to reduce the likelihood and prevent any cracks that form in the layer from propagating through the entire length of the layer. A thin film conductive layer (4) is then formed over the composite dielectric layer (2) and a thin film dielectric layer (5) is formed over the thin film conductive layer (4). In a preferred embodiment, the composite dielectric layer (2) is a Ciba Probimer layer deposited from a curtain coating process.		

