

**METHOD AND APPARATUS FOR TESTING A MEGACELL IN
AN ASIC USING JTAG**

BACKGROUND OF THE INVENTION

Field of the Invention

5 The present invention relates to improvements in testing of integrated circuits. Specifically, the invention involves a method and apparatus for testing a megacell within an application specific integrated circuit "ASIC" at the chip level.

Description of Related Art

10 The increasing complexity of circuit designs and new integrated circuit packaging techniques leads to an ever increasing problem of testing integrated circuits and printed circuit boards. Software testing of digital hardware is constantly improving, however the complexity of the circuitry makes testing more difficult unless the components are designed with testability in mind.

 One method for testing circuitry which has received notable attention is the IEEE 1149.1 Boundary-Scanned Standard originated by the International Joint Tests Action Group (JTAG), (hereby incorporated by reference). One
15 implementation of this standard involves designing components (e.g., integrated circuits) for serial boundary-scanned testing by providing shift-register elements daisy chained to form a path around the periphery of an integrated circuit component. The idea behind the serial testing is to shift serial data into and through a number of integrated circuit components. The serial data is applied to inputs of known circuitry to effect outputs as determined by the circuit functions. A master testing circuit compares the return data to an expected result (i.e., a result which is dependent
20 upon the functions of the known circuitry). In other words, the serial data inputs applied to the circuit being tested produces known outputs if the circuit is functioning properly. If the data stream returned to the master testing circuit is not as expected, then a malfunction in the circuit is detected by the testing circuit. A careful analysis (under software control) of the deviations in the data stream may isolate any malfunctions within a circuit.

 Boundary-scanned testing of components, as briefly explained above, can also be expanded to testing of
25 a very large scale integrated (VLSI) circuitry such as an ASIC. An ASIC includes internal logic circuitry which is normally inaccessible via the output pins supplied on the IC package. Such internal logic circuitry within the ASIC is typically vendor-supplied as a module having defined inputs and outputs, and is commonly referred to as a megacell. In some circuit boards, the test inputs and outputs for the vendor-supplied megacell within the ASIC are connected to special pins on the IC package so that the megacell is accessible for testing purposes by the
30 manufacturer via external pins on the IC package. However, the extra pins required to test the cell are typically of no use during normal implementation and operation of the IC. Furthermore, the additional test pins sometimes require the manufacturer to increase the IC package to the next larger size die and or package because of the increased number of pins. Thus, the IC package takes additional printed circuit board real estate and costs are increased because a larger die size is generally more expensive.

35 Furthermore, the standard JTAG specification allows a megacell within an ASIC to be surrounded internally with JTAG cells. However, use of this test architecture is incompatible with the way a vendor typically tests

Under a further aspect, the invention is a method of testing a megacell within an integrated circuit having the megacell as an integral component of circuitry within the integrated circuit. The megacell has at least one test output signal having no connection external to the integrated circuit during operation of the integrated circuit. The integrated circuit has a plurality of signals which are provided as outputs on respective pins of the integrated circuit during the operation of the integrated circuit. The method comprises applying a serial instruction to the integrated circuit via a JTAG input pin to place the integrated circuit into a predetermined test mode; selectively disabling one of the plurality of output signals from a respective first pin of the integrated circuit; selectively routing the test output from the megacell to the respective first pin of the disabled output signal; applying a test input to the megacell via a second pin of the integrated circuit to stimulate the megacell to perform a test operation; and monitoring the test output of the megacell at the respective first pin of the integrated circuit.

Brief Description of the Drawings

Figure 1 is a schematic block diagram which illustrates the configuration of a JTAG test circuit.

Figure 2 is a schematic block diagram which shows an IC circuit having a megacell with test input/output terminals connected to external pins of the IC.

Figure 3 is a state diagram showing the operation of the TAP controller circuit used to control the JTAG test circuit.

Figure 4 is a schematic block diagram showing an improved JTAG test circuit which provides a connection of an internal megacell with an external pin.

Detailed Description of the Invention

Figure 1 is a schematic block diagram showing an integrated circuit (IC) chip 100 configured for testing using a JTAG IEEE 1149.1 daisy-chain boundary-scan serial testing system. The exemplary JTAG system shown in Figure 1 comprises a master pattern generator/comparator 102 which outputs a data/instruction signal over a line 105, a mode signal over a line 107, and a clock signal over a line 109. It should be understood that according to conventional terminology, the data/instruction signal line 105 is also referred to as the TDI signal line, the mode signal line 107 is referred to as the TMS signal line, and the clock signal line 109 is referred to as the TCK signal line. The output lines 105, 107, and 109 of the pattern generator/comparator 102 connect to external input pins extending from the IC 100 so that a TAP controller state machine 110 within the IC 100 receives the signals via the lines 105, 107, and 109.

The TAP controller state machine 110 connects to a data shift register 115 via a serial data line 117 and a clock enable line 119. The TAP controller state machine 110 further connects to an instruction shift register 120 via a serial instructions line 122 and a clock enable line 124. It should be noted here that, typically, the TDI line 105, the serial data line 117, and the serial instructions line 122 are connected to a common node and the lines 105, 117, and 122 differ only insofar as they are considered as carrying data, instructions, or both.

The data shift register 115 is connected in parallel with a latched data register 130, while the instruction shift register 120 connects in parallel with a latched instruction register 140. Each of the bit storage locations within the latched data register 130 connects to a first input of a multiplexer within the IC 100. For example, as

the multiplexer 145 shown in Figure 1) receives a JTAG input which is connected to the latched data register 130. Thus, for example, the multiplexer 145 is enabled by the decoder 150 via the line 152 to select the input 147 connecting to a storage location within the register 130. Thus, the output 165 of the multiplexer 145 is forced to the bit value stored within the register 130. In this manner, the output connections of the IC 100 over the line 165 may be tested for defects. For example, if the storage location connected to the multiplexer 145 via the line 147 contains a high voltage level bit (i.e., corresponding to a digital 1), then the output of the multiplexer 145 along the line 165 should be detected at the output pin of the IC 100 to be a digital 1. If this output pin does not generate a digital 1, then the test circuitry to which the IC 100 is connected will register an error so that the IC 100 may be designated as defective. This test is performed for each of the inputs and outputs designated by the decoder 150 in response to the instructions loaded by the pattern generator/comparator 102.

Of course, although not depicted in Figure 1, it will be understood that multiple ICs may be connected in series in a daisy-chain configuration so that the pattern generator/comparator 102 can shift in data and instructions for multiple ICs at one time. Thus, the IC 100 includes a multiplexer 170 which selectively shifts out the data passing through the register 115 or the instructions passing through the register 120 via the lines 172 or 174 under the control of the TAP controller state machine 110. Finally, the data output from the last IC is transferred back to the pattern generator/comparator 102 via the serial return line 175.

Figure 2 is a schematic block diagram which depicts an IC 200 including a vendor-supplied megacell 210 in addition to normal integrated circuitry 220. The megacell 210 operates as a functional unit within the IC 200 which receives inputs from and provides inputs to the normal circuitry 220 via lines 225.

The vendor-supplied megacell 210 is distinguished from the normal circuitry 220 in that the vendor-supplied megacell 210 has a standardized structure and function provided by the vendor, while the normal circuitry is custom designed by an ASIC designer. Thus, the megacell module has an independent functionality (i.e., the megacell could be used to perform the same function in a variety of different surrounding circuit configurations so that this functionality is substantially independent from the other circuitry within the IC 200). Furthermore, a separate set of test vectors than those used to test the overall IC 200 are typically used to separately test the functionality of the megacell 210.

Thus, for example, an ASIC designer uses standard functional logic blocks such as UARTS, phase locked loops, etc., as a part of the ASIC design. An ASIC vendor supplies structure for these standard functional logic blocks, which the ASIC designer incorporates into a custom ASIC. These standard functional blocks are referred to as megacells, and the megacell vendor typically supplies test vectors which are used by the chip foundry during the manufacturing process to test the megacell within the ASIC. Typically, the ASIC can be tested as an entire unit, but if malfunctions are discovered in the entire unit, it will be difficult to determine if the malfunctions are due to custom circuitry whose structure is provided by the ASIC designer or due to the cell vendor-supplied megacell circuitry. For this reason, the megacells are tested independently using the test vectors provided by the cell vendor. Additionally, the ASIC designer need not expend the effort to exhaustively test the megacell since this testing will be done via the vendor supplied tests.

the line 117. The TAP controller 110 continues in the shift data register state 320 as long as TMS is held low. Thus, as many data bits as are necessary to load the prespecified test vectors into the shift registers 115 are shifted into the register 115 while TMS is held low in the state 320.

5 When the TAP controller 110 is in the shift data register state 320 and a rising edge is applied to TCK while TMS is held high, then the TAP controller state machine 110 enters the exit data register state 325. The exit data register state 325 is a temporary controller state. If TMS is held high, a rising edge applied to TCK causes the TAP controller 110 to enter an update data register state 340, while if TMS is held low while the rising edge is applied to TCK then the TAP controller 110 enters a pause data register state 330. The pause data register state 330 allows the shifting of the test data register 315 to be temporarily halted. The TAP controller 110 remains in
10 pause data register state 330 while TMS is held low. When TMS is held high and a rising edge is applied to TCK, then the TAP controller state machine 110 enters an exit 2 data register state 335 which is also a temporary controller state. If a rising edge is applied to TCK while TMS is held low, then the TAP controller state machine 110 returns to the shift data register state 320. However, if TMS is held high while a rising edge is applied to TCK, then the TAP controller state machine 110 transitions from the exit 2 data register state 335 to the update
15 data register state 340. As shown in Figure 1, the shift data register 115 includes a latched parallel output to prevent changes to the data in the data register 130 while data is shifted in the associated shift register path 115 in response to certain instructions with the instruction register 140. Thus, in the update data register state 340, data is latched from the shift register 115 onto the parallel output of the shift register 115 on the falling edge of TCK. Thus, this data is stored within the latched data register 130 so that the data within the register 130 does
20 not change other than in the update data register state unless operation during the execution of a self-test is required (e.g., during the idle state in response to a design-specific public instruction). As with each of the states 305-335, the instructions stored within the instruction shift register 120 and the instruction latch data register 140 do not change while the TAP controller 110 is within the update data register state 340. When the TAP controller is in the update data register state and a rising edge is applied to TCK, the TAP controller 110 enters the select data
25 register scan state 305 when TMS is held high, or the idle state 300 when TMS is held low.

If TMS is held high, and a rising edge is applied to TCK while the TAP controller state machine 110 is in the select data register state 305, then the TAP controller state machine 110 transitions to the select instruction register scan state 310.

30 If the TAP controller state machine 110 transitions into the capture instruction register state 345, then, in this state, instructions may be parallel-loaded into the instruction register 140 from the shift instruction register 120 on the rising edge of TCK. If the JTAG test circuitry does not include a parallel-loaded instruction register 140, or if capturing is not required for the selected test, then the instruction shift register 120 retains its previous state unchanged. Furthermore, the bits stored within the data registers 130, 115 remain unchanged while the TAP controller state machine 110 is in the captured instruction register state 345. When the TAP controller 110 is in
35 the capture instruction register state 345 while TMS is held low and a rising edge is applied to TCK, then the controller enters a shift instruction register state 350. However, if TMS is held high while the rising edge is applied

in the test logic reset state 342 while TMS is held high. By holding TMS low during a rising edge on TCK, the TAP controller state machine 110 will enter the idle state 300.

Figure 4 is a schematic block diagram which shows an exemplary internal JTAG test circuit within an IC 400. For simplicity of illustration of the present invention, the TAP state controller 110, the data and instruction shift registers 115, 120, and other associated JTAG circuitry are not shown in Figure 4. However, it will be understood by those of ordinary skill in the art that the IC 400 includes the aforementioned JTAG circuitry having substantially the same operation as described above. The IC 400 may, for example, comprise an application-specific integrated circuit (ASIC) which includes custom-digital circuitry designed by an ASIC designer (represented in Figure 4 as normal circuitry 410) and a vendor-supplied structure for a megacell which the ASIC designer incorporates into the custom ASIC (represented as the megacell circuitry 420 in Figure 4). The normal circuitry 410 communicates via input and output lines 422 with the megacell circuitry 420. For example, the megacell circuitry 420 may comprise a standard arithmetic logic unit, microprocessor, or other circuitry which has a standard design and can be implemented as an independent module within the ASIC 400.

The normal circuitry 410 receives inputs from external pins such as pins 423, 425, via lines 433, 435. Of course, it will be understood that typically the normal circuitry 410 will receive on the order of dozens, or even hundreds of inputs but for purposes of clarity in illustrating the present invention, only the input terminals 423, 425 are shown to connect to the normal circuitry 410. In addition to outputting signals to the megacell circuitry 420 via the lines 422, the normal circuitry 410 may also output certain signals to the megacell circuitry 420 via a line 437 which connects to a first input of a 2-to-1 multiplexer 440. The multiplexer 440 further receives an input signal from an external pin 445 via a second input 447. The output of the multiplexer 440 is provided to an input of the megacell 420 via a line 449 as shown in Figure 4.

The multiplexer 440 receives a select input from a decoder 450 via a line 452. The megacell circuitry 420 further receives test inputs from an AND-gate 455 and an OR-gate 457. Of course, it should be understood, that the megacell circuitry 420 will typically include several test inputs, but the AND-gate 455 and the OR-gate 457 are shown to provide two exemplary test inputs to the megacell circuitry 420. The AND-gate 455 receives a first input via the line 452 and a second input via the line 433 from the input pin 423. Furthermore, the OR-gate 457 receives a first inverting input via the line 452 and a second input via the line 435 from the input pin 425. Although not shown in Figure 4, pin input and output buffers are assumed to be present but are not shown for ease of illustration.

The normal circuitry 410 connects to an input of a JTAG output multiplexer 460 via a line 462. Again, it should be understood, that the normal circuitry 410 will typically include on the order of tens or hundreds of outputs, however, for clarity of illustration, only the output 462 is depicted in Figure 4. The output of a 2-to-1 multiplexer 460 is provided to an external pin via a line 464. A select input of the 2-to-1 multiplexer 460 is provided by decoder 450 via a line 466. According to conventional circuitry, the second input of the 2-to-1 multiplexer 460 would connect directly to a latch boundary scan data register so that the JTAG standard input value would force the output terminal 465 to be equal to the JTAG bit when the appropriate select signal was provided to the input of the 2-to-1 multiplexer 460. However, in accordance with the present invention, the second input of the

5 outputs of the AND-gate 455 and the OR-gate 457 are set to low and high, respectively, so as to prevent the test inputs to the megacell circuitry 420 from changing during normal operation. When the standard test vector inputs applied at the input terminals 423, 425 are propagated through to the test inputs of the megacell circuitry 420, the megacell circuitry 420 outputs signals in response to the test vector inputs over multiple output lines. In the example of Figure 4, only the output line 474 is shown for ease of illustration; however, it will be understood that a plurality of output lines will be provided to a plurality of 2-to-1 multiplexers (such as the multiplexer 470) in order to fully test the functional characteristics of the megacell circuitry 420.

10 The signal output by the megacell circuitry 420 in response to the test vector inputs is provided as the first input to the multiplexer 470 over the line 474. The latched instruction register 484, when in the megacell test mode, further contains instruction bits which cause the decoder 450 to assert the select signal on the line 478 to select the megacell test output on the line 474. Thus, the output of the megacell circuitry 420 in response to the test vector inputs is provided on the line 472 at the output of the multiplexer 470. The decoder 450 further provides a signal on the line 464, in response to the instructions within the register 484, to select the input line 472 so that the megacell circuitry test output is provided on the line 464 to the output pin 465. If the megacell circuitry 15 420 is functioning correctly, then the test vector inputs will cause the appropriate pattern of test vector outputs to appear on the output pins for which a path is provided from the megacell circuitry 420. Thus, the output pin 465 will be indicative of the functionality of the megacell circuitry 420 when the test vector inputs are applied to the input pins 423, 425. In this manner, the functionality of the megacell circuitry 420 may be tested without the provision of additional output pins on the ASIC 400.

20 When the functionality of the megacell circuitry 420 is not being tested, the instruction register 484 is loaded with the appropriate instruction bits to cause the decoder 450 to select either the normal operation mode or the JTAG test mode. When the JTAG test mode is selected, this causes the decoder 450 to output a select signal over the lines 478 to propagate the input over the line 476 from the latch data register 480 to the output 472 of the multiplexer 470. Furthermore, the decoder 450 outputs a select signal over the line 466 which causes the input on the line 472 (which represents the value of a data bit within the latch data register 480 via the line 25 476) to be propagated on the output 464 of the multiplexer 460 so that the JTAG boundary scan data bit is provided on the output pin 465 if the output path has integrity.

30 If, on the other hand, the ASIC 400 is to operate in the normal manner, the JTAG TAP state controller 486 causes the decoder 450 to select the first input 462 of the multiplexer 460 so that the signal on the line 462 is output to the pin 465 via the multiplexer 460 and the line 464. Further, the decoder 450 outputs a low signal on the line 452 so that the test inputs to the megacell circuitry 420 are held to defined values so that the operation of the megacell circuitry 420 is not affected by the inputs on the pins 423, 425.

35 Although the preferred embodiments of the present invention have been described in detail above, it will be understood to those of ordinary skill in the art that obvious modifications could be made to the invention without departing from its spirit or essential characteristics. Thus, the foregoing description should be considered as

WHAT IS CLAIMED IS:

1. A system which provides for a reduced number of external pins on an integrated circuit (IC) package having JTAG test capability, said system comprising:

custom designed digital logic circuitry formed within said IC package, said custom designed digital logic circuitry having inputs and outputs;

a standardized megacell module having independent functionality formed within said IC package and incorporated into said IC package so as to communicate and function in unison with said custom designed digital logic circuitry, said megacell module having test inputs and test outputs which are used to test functionality of said megacell module;

a JTAG boundary scan data register which stores a test vector used to test integrity of inputs and outputs of said IC package, said boundary scan data register having outputs;

first selection circuitry having first inputs connected to at least one of said outputs of said boundary scan data register and at least one of said test outputs of said megacell module, said first selection circuitry further receiving a first selection input and providing one of said first inputs as an output based upon said first selection input;

second selection circuitry having second inputs connected to said output of said first selection circuitry and to at least one of said outputs of said custom designed digital logic circuitry, said second selection circuitry further receiving a second selection input and providing one of said second inputs as an output based upon said second selection input;

a JTAG instruction register which stores instruction bits, and wherein said instruction bits and the JTAG tap state, are used to determine said first selection input to said first selection circuitry and said second selection input to said second selection circuitry; and

a plurality of external pins connected as outputs of said second selection circuitry so that said test outputs of said megacell module are provided on said external pins when said instruction register and tap state are set to cause said first and second selection circuitry to propagate said megacell module test outputs to said external pins.

2. A system as defined in Claim 1, further comprising a switching circuit including first and second inputs and an output, said switching circuit selecting between an input pin connected with said first input of said switching circuit or said custom designed digital logic circuitry connected with said second input of said switching circuit, said output of said switching circuit being connected to said standardized megacell module.

3. A system as defined in Claim 2, wherein said switching circuit comprises a multiplexer.

4. A system as defined in Claim 1, further comprising an AND gate which has an output connected to test inputs of said standardized megacell module, said test inputs of said megacell module being held either high or low during normal testing of said megacell module, so that said test inputs can be controlled by a single input pin during JTAG testing.

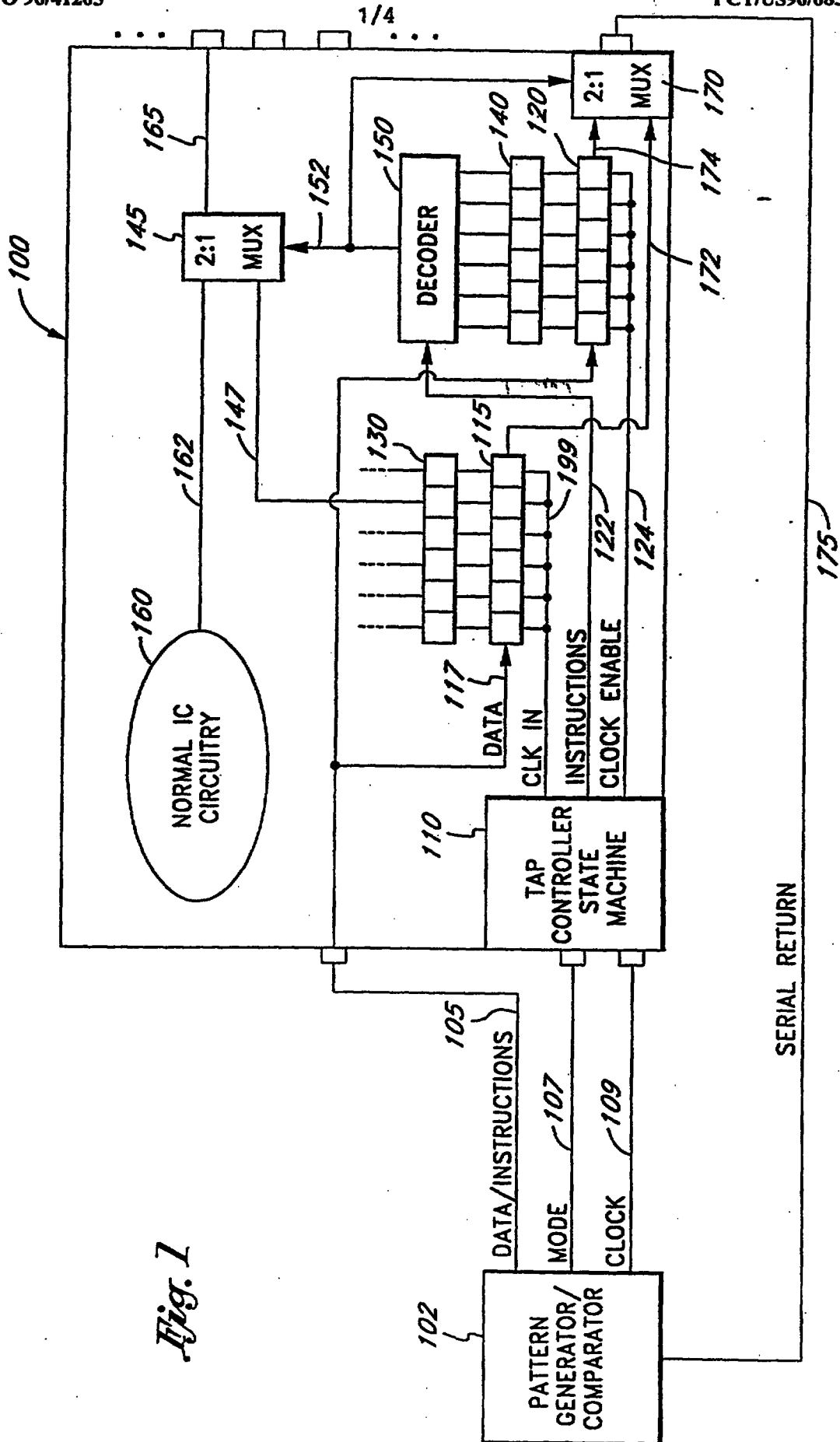


Fig. 1

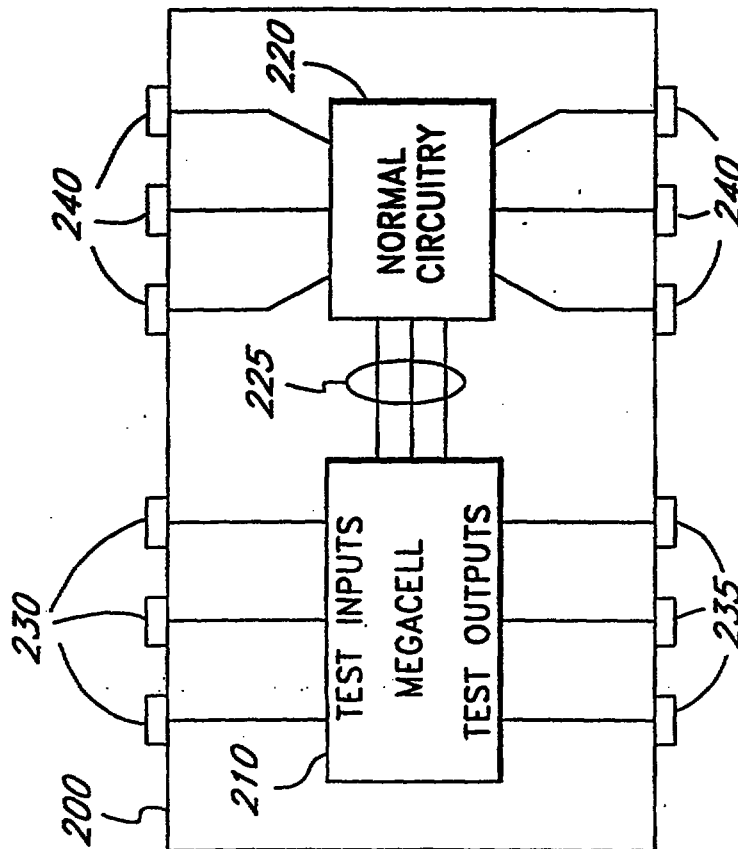


Fig. 2

3/4

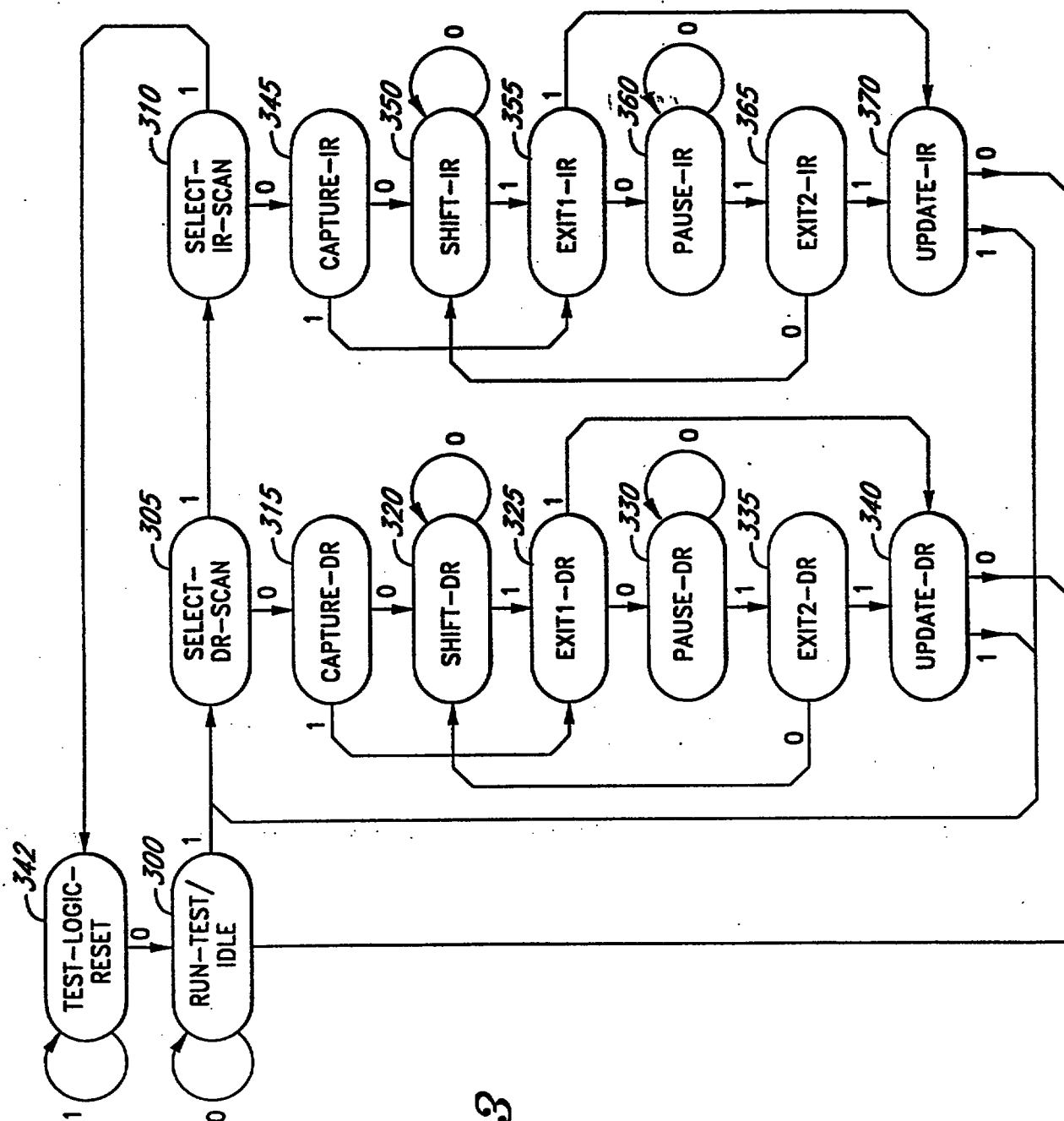
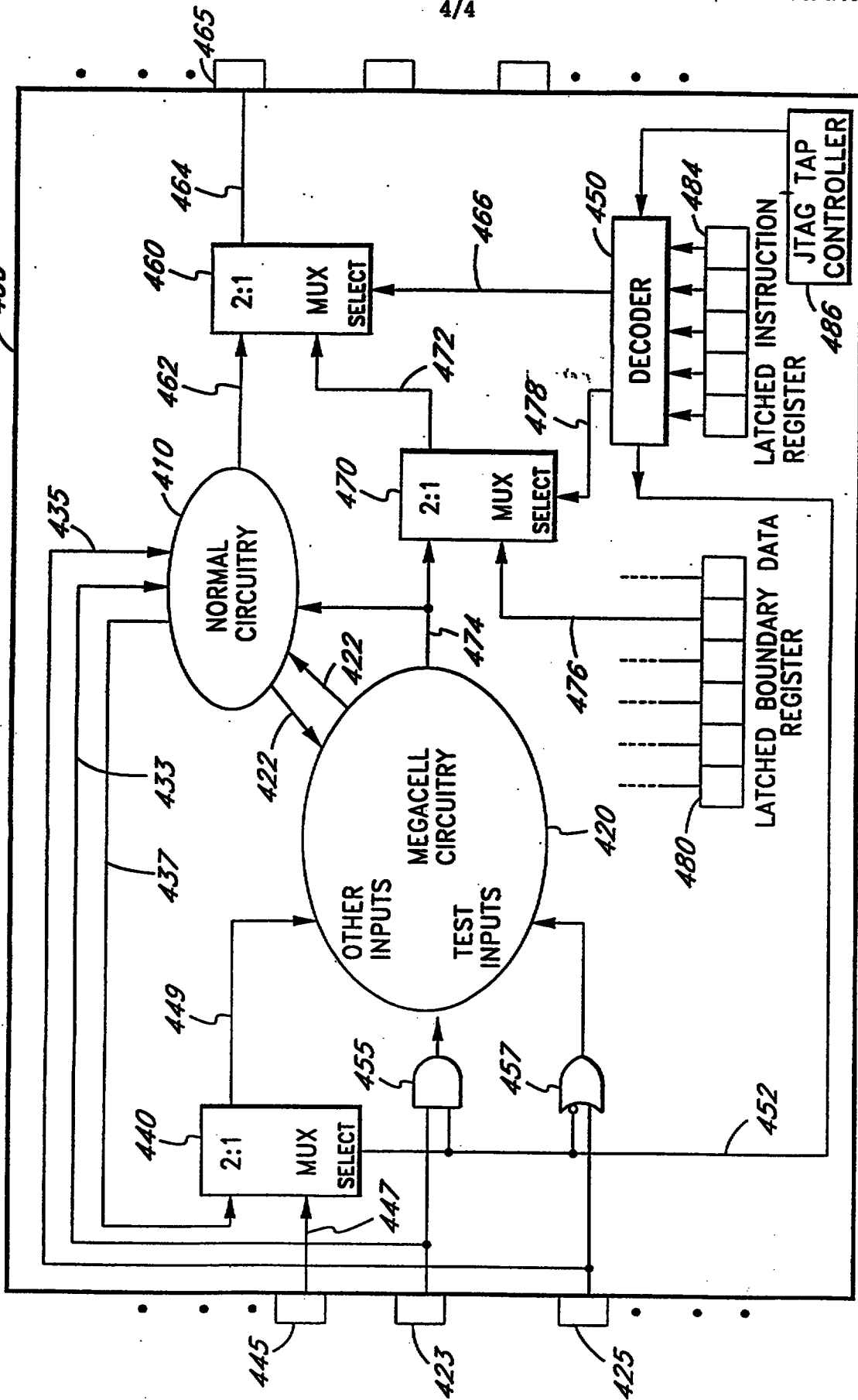


Fig. 3

Fig. 4





9706157-9
IP05 copy.

1. A system which permits an embedded megacell within an integrated circuit to be tested using test vectors applied to input/output pins of the integrated circuit without requiring dedicated input/output pins for the test vectors, said system comprising:

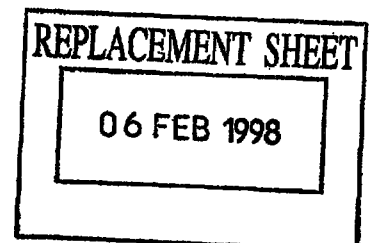
custom designed digital logic circuitry formed within said integrated circuit, said custom designed digital logic circuitry having inputs and outputs which are connected to input/output pins of said integrated circuit when said integrated circuit is operating in an normal operational mode;

a standardized megacell module having independent functionality formed within said integrated circuit and incorporated into said integrated circuit so as to communicate and function in unison with said custom designed digital logic circuitry, said megacell module having test inputs and test outputs which are used to test functionality of said megacell module, said test inputs and test outputs having no connections to input/output pins of said integrated circuit when said integrated circuit is operating in said normal operational mode;

a JTAG boundary scan data register which stores a test vector used to test integrity of inputs and outputs of said integrated circuit, said boundary scan data register having outputs;

selection circuitry having first inputs which receive said outputs from said custom designed logic circuitry, second inputs which receive said outputs from said boundary scan data register and third inputs which receive said outputs from said megacell module, said selection circuitry having outputs, said selection circuitry having selection inputs which control which of said first inputs, said second inputs and said third inputs are routed to said outputs of said selection circuitry;

a JTAG instruction register which stores instruction bits, selected ones of said instruction bits provided to said selection inputs of said selection circuitry to control which of said first inputs, said second inputs





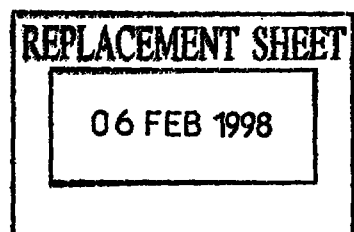
31 and said third inputs of said selection circuitry are routed to said outputs
32 of said selection circuitry, said instruction bits controlled in said normal
33 operational mode to select said first inputs to route the outputs of said
34 custom designed logic circuitry to said output of said selection circuitry,
35 said instruction bits controlled in a JTAG boundary scan test operational
36 mode to select said second inputs to route said outputs from said
37 boundary scan data register to said outputs of said selection circuitry, and
38 said instruction bits controlled in a megacell test mode to select said third
39 inputs to route said outputs of said megacell to said outputs of said
40 selection circuitry; and

41 a plurality of external pins connected to said outputs of said
42 selection circuitry, said outputs from said custom designed logic circuitry
43 being propagated to said external pins when said integrated circuit is
44 operating in said normal operational mode, said test outputs of said
45 megacell module being propagated to said external pins when said
46 selected ones of said instruction register bits are controlled to cause said
47 integrated circuit to operate in said megacell test mode of operation.

1 2. A system as defined in Claim 1, further comprising a switching
2 circuit including first and second inputs and an output, said switching circuit
3 selecting between an input pin connected with said first input of said switching
4 circuit or said custom designed digital logic circuitry connected with said second
5 input of said switching circuit, said output of said switching circuit being
6 connected to said standardized megacell module.

1 3. A system as defined in Claim 2, wherein said switching circuit
2 comprises a multiplexer.

1 4. A system as defined in Claim 1, further comprising an AND gate
2 which has an output connected to test inputs of said standardized megacell
3 module, said test inputs of said megacell module being held either high or low





4 during normal testing of said megacell module, so that said test inputs can be
5 controlled by a single input pin during JTAG testing.

1 5. A system as defined in Claim 1, further comprising an OR gate
2 which has an output connected to test inputs of said standardized megacell
3 module, said test inputs of said megacell module being held either high or low
4 during normal testing of said megacell module, so that said test inputs can be
5 controlled by a single input pin during JTAG testing.

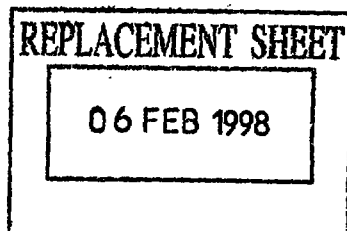
1 6. A method of testing a megacell within an integrated circuit having
2 said megacell as an embedded component of circuitry within said integrated
3 circuit, said megacell having at least one test output signal having no connection
4 external to said integrated circuit during normal operation of said integrated
5 circuit, said integrated circuit including logic which communicates signals to and
6 receives signals from said megacell during said normal operation of said
7 integrated circuit, said integrated circuit having a plurality of signals which are
8 provided as inputs to and outputs from said logic via respective pins of said
9 integrated circuit during said normal operation of said integrated circuit, said
10 method comprising:

11 applying a serial instruction to said integrated circuit via a JTAG
12 input pin to place said integrated circuit into a predetermined megacell
13 test mode such that said integrated circuit is no longer operating in said
14 normal mode of operation;

15 selectively disabling at least one of said plurality of output signals
16 from said logic to a respective first pin of said integrated circuit;

17 selectively routing said test output signal from said megacell to
18 said respective first pin of said integrated circuit;

19 applying a test input signal to said megacell via a second pin of
20 said integrated circuit to stimulate said megacell to perform a test
21 operation; and





22 monitoring said test output signal from said megacell at said
23 respective first pin of said integrated circuit.

1 7. A system for testing a megacell within an integrated circuit having
2 said megacell as an embedded component of circuitry within said integrated
3 circuit, said megacell having test inputs which are not connected to external pins
4 of said integrated circuit during a normal mode of operation of said integrated
5 circuit, said integrated circuit further including interface logic, said integrated
6 circuit having a plurality of signals which are provided as normal input signals
7 to and normal output signals from said interface logic on respective external pins
8 of said integrated circuit during said normal operation of said integrated circuit,
9 said system comprising:

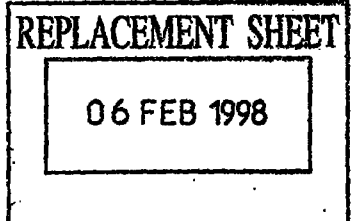
10 a JTAG input pin, wherein a serial instruction is applied to said
11 JTAG input pin which places said integrated circuit into a predetermined
12 megacell test mode;

13 a first pin of said integrated circuit which receives one of said
14 output signals from said interface logic when said integrated circuit is
15 operating in said normal mode of operation;

16 a selectable electrical path from said first pin to said megacell,
17 wherein a test input signal applied to said first pin when said integrated
18 circuit is in said megacell test mode is communicated to said megacell
19 via said selectable electrical path to thereby stimulate said megacell to
20 perform a test operation and to generate a test output signal, said
21 selectable electrical path blocked when said integrated circuit is operating
22 in said normal mode of operation;

23 a second pin of said integrated circuit; and

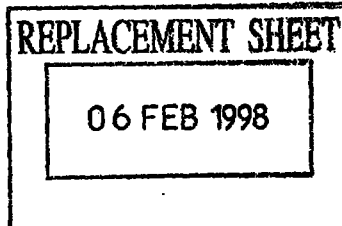
24 a selection circuit which receives said test output signal from said
25 megacell and which receives one of said plurality of output signals from
26 said interface logic, said selection circuit providing a selected output
27 signal to said second pin of said integrated circuit, said selected output





28 signal being said test output signal when said integrated circuit is in said
29 test mode of operation upon application of said serial instruction on said
30 JTAG input pin, said selected output signal being said one of said
31 output signals from said interface logic when said integrated circuit is in
32 said normal mode of operation.

JTS-8836
19980203/1





INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(51) International Patent Classification ⁶:

G01R 31/28

A1

(11) International Publication Number:

WO 96/41205

(43) International Publication Date: 19 December 1996 (19.12.96)

(21) International Application Number: PCT/US96/08576

(22) International Filing Date: 6 June 1996 (06.06.96)

(30) Priority Data:

08/480,483

7 June 1995 (07.06.95)

US

08/528,397

14 September 1995 (14.09.95)

US

(71) Applicant: AST RESEARCH, INC. [US/US]; 16215 Alton Parkway, Irvine, CA 92718 (US).

(72) Inventor: MOTE, Randall, L., Jr.; 26152 Red Corral Road, Laguna Hills, CA 92653 (US).

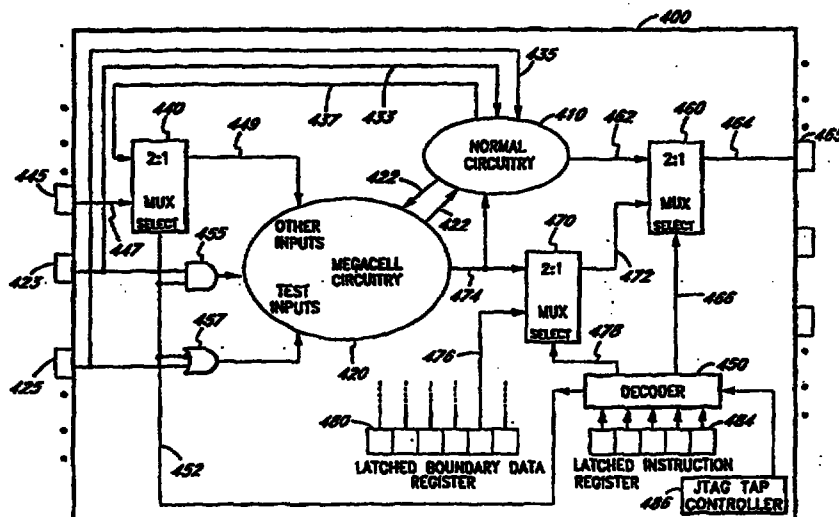
(74) Agent: ALTMAN, Daniel, E.; Knobbe, Martens, Olson and Bear, 16th floor, 620 Newport Center Drive, Newport Beach, CA 92660 (US).

(81) Designated States: AU, CN, JP, KP, KR, LK, MN, NZ, SG, VN.

Published

With international search report.

(54) Title: METHOD AND APPARATUS FOR TESTING A MEGACELL IN AN ASIC USING JTAG



(57) Abstract

Specially modified JTAG test circuitry is used to provide test inputs and outputs for vendor supplied megacells (420) with buried I/Os within an integrated circuit chip. A multiplexer (460) or similar circuit is used to alternatively select between a JTAG boundary scan output or a megacell (420) circuit test output in response to JTAG instructions within an instruction register. Additionally, a multiplexer (440) or similar circuit is used to alternatively select between an input pin or normal circuitry for input to a megacell's buried input. Furthermore, an AND (455) or OR (457) gate is used to allow test inputs to a megacell, which are normally tied either high or low, to be controlled by an input pin when in the special JTAG test mode. In this manner, test vectors applied at test inputs to the megacell circuitry result in test outputs to the megacell circuitry being provided on output pins of the integrated circuit without requiring additional input and/or output pins that are solely operational as test inputs or outputs to the megacell circuitry.