Description

The present invention relates to a semicustom semiconductor IC (integrated circuit) device and, in particular, to a semiconductor IC device having signal lines for supplying a signal, such as a clock signal, to any places of an associated circuit.

Fig. 1 is a plan view showing a pattern of a conventional standard cell-or gate array-type semiconductor IC device. In Fig. 1, reference numeral 50 shows an IC chip body including a plurality of cell rows 51 each constituted by a plurality of standard cells and macroblock 52, such as a memory. A plurality of I/O cells 53 are provided around chip body 50. Of these IO cells, cell 53A is of a clock driver type which has a greater drive capability and receives a clock signal. The clock signal is amplified at cell 53A and supplied via signal lines 54 to an associated cell in respective cell row 51.

Fig. 2 is an equivalent circuit showing a relation of a signal connection between the clock driver cell and the standard cells in the respective cell row. In Fig. 2, reference numerals 55 show standard cells, such as flip-flops (F/F), which are arranged in the respective cell rows and need an associated clock signal.

In the aforementioned semicustom integrated circuit, the connection layout of signal lines 54 for supplying a clock signal is implemented by randomly finding unconnected areas by virtue of a layout CAD, resulting in the connection line being excessively longer. For this reason, the associated signal lines have a resistance too great to be disregarded and a signal is supplied to the respective cell with a different delay time.

With an increase in the scale of an integrated circuit involved, an output waveform from the clock driver cell is distorted, sometimes prominently, depending upon the distance from the clock driver cell to the respective associated cell. If that signal is a clock signal, the integrated circuit involves a problem, such as a clock skew, thus failing to perform a normal operation. This problem cannot be resolved with the use of a clock driver cell of a greater driving capability, because it is caused by the resistance of the signal line per se. That is to say, in the conventional device, the connection length of the signal line becomes excessively longer and the signal is supplied to the associated cells with a different delay time and hence with a different phase. Furthermore, the signal waveform becomes distorted prominently at the far end cell or cells.

The Japanese patent JP-A-61-2342 describes a semiconductor integrated circuit device including rows of unit blocks. In a clock generating circuit, the wirings conduct a higher current and are therefore made wider than ordinary wirings. The larger wirings are formed perpendicular to the rows of unit blocks and are connected to wirings to supply electric power to the same.

It is accordingly the object of the present invention to provide a semiconductor integrated circuit device which can attain the reduction of a signal line length and achieve a low resistance feature with the result that the deformation and phase shift of a signal waveform can be reduced.

According to the present invention, a semiconductor integrated circuit device is provided which comprises a plurality of cell rows each including a plurality of standard cells; signal connection cells provided one in each of the cell rows and located all on a straight line perpendicular to the cell rows; signal lines for cell rows connected to said signal connection cells to allow a signal which is propagated via the signal connection cells to be supplied to the cells in the respective cell rows; and row-to-row signal lines each connected between the signal connection cells and supplying the signal to said signal connection cells, said row-to-row signal lines having a width greater than that of said signal lines for cell rows.

In the semiconductor integrated circuit device of the present invention the signal connection cells are connected together by the cell-to-cell connection line whose connection width is broader than that of the ordinary connection line, resulting in a signal being propagated to the associated cell in a low-resistance fashion. Furthermore, the signal connection cells are arranged at the respective cell rows so as to be located on a single straight line and it is, therefore, possible to connect the respective signal connection cells together by the cell-to-cell connection line so that a distance of the signal connection line can be reduced. A signal coming from the signal connection cell is supplied in a row unit to the associated cell in the respective cell row via the line for cell rows, so that a signal is propagated over a minimum connection line length.

According to the present invention, as set out above, a semiconductor integrated circuit device is provided which can reduce a signal connection line length and achieve a low-resistance feature so that the phase shift of a signal waveform, as well as the deformation of the signal waveform at an output of the cell to which it is supplied from a clock driver cell, occurs.

This invention can be more fully understood from the following detailed description when taken in conjunction with the accompanying drawings, in which:

Fig. 1 is a plan view showing a pattern of a conventional semicustom semiconductor integrated circuit device;

Fig. 2 is an equivalent circuit showing a relation between a clock driver cell and standard cells in

respective cell rows in the conventional semi-custom semiconductor integrated circuit of Fig. 1;

Fig. 3 is a plan view showing a pattern of an IC chip as obtained by incorporating a semiconductor integrated circuit device into an associated integrated circuit of a standard cell type;

Fig. 4 is a plan view showing a detailed pattern of a signal connection cell in Fig. 3;

Fig. 5 is a view showing a signal connection line between a clock driver cell and standard cells in the respective cell row in the semiconductor integrated circuit device of Fig. 3;

Fig. 6 is a plan view showing an IC chip pattern of a semiconductor integrated circuit device, according to another embodiment of the present invention, which is applied to a standard cell type integrated circuit;

Fig. 7 is a plan view showing a pattern of a signal connection cell in a semiconductor integrated circuit device, according to another embodiment of the present invention, which is applied to a standard cell type integrated circuit;

Fig. 8 is a plan view showing an IC chip pattern including a signal connection cell in Fig. 7;

Fig. 9 is a plan view showing an IC chip pattern of a semiconductor integrated circuit, according to another embodiment of the present invention, which includes signal connection cells shown in Fig. 7; and

Fig. 10 is a plan view showing a configuration pattern of a signal connection cell in a semiconductor integrated circuit device, according to another embodiment of the present invention, which is applied to a standard cell type integrated circuit.

The embodiment of the present invention will be explained below with reference to the accompanying drawings.

Fig. 3 is a plan view showing an IC chip pattern obtained by incorporating an invention into a standard cell type integrated circuit.

In Fig. 3, IC chip body 10 includes a plurality of cell rows 11 each having a plurality of cells and macro block 12, such as a memory. In respective cell rows 11, signal connection cells 13 are each so provided as to be located on a single line across the cell row array. These signal connection cells 13 are mutually connected by cell-to-cell connection line 14 whose width is broader than that of those ordinary lines in the respective cell rows.

A plurality of I/O cells 15 are provided around chip body 10 and, of I/O cells, I/O cell 15A is a clock driver cell of a greater driving capability which receives a clock signal. The clock signal is amplified by clock driver cell 15A and coupled via a corresponding signal line to signal connection cell 13 at a location nearest to cell 15A.

Connection line 16 for cell rows which has a width equal to that of the ordinary connection line is connected to signal connection cell 13. Through cell row connection line 16 the clock signal is supplied to a clock signal demand standard cell, such as a standard flip-flop cell.

Fig. 4 is a plan view showing a detailed pattern of signal connection cell 13 in the aforementioned integrated circuit. Signal connection cell 13 has a metal connection layer, such as aluminum as well as input-side connection line 17 equal in width to connection line 14 and output-side connection line 18 connected to input-side connection line 17 and having a width equal to that of the ordinary connection line. Input side connection line 17 is connection to cell-to-cell connection line 14 and output side connection line 18 is connected to cell row connection line 16, not shown in Fig. 4.

Fig. 5 is an equivalent circuit showing a relation of signal connection lines between the clock driver cell and standard cells in the respective cell row. In Fig. 5, connection line 21 indicated by a broad line comprises input-side connection line 17 and cell-to-cell connection line 14 both having a corresponding connection line in signal connection cell 13. As will be evident from Fig. 5, a clock signal is propagated from clock driver cell 15A via connection line 21 to the cell row position. Connection line 21 has a greater width and extends on a straight line as shown in Fig. 3 so as to obtain a minimum connection line. It is thus possible to obtain an adequately small resistive value. As a result, the delay times for a signal to reach the respective cell rows become adequately small and equal to each other. A clock signal is supplied from respective connection cell 13 to a clock signal demand standard cell, such as a flip-flop (F/F) cell, in the respective row via connection line 16 for the corresponding cell row. It is thus possible to provide a minimum connection line length for connection line 16 with the ordinary connection line of the aforementioned width, and to solve, for example, a "clock skew" problem.

According to the aforementioned embodiment, it is possible to reduce the length of a signal connection line, as well as to achieve a low resistance feature, when a clock signal is propagated. This arrangement can suppress the generation of the phase displacement of a clock signal and reduce the deterioration of an output waveform when being propagated from the clock drive cell to the respective cell.

Fig. 6 is a plan view showing an IC chip pattern when the semiconductor IC device of the present invention is applied to a standard cell type integrated circuit. In this embodiment, connection line 16 for cell rows is shared between two respective adjacent cell rows, thus allowing the reduction

of the length of a connection line for propagating a clock signal so that the clock signal can drive the corresponding cell without loosing an enhanced drive capability.

Fig. 7 is a plan view showing a cell configuration pattern for signal connection when a semiconductor device of the present invention is applied to a standard cell type integrated circuit. In this embodiment, cell 33 for signal connection includes input-side connection line 37 and output-side connection line 38 both made of a metal connection line, such as aluminum, and amplifier 39 connected between input-side connection line 37 and output-side connection line 38.

In the integral circuit having signal connection cells, a cell-to-cell connection line is of two type: connection line 34A and connection line 34B. Input-side connection line 37 in the signal connection cell is connected to cell-to-cell connection line 34A of a broader connection width than that of the ordinary connection line and to cell-to-cell connection line 34 whose width is equal to that of the ordinary connection line. Output-side connection line 38 in the signal connection cell is connected to connection line 16, not shown in Fig. 7, for cell rows.

Fig. 8 is a plan view showing an IC chip configuration pattern with signal connection cells shown in Fig. 7 incorporated therein. In the embodiment shown in Fig. 8, amplifier 39 is connected between input-side connection line 37 and output-side connection line 38 in respective signal connection cell 33 so that a clock signal is supplied to the respective cell row with an enhanced cell drive capability.

Fig. 9 is a plan view showing an IC chip configuration pattern in a semiconductor IC device, with the signal connection cells (Fig. 7) incorporated therein, according to another embodiment of the present invention. In the embodiment, connection line 16 for cell rows is provided for every two adjacent cells as in the embodiment shown in Fig. 6. According to the present invention, it is possible to reduce the length of a connection line for propagating a clock signal and hence to provide an enhanced cell drive capability with which a clock signal is propagated to the associated cell.

Fig. 10 is a plan view showing a connection cell configuration pattern for signal connection in a semiconductor IC device, with a standard cell type integrated circuit incorporated therein, according to another embodiment of the present invention. In the embodiment shown in Fig. 10, signal connection cells 33 include input-side connection line 37, output-side connection line 38 and amplifier 39 as in Fig. 7. The cell-to-cell connection line is constituted by one type of connection line 34A whose width is greater than that of the ordinary connection line. Only input-side connection line 37 in the signal connection cell is connected to each other via cell-to-cell connection line 34A. This type of the integrated circuit is advantageous in the case where the number of clock signal demand cells in the respective cell row is averaged.

The present invention is not restricted to the aforementioned embodiment and can be changed in a variety of ways without being restricted to the aforementioned embodiments. Although, in the aforementioned respective embodiments, a clock signal has been explained as being supplied or propagated via the signal connection cell, the present invention can also been reduced to practice if an ordinary signal is used in place of the clock signal.

Claims

1. A semiconductor integrated circuit device comprising a plurality of cell rows (11) each including a plurality of standard cells;

   signal connection cells (13) provided one in each of the cell rows and located all on a straight line perpendicular to the cell rows;

   signal lines (16) for cell rows connected to said signal connection cells (13) to allow a signal which is propagated via the signal connection cells (13) to be supplied to the cells in the respective cell rows; and

   row-to-row signal lines (14,34A) each connected between the signal connection cells (13) and supplying the signal to said signal connection cells, said row-to-row signal lines (14,34A) having a width greater than that of said signal lines (16) for cell rows.

2. The semiconductor integrated circuit device according to claim 1, characterized in that said signal connection cell (13,33) has signal lines (17,18; 37,38) for propagating a signal.

3. The semiconductor integrated circuit device according to claim 2, characterized in that said signal lines (17,18; 37,38) include an input-side line (17,37) connected to said row-to-row signal line (14,34A) and having a signal line whose width is equal to that of said row-to-row signal line (14,34A) and an output-side signal line (18,38) connected to said input-side signal line (17,37).

4. The semiconductor integrated circuit device according to claim 3, characterized by further including an amplifier (39) whose input terminal is connected to said input-side signal line (17,37) and whose output terminal is connected to said output-side signal line (18,38).

of the length of a connection line for propagating a clock signal so that the clock signal can drive the corresponding cell without loosing an enhanced drive capability.

Fig. 7 is a plan view showing a cell configuration pattern for signal connection when a semiconductor device of the present invention is applied to a standard cell type integrated circuit. In this embodiment, cell 33 for signal connection includes input-side connection line 37 and output-side connection line 38 both made of a metal connection line, such as aluminum, and amplifier 39 connected between input-side connection line 37 and output-side connection line 38.

In the integral circuit having signal connection cells, a cell-to-cell connection line is of two type: connection line 34A and connection line 34B. Input-side connection line 37 in the signal connection cell is connected to cell-to-cell connection line 34A of a broader connection width than that of the ordinary connection line and to cell-to-cell connection line 34 whose width is equal to that of the ordinary connection line. Output-side connection line 38 in the signal connection cell is connected to connection line 16, not shown in Fig. 7, for cell rows.

Fig. 8 is a plan view showing an IC chip configuration pattern with signal connection cells shown in Fig. 7 incorporated therein. In the embodiment shown in Fig. 8, amplifier 39 is connected between input-side connection line 37 and output-side connection line 38 in respective signal connection cell 33 so that a clock signal is supplied to the respective cell row with an enhanced cell drive capability.

Fig. 9 is a plan view showing an IC chip configuration pattern in a semiconductor IC device, with the signal connection cells (Fig. 7) incorporated therein, according to another embodiment of the present invention. In the embodiment, connection line 16 for cell rows is provided for every two adjacent cells as in the embodiment shown in Fig. 6. According to the present invention, it is possible to reduce the length of a connection line for propagating a clock signal and hence to provide an enhanced cell drive capability with which a clock signal is propagated to the associated cell.

Fig. 10 is a plan view showing a connection cell configuration pattern for signal connection in a semiconductor IC device, with a standard cell type integrated circuit incorporated therein, according to another embodiment of the present invention. In the embodiment shown in Fig. 10, signal connection cells 33 include input-side connection line 37, output-side connection line 38 and amplifier 39 as in Fig. 7. The cell-to-cell connection line is constituted by one type of connection line 34A whose width is greater than that of the ordinary connection line. Only input-side connection line 37 in the signal connection cell is connected to each other via cell-to-cell connection line 34A. This type of the integrated circuit is advantageous in the case where the number of clock signal demand cells in the respective cell row is averaged.

The present invention is not restricted to the aforementioned embodiment and can be changed in a variety of ways without being restricted to the aforementioned embodiments. Although, in the aforementioned respective embodiments, a clock signal has been explained as being supplied or propagated via the signal connection cell, the present invention can also been reduced to practice if an ordinary signal is used in place of the clock signal.

Claims

1. A semiconductor integrated circuit device comprising a plurality of cell rows (11) each including a plurality of standard cells;

   signal connection cells (13) provided one in each of the cell rows and located all on a straight line perpendicular to the cell rows;

   signal lines (16) for cell rows connected to said signal connection cells (13) to allow a signal which is propagated via the signal connection cells (13) to be supplied to the cells in the respective cell rows; and

   row-to-row signal lines (14,34A) each connected between the signal connection cells (13) and supplying the signal to said signal connection cells, said row-to-row signal lines (14,34A) having a width greater than that of said signal lines (16) for cell rows.

2. The semiconductor integrated circuit device according to claim 1, characterized in that said signal connection cell (13,33) has signal lines (17,18; 37,38) for propagating a signal.

3. The semiconductor integrated circuit device according to claim 2, characterized in that said signal lines (17,18; 37,38) include an input-side line (17,37) connected to said row-to-row signal line (14,34A) and having a signal line whose width is equal to that of said row-to-row signal line (14,34A) and an output-side signal line (18,38) connected to said input-side signal line (17,37).

4. The semiconductor integrated circuit device according to claim 3, characterized by further including an amplifier (39) whose input terminal is connected to said input-side signal line (17,37) and whose output terminal is connected to said output-side signal line (18,38).

5. The semiconductor integrated circuit device according to claim 1, characterized in that each of said signal lines (16) for cell rows is provided between adjacent cell rows (11) to propagate signals to cells of the adjacent cell rows.

Patentansprüche

1. Integrierte Halbleiterschaltungs-Vorrichtung mit mehreren Zellenreihen (11), die jeweils mehrere Standardzellen aufweisen;
Signalverbindungszellen (13), von denen eine in jeder der Zellenreihen vorgesehen ist, und die sämtlich auf einer geraden Linie senkrecht zu den Zellenreihen liegen;
Signalleitungen (16) für Zellenreihen, die an die Signalverbindungszellen (13) angeschlossen sind, um die Zufuhr eines Signals, das sich über die Signalverbindungszellen (13) ausbreitet, an die Zellen in den jeweiligen Zellenreihen zu gestatten; und
Reihen-Reihen-Signalleitungen (14, 34A), die jeweils zwischen die Signalverbindungszellen (13) geschaltet sind und das Signal an die Signalverbindungszellen übertragen, wobei die Reihen-Reihen-Signalleitungen (14, 34A) eine Breite aufweisen, die größer ist als die der Signalleitungen (16) für Zellenreihen.

2. Integrierte Halbleiterschaltungs-Vorrichtung nach Anspruch 1, dadurch gekennzeichnet, daß die Signalverbindungszelle (13, 33) Signalleitungen (17, 18; 37, 38) zur Ausbreitung eines Signals aufweist.

3. Integrierte Halbleiterschaltungs-Vorrichtung nach Anspruch 2, dadurch gekennzeichnet, daß die Signalleitungen (17, 18; 37, 38) eine eingangsseitige Leitung (17, 37) aufweisen, die an die Reihen-Reihen-Signalleitung (14, 34A) angeschlossen ist und eine Signalleitung aufweist, deren Breite gleich der der Reihen-Reihen-Signalleitung (14, 34A) ist, und eine an die eingangsseitige Signalleitung (17, 37) angeschlossene ausgangsseitige Signalleitung (18, 38).

4. Integrierte Halbleiterschaltungs-Vorrichtung nach Anspruch 3, dadurch gekennzeichnet, daß weiterhin ein Verstärker (39) vorgesehen ist, dessen Eingangsklemme an die eingangsseitige Signalleitung (17, 37) und dessen Ausgangsklemme an die ausgangsseitige Signalleitung (18, 38) angeschlossen ist.

5. Integrierte Halbleiterschaltungs-Vorrichtung nach Anspruch 1, dadurch gekennzeichnet, daß jede der Signalleitungen (16) für Zellenreihen zwischen benachbarten Zellenreihen (11) vorgesehen ist, um Signale an Zellen der benachbarten Zellenreihen zu übertragen.

Revendications

1. Dispositif de circuit intégré semi-conducteur comprenant une pluralité de rangées de cellules (11) comportant chacune une pluralité de cellules standards;
des cellules de liaison de signaux (13) prévues une dans chacune des rangées de cellules et situées toutes sur une ligne droite perpendiculairement aux rangées de cellules;
des lignes de signaux (16) pour des rangées de cellules reliées auxdites cellules de liaison de signaux (13) pour permettre au signal qui se propage par les cellules de liaison de signaux (13) d'être appliqué à des cellules dans les rangées de cellules respectives; et
des lignes de signaux de rangée à rangée (14, 34A) chacune étant relié à des cellules de liaison de signaux (13) et fournissant le signal auxdites cellules de liaison de signaux, lesdites lignes de signaux de rangée à rangée (14, 34A) ayant une largeur supérieure à celle desdites lignes de signaux (16) pour des rangées de cellules.

2. Dispositif de circuit intégré selon la revendication 1, caractérisé en ce que ladite cellule de liaison de signaux (13, 33) a des lignes de signaux (17,18; 37,38) pour propager un signal.

3. Dispositif de circuit intégré semi-conducteur selon la revendication 2, caractérisé en ce que lesdites lignes de signaux (17,18; 37,38) comportent une ligne du côté de l'entrée (17, 37) reliée à ladite ligne de signaux de rangée à rangée (14, 34A) et ayant une ligne de signaux dont la largeur est égale à celle de ladite ligne de signaux de rangée à rangée (14, 34A) et une ligne de signaux du côté de la sortie (18, 38) reliée à ladite ligne de signaux du côté de l'entrée (17, 37).

4. Dispositif de circuit intégré semi-conducteur selon la revendication 3, caractérisé en ce qu'il comporte de plus un amplificateur (39) dont la borne d'entrée est reliée à ladite ligne de signaux du côté de l'entrée (17, 37) et dont une borne de sortie est reliée à ladite ligne de signaux du côté de la sortie (18,38).

5. Dispositif de circuit intégré semi-conducteur selon la revendication 1, caractérisé en ce que chacune desdites lignes de signaux (16) pour

des rangées de cellules est placée entre des rangées de cellules (11) pour propager des signaux aux cellules des rangées de cellules adjacentes.