

Description

Field of the Invention

The invention is in the field of analog to digital encoders and more particularly relates to a telephony encoder with variable gain.

Background of the Invention

Telephone systems of the digital signal type require analog to digital and digital to analog converter circuits, usually referred to as CODECs for interfacing voice signals and the like between analog signals compatible with analog transducers and binary signals compatible with digital telephony switching and transmission function and apparatus. In order that the encoding function be performed such that pulse code modulated (PCM) words are generated which accurately represent an analog input signal, the analog signal must be centered about an encoder midpoint. That is, the encoder operating midpoint and the zero level of the analog signal should correspond. If not, quantization distortion, harmonic distortion and noise are included in the PCM words. It is typical practice to have predetermined the gain of an encoder during manufacture, and if desired, later when in use, alter the gain, in circuit, with the use of a preset gain pad. Biasing of the midpoint may be conveniently achieved by AC coupling an appropriate node within the encoder and charging the node via a switched capacitor resistance to null any offset at the encoder input. In effect, the sign bit of each PCM word is integrated onto the AC coupled node such that its long term voltage (d.c. value) is representative of the average of the sign bit polarities. Stability is achieved when the sign bit occurrences are evenly negative and positive.

If however the gain of the typical encoder is changed during its normal operation, a step component consequently appears at the input of the encoder because the integrated signal at the AC coupled node no longer cancels the total offset. Hence, the operational midpoint is shifted to no longer correspond to the zero level of the analog signal. In a linear encoder the effect of a gain change will be manifest as an annoying click. In a compression encoder, severe harmonic distortion may also result. Given time, the step voltage diminishes until the operational midpoint again corresponds to the zero level of the analog signal. However, during this time resulting harmonic distortions deteriorate the quality of compression encoded signal. In an application wherein the gain of the encoder is adjusted from time to time, or frequently, such performance is unacceptable. European patent application No. 0 005 999 and United States patent 4,590,458 each disclose analog-to-digital encoder systems which are gain variable over such wide ranges that at high gain settings off-set errors can signif-

icantly depreciate the accuracy of the digital output signals. Off-set errors are corrected by determining the error value present in a null or ground signal and adjusting either the input analog signal or the amplified analog signal accordingly to cancel the error. Neither of these documents is concerned with mid-operating point stabilizing of an amplifier, in response to sign bits as is typical in many analog-to-digital encoders used in telephony.

Summary of the Invention

It is an object of the invention to provide a variable gain encoder whereby analog to digital signal conversions may be modified during the course of a telephone call.

It is also an object of the invention to provide an encoder, the gain of which may be abruptly varied 'on the fly', that is to say during an active telephone call, without introducing significant noise and distortion.

In accordance with the invention, a variable gain analog to digital encoder includes, a first fixed gain encoding path, which provides a first stabilized mid-operating point analog signal to a second variable gain encoding path wherein, an analog amplifier inversely amplifies a variably tapped difference signal developed between the first analog signal and a signal for encoding at an output of the analog amplifier in the second path.

An apparatus in accordance with the invention for variably encoding an analog signal to produce pulse code modulated (PCM) signal samples therefrom, comprises a first means for generating encoded signal samples, and a second means for generating variable gain encoded signal samples. The first means includes a first amplifier means, having an analog signal input port, and being for producing a first stabilized mid-operating point analog signal in response to the analog signal and to first sign bits, said first sign bit emanating from an analog to digital converter for generating the first sign bits in response to the first stabilized analog signal. The second means includes a second amplifier means for producing a second stabilized mid-operating point analog signal in proportional inverse relationship with the first stabilized analog signal and in response to second sign bits. A resistance means is connected to have a difference of the first and second stabilized analog signals appear there across, and includes a variable tap means which is connected to an inverting input of the second amplifier. The analog to digital converter generates the PCM signal samples, including the second sign bits, in response to said second stabilized analog signal.

An alternate gain method for generating digital word representations of an analog signal in accordance with the invention includes, providing a first signal in response to the analog signal and first sign

bits corresponding thereto by stabilized mid-operating point amplifying the analog signal with a predetermined fixed gain. A second signal is provided in response to the first signal and second sign bits corresponding to the second signal by stabilized mid-operating point amplifying the first signal with a controllably varied gain. The second signal is digitally converted to provide plural bit words, each including one of said second sign bits, whereby said plural bit words are gain variable with respect to the first signal.

Brief Description of the Drawings

An example embodiment is discussed with reference to the accompanying drawing in which:

Figure 1 is a graphical illustration of a reconstructed signal having been affected by a momentary gain adjustment in a prior art encoder;

Figure 2 is a schematic block diagram of a prior art encoder having predetermined fixed gain;

Figure 3 is a schematic block diagram of a variable encoder circuit in accordance with the invention;

Figure 4 is a more detailed schematic block diagram of an example of the variable encoder circuit illustrated in figure 3; and

Figure 5 is an abbreviated schematic diagram of one example of a gain adjustment element used an encoder circuit as illustrated in figure 4.

Description of the Example Embodiment

The graphical illustration in figure 1 includes a voltage axis V at a left side of the figure and a time axis T extending at right angles to the voltage axis V. A reconstructed analog representation of an encoded audio signal as might be obtained from the encoder in figure 2 is depicted along the time axis T. A first 1 1/2 cycles on the left side of the figure represent an encoding function of a constant signal wherein the encoding function is of a first gain. The remaining cycles represent an encoding function of the constant signal after the encoding function was abruptly changed or adjusted in the encoder circuit to a second gain, greater than the first gain. If gain changes are extreme, as might be the case if handsfree voice switching were required, the time for the signal to settle as depicted on the right-hand side of the figure could be as much as a minute. Such performance would not be practical in a telephone system.

The typical encoder, illustrated in figure 2, is adapted as illustrated in figures 3 and 4, the structure and functions of which may be more readily understood by first considering the prior art. In figure 2, an analog audio signal is applied at an audio input 9 and capacitively coupled via a capacitor 12 to a node 18 of a Butterworth second order filter circuit shown in detail at 11. A low pass filter 14, often referred to as

an anti-aliasing filter, passes voice band frequencies to an input of an analog to digital converter circuit 13. In a typical telephony application, converter circuits are operated at a sampling rate of 8 KHz and the filter cut off characteristic is between 3 KHz and 4 KHz. The analog to digital converter circuit 13 generates plural bit words, usually 8 bit PCM words, at an 8 KHz rate in response to the analog signals from the low pass filter 14. A sign bit of each word defines the polarity of each word. The sign bit is also used to adjust the mid-operating point of the circuit 11 via the node 18, where, an integration of sign bit occurrences is coupled via a sign bit latch 16 and a switched capacitor functional resistance element at 17.

As thus far described, the prior art encoder circuit provides a fixed gain encoding function. The gain of this circuit may be altered, for example, by introducing resistance in a series with the inverting input of the amplifier 10. If the gain is altered during operation, for example during a telephone conversation, this will have the effect of disturbing the mid-operating point similar to that exemplified in figure 1. As before mentioned, frequent gain changes of this consequence would not be tolerable in a typical telephone system.

In figure 3, a fixed gain amplifier 10 is representative of all but the analog to digital converter 13 in figure 2. The analog to digital converter 13 in figure 3 is alternately connected to receive first and second analog signals from the fixed gain amplifier 10 and a variable gain amplifier 20, via a switch 45. An output of the converter circuit 13 is coupled by a switch 46 to provide digital outputs alternately on leads 15 and 25.

The converter 13 is operated in this example at a 16 KHz sampling rate, in synchronism with the switches 45 and 46. Signals from the output of the fixed gain amplifier 10 are inversely amplified in the variable gain amplifier 20 in accordance with a gain factor controlled via a control input 44. Both the amplifiers 10 and 20 are mid-operating point stabilized in response to sign bits coupled via respective paths 15a and 25a. Hence the sign bits on the path 15a are the inverse of the sign bits on the path 25a. In another example, not shown, the switches 45 and 46 are not used and only the output of the variable gain amplifier is converted to a digital signal. In this example, the path 15a is connected directly to the path 25a but differs therefrom in that it includes an inverter in series therewith for inverting the sign bits on the path 25a for use in stabilizing the amplifier 10.

In figure 4, the variable encoder circuit illustrated includes all the elements of the prior art figure 2 (which are correspondingly labeled) in addition to elements which provide an example of the variable gain amplifier 20 in figure 3. With exception of the capacitor 12 and a capacitor 22, all of the elements in figure 4, are preferably integrated in CMOS transistor technology within an integrated circuit. In this example, low pass filters 17 and 27 are implemented by switch-

ed capacitor resistances. An operational amplifier 21 includes a non-inverting input which is used as a stabilizing node for mid-point operating bias potential. The bias potential is generated by the capacitor 22 and the switched capacitor resistance 27 in response to sign bits from a latch 26 which captures and holds sign bits from the digital output 25, at an 8 KHz sampling rate. A resistance element 40 is connected via a lead 41 to the output of the low pass filter 14 and via a lead 42 to an output of the amplifier 21. An inverting input of the amplifier 21 is capacitively connected to its output via a capacitor (of about 5pf) 23 and is also connected to the resistance element 40 by a variable tap 43. The tap is alterable by a control input shown at 44.

The output mid-point of the amplifier 11 is directly coupled through the filter 14 such that a potential difference between the output of the amplifier 11 and the amplifier 21 appears across the resistance element 40. The variable tap 43, when adjusted, travels through a d.c. potential difference which counter balances the d.c. output of the amplifier 20 such that it remains at about the preferred mid-point even during those periods shorter than the time constant of the integrating function of the elements 22 and 27.

An example of the resistance element 40 is illustrated in more detail in figure 5. This example is particularly adapted to being integrated in the CMOS technology. Thirty-two columns labeled C0-C31 each include ten field effect transistors being arranged in a series string and terminating at a rail which corresponds to the variable tap 43. Thirty-two corresponding resistance segments, labelled R1-R32, are connected in series between the leads 41 and 42. The first column C0 is connected to a junction of the lead 41 and the resistance segment R1, and the second column C1 is connected to a junction between resistance segments R1 and R2 and so on as illustrated.

The control input 43 includes five leads labelled A-E, each of which is connected to gate electrodes, as exemplified at 55, of a pair of the field effect transistor (FET) in each of the columns and which are of opposite conductivity type. For convenience, this is illustrated by one of the pair having a gate electrode with an inversion symbol 55' attached.

For example, in column C0 a FET 52 is paired with a FET 53 which includes the inversion symbol. Both the FETs 52 and 53 include gate electrodes which are connected to the lead 43A but the FETs 52 and 53 respond oppositely to a control signal on the lead so that when one FET is OFF, the other is ON. For simplicity of illustration, the control leads are shown as running straight across each respective row. This is intended to indicate that the gate electrode of each of the FETs is connected to its respective control lead. It will be noticed that in each column, half of the FETs are each bridged by a conductive path, as exemplified at 54. The conductive paths or

bridges are organized in a prearranged pattern such that only one of the columns C0-C31 will be switched ON in the presence of any five bit binary word applied at control input 44. More particularly in this pattern, one of each FET pair is bridged while the other is not, such that the bridged FET is of no function. Therefore, each of the leads A-E is of effect with respect to only one FET in each row even though it is connected to its respective pair of FETs in each row. This particular structure was arrived at as a matter of convenience in fabricating the example embodiment in the MOS technology.

In this particular example of the encoder in figure 4, the resistance element is so arranged to provide a gain alteration of 1.7 decibel steps through a range of 52.7 decibels.

Claims

1. An analog to digital (A/D) encoder for providing digital words being representative of samples of an input analog signal, including:
 - an analog to digital converter circuit (13), having an input and an output, for generating said digital words each consisting of plural bits including a sign bit;
 - a first amplifier means (11) for generating a first analog signal with fixed gain in response to the input analog signal;
 - a first feedback means (16, 17) being for mid-operating point stabilizing the operation of the first amplifier means, in response to the sign bits;
 - the analog to digital encoder being characterized by:
 - a second amplifier means (21) for generating a second analog signal with variably controllable gain, in response to the first analog signal;
 - a second feedback means (26, 27) being for mid-operating point stabilizing the operation of the second amplifier means, in response to the sign bits corresponding to the variably controllable gain analog signal; and
 - a switch (45, 46) for alternately connecting the first and second analog signals to the input of the analog to digital converter circuit and for likewise alternately connecting the first and second feedback means to the output of the digital converter circuit;
 - whereby first and second digital words corresponding to fixed and variable gain conversions of the input analog signal are alternately available at the output of the analog to digital converter circuit.
2. An A/D encoder as defined in claim 1 being fur-



ed capacitor resistances. An operational amplifier 21 includes a non-inverting input which is used as a stabilizing node for mid-point operating bias potential. The bias potential is generated by the capacitor 22 and the switched capacitor resistance 27 in response to sign bits from a latch 26 which captures and holds sign bits from the digital output 25, at an 8 KHz sampling rate. A resistance element 40 is connected via a lead 41 to the output of the low pass filter 14 and via a lead 42 to an output of the amplifier 21. An inverting input of the amplifier 21 is capacitively connected to its output via a capacitor (of about 5pf) 23 and is also connected to the resistance element 40 by a variable tap 43. The tap is alterable by a control input shown at 44.

The output mid-point of the amplifier 11 is directly coupled through the filter 14 such that a potential difference between the output of the amplifier 11 and the amplifier 21 appears across the resistance element 40. The variable tap 43, when adjusted, travels through a d.c. potential difference which counter balances the d.c. output of the amplifier 20 such that it remains at about the preferred mid-point even during those periods shorter than the time constant of the integrating function of the elements 22 and 27.

An example of the resistance element 40 is illustrated in more detail in figure 5. This example is particularly adapted to being integrated in the CMOS technology. Thirty-two columns labeled C0-C31 each include ten field effect transistors being arranged in a series string and terminating at a rail which corresponds to the variable tap 43. Thirty-two corresponding resistance segments, labelled R1-R32, are connected in series between the leads 41 and 42. The first column C0 is connected to a junction of the lead 41 and the resistance segment R1, and the second column C1 is connected to a junction between resistance segments R1 and R2 and so on as illustrated.

The control input 43 includes five leads labelled A-E, each of which is connected to gate electrodes, as exemplified at 55, of a pair of the field effect transistor (FET) in each of the columns and which are of opposite conductivity type. For convenience, this is illustrated by one of the pair having a gate electrode with an inversion symbol 55' attached.

For example, in column C0 a FET 52 is paired with a FET 53 which includes the inversion symbol. Both the FETs 52 and 53 include gate electrodes which are connected to the lead 43A but the FETs 52 and 53 respond oppositely to a control signal on the lead so that when one FET is OFF, the other is ON. For simplicity of illustration, the control leads are shown as running straight across each respective row. This is intended to indicate that the gate electrode of each of the FETs is connected to its respective control lead. It will be noticed that in each column, half of the FETs are each bridged by a conductive path, as exemplified at 54. The conductive paths or

bridges are organized in a prearranged pattern such that only one of the columns C0-C31 will be switched ON in the presence of any five bit binary word applied at control input 44. More particularly in this pattern, one of each FET pair is bridged while the other is not, such that the bridged FET is of no function. Therefore, each of the leads A-E is of effect with respect to only one FET in each row even though it is connected to its respective pair of FETs in each row. This particular structure was arrived at as a matter of convenience in fabricating the example embodiment in the MOS technology.

In this particular example of the encoder in figure 4, the resistance element is so arranged to provide a gain alteration of 1.7 decibel steps through a range of 52.7 decibels.

Claims

1. An analog to digital (A/D) encoder for providing digital words being representative of samples of an input analog signal, including:

an analog to digital converter circuit (13), having an input and an output, for generating said digital words each consisting of plural bits including a sign bit;

a first amplifier means (11) for generating a first analog signal with fixed gain in response to the input analog signal;

a first feedback means (16, 17) being for mid-operating point stabilizing the operation of the first amplifier means, in response to the sign bits;

the analog to digital encoder being characterized by:

a second amplifier means (21) for generating a second analog signal with variably controllable gain, in response to the first analog signal;

a second feedback means (26, 27) being for mid-operating point stabilizing the operation of the second amplifier means, in response to the sign bits corresponding to the variably controllable gain analog signal; and

a switch (45, 46) for alternately connecting the first and second analog signals to the input of the analog to digital converter circuit and for likewise alternately connecting the first and second feedback means to the output of the digital converter circuit;

whereby first and second digital words corresponding to fixed and variable gain conversions of the input analog signal are alternately available at the output of the analog to digital converter circuit.

2. An A/D encoder as defined in claim 1 being fur-



ther characterized in that the second analog signal is supplied to the converter circuit in inverse relationship to the fixed gain analog signal generated by the first amplifier means.

3. An A/D encoder as defined in claim 1 wherein the second amplifier means is responsive to an externally supplied control signal for defining an amount of amplification the first analog signal is subjected to in the generation of the second analog signal.

4. An A/D encoder as defined in claim 1 being characterized in that the second amplifier means includes a resistance means (40) with a variable tap means (43), the resistance means being coupled across the first and second analog signals and the variable tap means being connected to an input of the second amplifier means, whereby the second amplifier means is responsive to an externally supplied control signal for defining an amount of amplification the first analog signal is subjected to in the generation of the second analog signal.

5. An A/D encoder as defined in claim 4 being wherein the externally supplied control signal is a digital control signal having plural bits, and the A/D encoder is further characterized in that the resistance means includes a plurality of resistance segments joined in series between an output of the first amplifier means and an output of the second amplifier means, and the variable tap means includes a plurality of switch means being arranged to provide a connection between the input of the second amplifier means and a one of the resistance segments in response to the digital control signal.

6. An A/D encoder as defined in claim 1 being characterized in that the switch means is absent, the input of the analog to digital converter circuit being exclusively connected to receive the second analog signal, the output of the analog to digital converter circuit being connected in common to both the first and second feed back means, and the first feedback means being inversely responsive to the sign bits of the second digital words, whereby the digital words are solely representative of variable gain conversions of the input analog signal.

7. A method for providing digital words being representative of samples of an input analog signal, including the steps of;

a) generating first digital words each consisting of plural bits including a sign bit in response to a first analog signal;

b) amplifying the input analog signal with a fixed predetermined gain in response to previous occurrences of the sign bits, being generated in step a), to provide said first analog signal having a mid-operating point stabilized characteristic;

the method being characterized by the steps of:

c) generating second digital words each consisting of plural bits including a sign bit in response to a second analog signal;

d) amplifying said first analog signal having said mid-operating point stabilized characteristic with a controllably varied gain in response to previous occurrences of the sign bits being generated in step c), to provide said second analog signal having a mid-operating point stabilized characteristic;

whereby the intensity of an audible signal represented by the second digital words is controllably variable.

8. A method as defined in claim 7, further characterized in step d) in that the second analog signal is provided in inverse relationship to said first analog signal.

9. A method as defined in claim 7, further characterized in step d) by amplifying said first analog signal with a gain being varied in accordance with an externally supplied control signal in the form of a plural bit binary word.

10. A method as defined in claim 7, wherein step a) is not performed, there being only the digital words of step c) being generated, and wherein step b) is characterized in that said amplifying is performed in inverse response to the previous occurrences of the sign bits being generated in step c).

11. An A/D encoder as defined in claim 1 further characterized in that the switch means is operative to couple the first and second analog signals to the input of the analog to digital converter circuit at a fixed rate being at least twice that of a Nyquist frequency; and

wherein the converter circuit is operated at said fixed rate, whereby encoded samples of the signals from the first and second means are alternately available at an output of the converter circuit.

12. An A/D encoder as defined in claim 6, wherein the externally supplied control signal is a digital control signal having plural bits, and the A/D encoder is further characterized in that the resistance means includes a plurality of resistance seg-



ments joined in series between an output of the first amplifier means and an output of the second amplifier means, and the variable tap means includes a plurality of switch means being arranged to provide a connection between the input of the second amplifier means and a one of the resistance segments in response to the digital control signal.

13. An A/D encoder as defined in claim 1 wherein the second amplifier means includes a voltage divider (40) being connected between outputs of the first and second amplifier means and including at least two voltage tap positions.
14. An A/D encoder as defined in claim 1 wherein the second amplifier means comprises:
a differential amplifier (21) having an output for supplying said variable gain analog signal and an inverting input; and
a voltage divider (40) being connected between an output of the first amplifier means and the output of the differential amplifier, and including a plurality of voltage tapable positions (C0-C31), any one of which being selectably connected to the inverting input.
15. An A/D encoder as defined in claim 14 wherein the voltage divider comprises a plurality of resistance segments (R1-R32) and a plurality of corresponding switch means (52) being connected between each of the resistance segments and the inverting input.
16. An A/D encoder as defined in claim 15 wherein each of said switch means consists of a column of field effect transistor devices (53) being connected row on row in common with corresponding gate control leads (A-D), the field effect transistor devices being arranged in opposite responsive combinations and being selectively bridged, such that a binary word being applied to said control leads causes one column to be of a much higher conductance than any of the other columns.
17. An A/D encoder as defined in claim 14 wherein the voltage divider is responsive in operation to n bit binary words, and comprises:
n leads for application of the binary words thereto, each of the n leads being connected to control 2n switching devices (52), each of the 2n switching devices being arranged in a corresponding column of at least n switching devices, each of said columns being connected between a common rail (43) and a corresponding voltage tap of a segmented resistance rail having 2n resistance segments (R1-R32) connected in series

between the output of the first means and the output of the differential amplifier in the second means, said common rail being connected to the inverting input of the differential amplifier.

Patentansprüche

1. Analog-/Digital-(A/D-) Codierer zur Lieferung von Digitalworten, die Abtastproben eines Analog-Eingangssignals darstellen, mit
einer Analog-/Digital-Umsetzerschaltung (13) mit einem Eingang und einem Ausgang zur Erzeugung der Digitalworte, die jeweils aus mehreren Bits unter Einschluß eines Vorzeichenbits bestehen,
einer ersten Verstärkereinrichtung (11) zur Erzeugung eines ersten Analogsignals mit einer festen Verstärkung in Abhängigkeit von dem Analog-Eingangssignal,
eine erste Rückführungseinrichtung (16, 17), die zur Arbeitsmittelpunkt-Stabilisierung der Betriebsweise der ersten Verstärkereinrichtung in Abhängigkeit von den Vorzeichenbits dient, wobei der Analog-/Digital-Codierer gekennzeichnet ist durch:
eine zweite Verstärkereinrichtung (21) zur Erzeugung eines zweiten Analogsignals mit in veränderlicher Weise steuerbarer Verstärkung in Abhängigkeit von dem ersten Analogsignal,
eine zweite Rückführungseinrichtung (26, 27), die zur Arbeitsmittelpunkt-Stabilisierung der Betriebsweise der zweiten Verstärkereinrichtung in Abhängigkeit von den Vorzeichenbits dient, die dem eine in veränderlicher Weise steuerbare Verstärkung aufweisenden Analogsignal entsprechen, und
einen Schalter (45, 46) zum abwechselnden Verbinden der ersten und zweiten Analogsignale mit dem Eingang der Analog-/Digital-Umsetzerschaltung und in gleicher Weise zum abwechselnden Verbinden der ersten und zweiten Rückführungseinrichtungen mit den Ausgang der Digitalumsetzerschaltung,
wodurch erste und zweite Digitalworte, die den eine feste und eine veränderliche Verstärkung aufweisenden Umsetzungen des Analog-Eingangssignals entsprechen, abwechselnd am Ausgang der Analog-/Digital-Umsetzerschaltung verfügbar sind.
2. A/D-Codierer nach Anspruch 1, der weiterhin dadurch gekennzeichnet ist, daß das zweite Analogsignal der Umsetzerschaltung in invertierter Beziehung zu dem eine feste Verstärkung aufweisenden Analogsignal zugeführt wird, das durch die erste Verstärkereinrichtung erzeugt wird.



3. A/D-Codierer nach Anspruch 1, bei dem die zweite Verstärkereinrichtung auf ein von außen zugeführtes Steuersignal anspricht, um ein Ausmaß der Verstärkung festzulegen, dem das erste Analogsignal bei der Erzeugung des zweiten Analogsignals unterworfen wird. 5

4. A/D-Codierer nach Anspruch 1, dadurch gekennzeichnet, daß die zweite Verstärkereinrichtung eine Widerstandseinrichtung (40) mit einer veränderbaren Anzapfungseinrichtung (43) einschließt, daß die Widerstandseinrichtung längs der ersten und zweiten Analogsignale angeschaltet ist, während die veränderbare Anzapfungseinrichtung mit einem Eingang der zweiten Verstärkereinrichtung verbunden ist, wodurch die zweite Verstärkereinrichtung auf ein von außen zugeführtes Steuersignal anspricht, um das Ausmaß der Verstärkung festzulegen, dem das erste Analogsignal bei der Erzeugung des zweiten Analogsignals unterworfen ist. 10
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5. A/D-Codierer nach Anspruch 4, bei dem das von außen zugeführte Steuersignal ein digitales Steuersignal mit mehreren Bits ist und bei dem der A/D-Codierer weiterhin dadurch gekennzeichnet ist, daß die Widerstandseinrichtung eine Vielzahl von Widerstandssegmenten einschließt, die in Serie miteinander verbunden und zwischen einem Ausgang der ersten Verstärkereinrichtung und einem Ausgang der zweiten Verstärkereinrichtung eingeschaltet sind, und daß die veränderbare Anzapfungseinrichtung eine Vielzahl von Schalterelementen einschließt, die jeweils so angeordnet sind, daß sie eine Verbindung zwischen dem Eingang der zweiten Verstärkereinrichtung und einem der Widerstandssegmente in Abhängigkeit von dem digitalen Steuersignal herstellen. 25
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6. A/D-Codierer nach Anspruch 1, dadurch gekennzeichnet, daß die Schaltereinrichtungen fehlen, daß der Eingang der Analog-/ Digital-Umsetzerschaltung ausschließlich zum Empfang des zweiten Analogsignals angeschaltet ist, daß der Ausgang der Analog-/ Digital-Umsetzerschaltung gemeinsam sowohl mit der ersten als auch der zweiten Rückführungseinrichtung verbunden ist, und daß die erste Rückführungseinrichtung in invertierter Weise auf die Vorzeichenbits der zweiten Digitalworte anspricht, wodurch die Digitalworte ausschließlich die mit veränderbarer Verstärkung erfolgenden Umsetzungen des Analog-Eingangssignals darstellen. 40
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7. Verfahren zur Lieferung von Digitalworten, die Abtastproben eines Analog-Eingangssignals darstellen, mit den folgenden Schritten: 55
 - a) Erzeugen erster Digitalworte, die jeweils aus mehreren Bits unter Einschluß eines Vorzeichenbits bestehen, in Abhängigkeit von einem ersten Analogsignal,
 - b) Verstärken des Analog-Eingangssignals mit einer festen vorgegebenen Verstärkung in Abhängigkeit von vorhergehenden Häufigkeiten der Vorzeichenbits, die im Schritt a) erzeugt wurden, um das erste Analogsignal mit einer stabilisierten Arbeitsmittelpunkt-Charakteristik zu liefern,
wobei das Verfahren durch die folgenden Schritte gekennzeichnet ist:
 - c) Erzeugen zweiter Digitalworte, die jeweils aus mehreren Bits unter Einschluß eines Vorzeichenbits bestehen, in Abhängigkeit von einem zweiten Analogsignal,
 - d) Verstärken des ersten Analogsignals mit der stabilisierten Arbeitsmittelpunkt-Charakteristik mit einer in steuerbarer Weise geänderten Verstärkung in Abhängigkeit von vorhergehenden Häufigkeiten der Vorzeichenbits, die im Schritt c) erzeugt wurden, um das zweite Analogsignal mit einer stabilisierten Arbeitsmittelpunkt-Charakteristik zu liefern,
wodurch die Stärke eines durch die zweiten Digitalworte dargestellten Tonfrequenzsignals in steuerbarer Weise veränderlich ist.

8. Verfahren nach Anspruch 7, weiterhin dadurch gekennzeichnet, daß im Schritt d) das zweite Analogsignal in invertierter Beziehung zu dem ersten Analogsignal geliefert wird.

9. Verfahren nach Anspruch 7, dadurch gekennzeichnet, daß im Schritt d) das erste Analogsignal mit einer Verstärkung verstärkt wird, die entsprechend einem von außen zugeführten Steuersignal in der Form eines Mehrbit-Binärwortes geändert wird.

10. Verfahren nach Anspruch 7, bei dem der Schritt a) nicht ausgeführt ist, so daß lediglich die Digitalworte des Schrittes c) erzeugt werden, und bei dem der Schritt b) dadurch gekennzeichnet ist, daß die Verstärkung mit invertiertem Ansprechverhalten auf die vorhergehenden Häufigkeiten der Vorzeichenbits ausgeführt wird, die im Schritt c) erzeugt werden.

11. A/D-Codierer nach Anspruch 1, der weiterhin dadurch gekennzeichnet ist, daß die Schaltereinrichtung so betreibbar ist, daß sie die ersten und zweiten Analogsignale dem Eingang der Analog-/Digital-Umsetzerschaltung mit einer festen Rate zuführt, die zumindestens gleich dem doppelten einer Nyquist-Frequenz ist, und



daß die Umsetzerschaltung mit der festen Rate betrieben wird, so daß die codierten Abtastproben der Signale von den ersten und zweiten Einrichtungen abwechselnd am Ausgang der Umsetzerschaltung verfügbar sind.

12. A/D-Codierer nach Anspruch 6, bei dem das von außen zugeführte Steuersignal ein digitales Steuersignal mit mehreren Bits ist, und bei dem der A/D-Codierer weiterhin dadurch gekennzeichnet ist, daß die Widerstandseinrichtung eine Vielzahl von Widerstandssegmenten einschließt, die in Serie miteinander verbunden und zwischen dem Ausgang der ersten verstärkereinrichtung und einem Ausgang der zweiten Verstärkereinrichtung angeschaltet sind, und daß die veränderliche Anzapfungseinrichtung eine Vielzahl von Schaltereinrichtungen einschließt, die so angeordnet sind, daß sich eine Verbindung zwischen dem Eingang der zweiten Verstärkereinrichtung und einem der Widerstandssegmente in Abhängigkeit von dem digitalen Steuersignal ergibt.

13. A/D-Codierer nach Anspruch 1, bei dem die zweite Verstärkereinrichtung einen Spannungsteiler (40) einschließt, der zwischen Ausgängen der ersten und zweiten Verstärkereinrichtung eingeschaltet ist und zumindestens zwei Spannungsanzapfpositionen einschließt.

14. A/D-Codierer nach Anspruch 1, bei dem die zweite Verstärkereinrichtung folgende Teile umfaßt:
einen Differenzverstärker (21) mit einem Ausgang zur Lieferung des eine veränderliche Verstärkung aufweisenden Analogsignals und mit einem invertierenden Eingang, und
einem Spannungsteiler (40), der zwischen einem Ausgang der ersten Verstärkereinrichtung und dem Ausgang des Differenzverstärkers angeschaltet ist und eine Vielzahl von Spannungsanzapfpositionen (C0 - C31) einschließt, von denen irgendeine selektiv mit dem invertierenden Eingang verbindbar ist.

15. A/D-Codierer nach Anspruch 14, bei dem der Spannungsteiler eine Vielzahl von Widerstandssegmenten (R1 - R32) und eine Vielzahl von entsprechenden Schalterelementen (52) umfaßt, die jeweils zwischen jedem der Widerstandssegmente und dem invertierenden Eingang eingeschaltet sind.

16. A/D-Codierer nach Anspruch 15, bei dem jedes Schalterelement aus einer Spalte von Feldeffekttransistorbauteilen (53) besteht, die Reihe an Reihe gemeinsam mit entsprechenden Gate-Steuerleitungen (A - D) verbunden sind, wobei

die Feldeffekttransistorbauteile in in entgegengesetzter Weise ansprechenden Kombinationen angeordnet und selektiv überbrückt sind, derart, daß ein an die Steuerleitungen angelegtes Binärwort bewirkt, daß eine Spalte eine wesentlich höhere Leitfähigkeit aufweist, als irgendeine der anderen Spalten.

17. A/D-Codierer nach Anspruch 14, bei dem der Spannungsteiler im Betrieb auf n-Bit-Binärworte anspricht und folgende Teile umfaßt:

n Leitungen zum Anlegen der Binärworte an diese, wobei jede der n Leitungen zur Steuerung von 2n Schalterelementen (52) angeschaltet ist, wobei jedes der 2n Schalterelemente in einer entsprechenden Spalte von zumindestens n Schalterelementen angeordnet ist und jede der Spalten zwischen einer gemeinsamen Sammelschiene (43) unter einer entsprechenden Spannungsanzapfung einer in Segmente unterteilten Widerstandsschiene verbunden ist, die 2n Widerstandssegmente (R1 - R32) in einer Serienschaltung zwischen dem Ausgang der ersten Einrichtung und dem Ausgang des Differenzverstärkers in der zweiten Einrichtung aufweist, wobei die gemeinsame Sammelschiene mit dem invertierenden Eingang des Differenzverstärkers verbunden ist.

Revendications

1. Codeur analogique-numérique (A/N) destiné à transmettre des mots numériques qui sont représentatifs d'échantillons d'un signal analogique d'entrée, comprenant :

un circuit convertisseur analogique-numérique (13) ayant une entrée et une sortie et destiné à créer les mots numériques formés chacun de plusieurs bits comprenant un bit de signe,

un premier dispositif amplificateur (11) destiné à créer un premier signal analogique de gain fixe à la suite du signal analogique d'entrée, et

un premier dispositif de réaction (16, 17) destiné à stabiliser au point médian de fonctionnement le fonctionnement du premier dispositif amplificateur en fonction des bits de signe,

le codeur analogique-numérique étant caractérisé par :

un second dispositif amplificateur (21) destiné à créer un second signal analogique à gain réglable de manière variable en fonction du premier signal analogique,

un second dispositif à réaction négative (26, 27) destiné à stabiliser au point médian de fonctionnement le fonctionnement du second dispositif amplificateur en fonction des bits de signe



correspondant au signal analogique à gain réglable de manière variable, et

un commutateur (45, 46) destiné à connecter en alternance le premier et le second signal analogique à l'entrée du circuit convertisseur analogique-numérique et à connecter en alternance de manière analogue le premier et le second dispositif à réaction négative à la sortie du circuit convertisseur numérique,

si bien que les premiers et seconds mots numériques correspondant aux conversions à gain fixe et à gain variable du signal analogique d'entrée sont disponibles en alternance à la sortie du circuit convertisseur analogique-numérique.

2. Codeur A/N selon la revendication 1, caractérisé en outre en ce que le second signal analogique est transmis au circuit convertisseur avec une relation inverse par rapport au signal analogique de gain fixe créé par le premier dispositif amplificateur.

3. Codeur A/N selon la revendication 1, dans lequel le second dispositif amplificateur est commandé par un signal de commande transmis depuis l'extérieur et destiné à donner une amplitude d'amplification à laquelle est soumis le premier signal analogique lors de la création du second signal analogique.

4. Codeur A/N selon la revendication 1, caractérisé en ce que le second dispositif amplificateur comporte un dispositif à résistance (40) ayant un dispositif à prise variable (43), le dispositif à résistance étant couplé entre le premier et le second signal analogique et le dispositif à prise variable étant connecté à une entrée du second dispositif amplificateur, si bien que le second dispositif amplificateur est commandé par un signal de commande transmis depuis l'extérieur afin qu'il détermine une amplitude d'amplification à laquelle le premier signal analogique est soumis lors de la création du second signal analogique.

5. Codeur A/N selon la revendication 4, dans lequel le signal de commande transmis depuis l'extérieur est un signal numérique de commande ayant plusieurs bits, et le codeur A/N est en outre caractérisé en ce que le dispositif à résistance comprend plusieurs segments de résistance raccordés en série entre une sortie du premier dispositif amplificateur et une sortie du second dispositif amplificateur, et le dispositif à prise variable comporte plusieurs dispositifs de commutation destinés à assurer la connexion entre l'entrée du second dispositif amplificateur et l'un des segments de résistance en fonction du signal nu-

mérique de commande.

6. Codeur A/N selon la revendication 1, caractérisé en ce que le dispositif de commutation est absent, l'entrée du circuit convertisseur analogique-numérique étant connectée exclusivement pour la réception du second signal analogique, le signal de sortie du circuit convertisseur analogique-numérique étant connecté en commun à la fois au premier et au second dispositif à réaction négative, et le premier dispositif à réaction négative est sensible de manière inverse aux bits de signe des seconds mots numériques, si bien que les mots sont représentatifs uniquement des conversions à gain variable du signal analogique d'entrée.

7. Procédé de transmission de mots numériques représentatifs d'échantillons d'un signal analogique d'entrée, comprenant les étapes suivantes :

- a) la création de premiers mots numériques constitués chacun de plusieurs bits comprenant un bit de signe en fonction d'un premier signal analogique, et
- b) l'amplification du signal analogique d'entrée avec un gain fixe prédéterminé en fonction des apparitions précédentes des bits de signe créés dans l'étape (a) pour la création du premier signal analogique ayant une caractéristique stabilisée à un point médian de fonctionnement,

le procédé étant caractérisé par les étapes suivantes :

- c) la création de seconds mots numériques constitués chacun de plusieurs bits comprenant un bit de signe en fonction d'un second signal analogique, et
- d) l'amplification du premier signal analogique ayant la caractéristique stabilisée au point médian de fonctionnement avec un gain variant de façon réglable en fonction des apparitions antérieures des bits de signe créés dans l'étape (c) afin qu'un second signal analogique ayant une caractéristique stabilisée à un point médian de fonctionnement soit créé,

si bien que l'intensité du signal audible représenté par les seconds mots numériques peut être réglée de manière variable.

8. Procédé selon la revendication 7, caractérisé en outre en ce que, dans l'étape d), le second signal analogique présente une relation inverse avec le premier signal analogique.

9. Procédé selon la revendication 7, caractérisé en outre en ce qu'il comprend, dans l'étape d), l'amplification du premier signal analogique avec un gain qui varie en fonction d'un signal de comman-



de transmis depuis l'extérieur sous forme d'un mot binaire à plusieurs bits.

10. Procédé selon la revendication 7, dans lequel l'étape a) n'est pas exécutée, et seuls les mots numériques de l'étape c) sont créés, et dans lequel l'étape b) est caractérisée en ce que l'amplification est réalisée en raison inverse des apparitions antérieures des bits de signe créés dans l'étape c).

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11. Codeur A/N selon la revendication 1, caractérisé en outre en ce que le dispositif de commutation est destiné à coupler le premier et le second signal analogique à l'entrée du circuit convertisseur analogique-numérique à une fréquence fixe qui est au moins le double de la fréquence de Nyquist, et

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dans lequel le circuit convertisseur fonctionne à la fréquence fixe, si bien que les échantillons codés des signaux provenant du premier et du second dispositif sont disponibles en alternance à une sortie du circuit convertisseur.

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12. Codeur A/N selon la revendication 6, dans lequel le signal de commande transmis de l'extérieur est un signal numérique de commande ayant plusieurs bits, et le codeur A/N est en outre caractérisé en ce que le dispositif de résistance comprend plusieurs segments de résistance montés en série entre une sortie du premier dispositif amplificateur et une sortie du second dispositif amplificateur, et le dispositif à prise variable comprend plusieurs dispositifs de commutation destinés à assurer la connexion entre l'entrée du second dispositif amplificateur et l'un des segments de résistance sous la commande du signal numérique de commande.

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13. Codeur A/N selon la revendication 1, dans lequel le second dispositif amplificateur comprend un diviseur de tension (40) connecté entre les sorties du premier et du second dispositif amplificateur et comprenant au moins deux positions de prise de tension.

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14. Codeur A/N selon la revendication 1, dans lequel le second dispositif amplificateur comprend :
un amplificateur différentiel (21) ayant une sortie destinée à transmettre le signal analogique à gain variable et une entrée d'inversion, et

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un diviseur (40) de tension connecté entre une sortie du premier dispositif amplificateur et la sortie de l'amplificateur différentiel et comprenant plusieurs positions (C0-C31) de prise de tension dont l'une quelconque peut être connectée sélectivement à l'entrée d'inversion.

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15. Codeur A/N selon la revendication 14, dans lequel le diviseur de tension comprend plusieurs segments de résistance (R1-R32) et plusieurs dispositifs correspondants de commutation (52) connectés entre chacun des segments de résistance et l'entrée d'inversion.

16. Codeur A/N selon la revendication 15, dans lequel chaque dispositif de commutation comprend une colonne de dispositifs (53) à transistors à effet de champ connectés ligne par ligne en commun avec des fils correspondants (A/N) de commande de grille, les dispositifs à transistors à effet de champ étant disposés en combinaison, étant commandés en sens opposé et étant mis sélectivement sous forme de ponts afin qu'un mot binaire appliqué aux fils de commande provoque la mise d'une colonne à une conductance bien supérieure à celle de toutes les autres colonnes.

17. Codeur A/N selon la revendication 14, dans lequel le diviseur de tension est commandé pendant le fonctionnement par des mots binaires à n bits, et il comprend :

n fils destinés à l'application des mots binaires, chacun des n fils étant connecté à 2n dispositifs de commutation (52), chacun des 2n dispositifs de commutation étant placé dans une colonne correspondante d'au moins n dispositifs de commutation, chacune des colonnes étant connectée entre un collecteur commun (43) et une prise correspondante de tension d'un collecteur segmenté de résistance ayant 2n segments de résistance (R1-R32) connectés en série entre la sortie du premier dispositif et la sortie de l'amplificateur différentiel du second dispositif, le collecteur commun étant connecté à l'entrée d'inversion de l'amplificateur différentiel.