

Description

The present invention relates to circuitry for producing a substantially jitter-free clock signal.

In video signal processing systems which include field or frame memories, for example, a frame comb filter, it may be desirable to use a sampling clock signal that is locked in phase to the horizontal line synchronizing signal component of the processed video signals. When a line-locked sampling clock signal is used, the number of samples in each line interval and, thus, the number of samples in each field interval remains substantially constant from field to field. This consistency is desirable to ensure that corresponding samples from successive fields or frames of the video signal are properly aligned for processing.

EP-A-185779, EP-A-189195 and JP-A-60197015, each disclose a conventional phase locked loop or phase alignment arrangement using a stable frequency clock signal provided by a precise crystal reference oscillator.

A typical line-locked clock signal generator is described in U.S. Patent No. 4,476,490 entitled "Horizontal Scanning Frequency Multiplying Circuit". This clock signal generator includes a phase-locked loop (PLL) which produces a signal having a frequency of Nf_H , N times the horizontal line scanning frequency, f_H . The PLL used in the referenced patent is shown in FIGURE 1, labelled "prior art". In this system, a horizontal synchronizing signal, HORIZ SYNC, separated from the input composite video signal, is applied to one input terminal of a phase comparator 14. Another input terminal of the phase comparator 14 is coupled to receive a signal, provided by a frequency divider 17, which has substantially the same frequency as the signal HORIZ SYNC. The phase comparator 14 produces an output signal which is proportional to the difference in phase between the signals applied to its input ports. The signal provided by the phase comparator 14 is applied to a low-pass filter 15, the loop filter of the PLL. The filter 15 includes circuitry for integrating the phase difference signal to develop a signal which is proportional to the difference in frequency between the signal HORIZ SYNC and the signal provided by the divider 17. This frequency difference signal is applied to the control input terminal of a voltage controlled oscillator (VCO) 16. The VCO 16, which has a free running frequency substantially equal to Nf_H , produces the output clock signal CK. This clock signal is applied to the input terminal of the frequency divider 17 to complete the loop. The signal CK produced by the VCO exhibits changes in frequency which track changes in the frequency of the horizontal line synchronizing signal, HORIZ SYNC.

Although the clock signal, CK, produced by the PLL system shown in FIGURE 1, is locked in phase to the horizontal line synchronizing signal, the frequency of the signal CK may not be an exact integer

multiple of the frequency of the signal HORIZ SYNC. Assuming that the frequency, F_H , of the signal HORIZ SYNC remains constant, the clock signal, CK, may vary in frequency between slightly more than $(N-1)f_H$ and slightly less than $(N+1)f_H$ without producing a change in the phase of the signal provided by the frequency divider 17. If the frequency of the signal CK is less than or equal to $(N-1)f_H$ or greater than or equal to $(N+1)f_H$, the phase of the signal provided by the circuitry 17 will change and the error in the frequency of the signal CK will be corrected.

The range of frequencies between $(N-1)f_H$ and $(N+1)f_H$ defines the amount of "jitter" which will be tolerated by the PLL. For example, in an NTSC television receiver which uses a nominal sampling frequency of $910 f_H$ (14.318 MHz), the clock signal may vary between $909 f_H$ (14.302 MHz) and $911 f_H$ (14.334 MHz) and still be locked in phase to the horizontal line synchronizing signal. While this amount of jitter may not change the number of samples produced from each horizontal line, it is significant as it relates to the timing of the first sample on a line relative to the horizontal synchronization pulse for that line. In the NTSC television receiver described above, due to the jitter in the clock signal, the first sample on a given line may be taken at any time within 70 ns after the positive-going transition of the horizontal synchronization pulse. This variation in the timing of the initial sample on a line also applies to subsequent samples on the line and may, therefore, distort the reproduced image. This timing variation would cause vertical or diagonal lines in the image to appear wavy or jagged.

It would be advantageous if the circuitry which generated the sampling clock signal also included circuitry for eliminating the jitter from the clock signal.

An aspect of the invention is specified in the claims.

In an embodiment of the present invention there is provided a system for generating a clock signal which is compensated for variations in frequency. The system includes a source of first reference signal and a source of second reference signal. Each of the first and second reference signals have a frequency that is substantially equal to a predetermined frequency. A phase locked loop is provided which is coupled to said source of first reference signal for generating an oscillatory signal that is locked in phase to the first reference signal, wherein the oscillatory signal has a nominal frequency of N times the predetermined frequency, N being an integer greater than 1, and is subject to undesirable variations in frequency between predetermined minimum and maximum values. Signal phase alignment circuitry is coupled to the phase locked loop for generating the clock signal compensated for the undesirable variations in frequency of said oscillatory signal. The phase alignment circuitry includes means responsive to the oscillatory signal for developing M oscillatory signals representing M

respectively different phases of the oscillatory signal where M is an integer greater than 1 and means responsive to the second reference signal for continually selecting one of the M oscillatory signals as the clock signal having a transition which is approximately coincident with a transition in the second reference signal.

A further embodiment of the invention includes a delay element in the phase locked loop which causes the clock signal and the second reference signal to be advanced in phase with respect to the first reference signal.

FIGURE 1 (prior art) is a block diagram of a conventional line locked clock generator.

FIGURE 2 is a block diagram of a portion of a television signal processing circuit which includes an embodiment of the present invention.

FIGURE 3 is a block diagram of phase alignment circuitry suitable for use in the signal processing circuitry shown in FIGURE 2.

FIGURES 4A through 4I are timing diagrams useful for explaining the operation of the circuitry shown in FIGURES 2 and 3.

In the drawings, broad arrows represent busses for conveying multiple-bit parallel digital signals and line arrows represent connections for conveying analog signals or single-bit digital signals. Depending on the processing speed of the devices, compensating delays may be required in certain of the signal paths. One skilled in the art of analog and digital signal processing circuit design would know where such delays would be needed in a particular system.

FIGURE 2 is a block diagram showing a portion of a partly analog, partly digital television receiver which incorporates the present invention. In FIGURE 2, a source of composite video signals 210, which includes the tuner, IF amplifier and video detector of a conventional television receiver, provides NTSC composite video signals to luminance/chrominance separation circuitry 212. The circuitry 212 used with this embodiment of the invention includes a low-pass filter (not shown) and a band-pass filter (not shown) for separating the respective luminance signal component, Y, and chrominance-band signal component, C, from the composite video signals. The separated chrominance-band signal, C, is applied to chrominance signal demodulation circuitry 214. The circuitry 214, which, in the present embodiment of the invention includes two synchronous demodulators (not shown), demodulates the signal C to provide two color difference signals, for example, I and Q. The luminance signal, Y, is applied to a compensating delay element 215 which compensates for the processing delay through the chrominance signal demodulation circuitry 214 to provide a luminance signal Y' that is aligned with the I and Q color difference signals produced by the circuitry 214. The luminance signal Y' and the color difference signals I and Q are applied

to respective analog-to-digital converters (ADC's) 216, 218 and 220. The ADC's 216, 218 and 220 sample the respective signals Y, I and Q at instants determined by a sampling clock signal CLK_s. The digital samples provided by the ADC's 216, 218 and 220 are applied to a field memory 222 which, in turn, provides the delayed samples Y'', I' and Q', for application to other video signal processing circuitry (not shown). The circuitry which uses the field memory 222 may include, for example, a field or frame comb filter, a recursive noise reduction system or a freeze field processor.

The sampling clock signal, CLK_s, applied to the ADC's 216, 218 and 220 is a line-locked clock signal, that is, a clock signal which is locked in phase to the horizontal line synchronizing signal component of the composite video signals provided by the source 210. This clock signal is developed by the circuitry described below.

The composite video signals provided by the source 210 are applied to conventional synchronizing signal separation circuitry 224. The circuitry 224 separates the horizontal line synchronizing signal component from the composite video signals and provides this separated signal as the signal HSYNC to one input terminal of a phase comparator 226. Another input terminal of the phase comparator 226 is coupled to receive a signal HD', having the same nominal frequency as the signal HSYNC. The phase comparator 226, which is of conventional design, generates a signal which is proportional to the instantaneous difference in phase between the signals HD' and HSYNC. This phase difference signal is applied to a loop filter 228, which integrates the signal over time to develop a signal representing the difference in frequency between the signals HD' and HSYNC. The frequency difference signal provided by the loop filter 228 is applied to the control input terminal of a conventional voltage controlled oscillator (VCO) 230. The VCO 230, used in this embodiment of the invention, has a free-running frequency of 28.64 MHz which is approximately equal to 8f_{sc}, eight times the frequency, f_{sc}, of the color subcarrier signal component of the composite video signal provided by source 210. The signal, CLK, provided by the VCO 230 is applied to frequency dividing circuitry 232. The circuitry 232 which, in the present embodiment of the invention includes an 11-bit counter, divides the signal CLK, in frequency, by a factor of 1820 to produce a signal HD, having the same nominal frequency as the horizontal line synchronizing signal HSYNC. The signal HD is applied to a delay element 234 which delays the signal HD by a predetermined amount of time, to generate the signal HD' which is applied to the phase comparator 226.

As set forth above, the phase comparator 226 and loop filter 228 adjust the frequency and phase of the VCO 230 so that the signal HD' is aligned in frequency and phase with the signal HSYNC. However,

since the signal HD' is delayed in time, via the delay element 234, with respect to the signal HD, the signal HD leads the signal HSYNC in phase. In other words, the pulses of the signal HD occur prior to corresponding pulses of the signal HSYNC by the amount of time that signals are delayed by the delay element 234. If, for example, the delay element 234 delays the signal HD by an amount of time substantially equal to the processing delay through the sync separator circuitry 224, then the signal HD would be aligned with the horizontal line synchronizing signal component of the composite video signal provided by the source 210. As set forth below, in the present embodiment of the invention the amount of time delay provided by the delay element 234 is selected so that a final horizontal drive signal HD_F and the clock signal CLK_S have a predetermined phase relationship with the horizontal line synchronizing signal components of the luminance signal Y and color difference signals I and Q applied to the respective ADC's 216, 218 and 220.

The phase-advanced horizontal drive signal HD and the clock signal CLK are applied to respectively different input terminals of phase alignment circuitry 236. The phase alignment circuitry used in this embodiment of the invention is shown in FIGURE 3.

In FIGURE 3, the 28.64 MHz clock signal, CLK, is applied to the input terminal of a delay line 310. The delay line 310 used in the present embodiment of the invention is a chain of 31 serially connected buffer circuits, D₁ through D₃₁. Each of the buffer circuits used in the delay line 310 provides a time delay substantially equal to 1/32 times the period of the signal CLK. The delay line 310 has 32 output terminals, one connected to the input terminal of the first buffer circuit in the chain, D₁, and one connected to the output terminal of each of the buffer circuits D₁ through D₃₁. The 32 output terminals of the delay line 310 are coupled to 32 respectively different input terminals of a phase selector 312. The signal HD, provided by the frequency dividing circuitry 232 is also coupled to the phase selector 312. Circuitry suitable for use as the phase selector 312 is disclosed in U.S. Patent No. 3,911,368 entitled "Phase Interpolating Apparatus and Method".

The phase selector 312 has 32 output terminals, one corresponding to each of 32 output terminals of the delay line 310. In operation, the phase selector 312 compares a transition in the signal HD with transitions in each of the 32 phases of the signal CLK provided by the delay line 310 and indicates which phase of the clock signal has a transition which most closely coincides with the transition in the signal HD. The phase alignment circuitry provides a logic one signal on the output terminal which corresponds to this phase. The other 31 output terminals of the phase selector 312 have logic zero output signals.

The 32 output terminals of the phase selector 312 are applied to respectively different input terminals of a line selection encoder 314. The line selection en-

coder 314 used in this embodiment of the invention is a conventional priority encoder. The output signal provided by the line selection encoder 314 is a five-bit signal indicating the number, in binary form, of the output signal of the phase selector 312 which has a value of logic one.

The output signal of the line selection encoder 314 is applied to the control input port of a multiplexer 316. The multiplexer 316 used in this embodiment of the invention is a conventional 32-to-1 multiplexer having 32 signal input terminals each of which is coupled to a respectively different one of the output terminals of the delay line 310. The control signal provided by the line selection encoder 314 conditions the multiplexer 316 to provide, as its output signal, the phase of the signal CLK which corresponds to the phase that was selected by the circuitry 312. The output signal, CLK', of the multiplexer 316 is the output signal of the phase alignment circuitry 236.

Referring to FIGURE 2, the signal CLK' is applied to frequency dividing circuitry 242 which produces a signal CLK'' having a frequency that is one-half of the frequency of the signal CLK (i.e. $910f_H$). The frequency divider 242 used in this embodiment of the invention is a conventional trigger-type flip-flop. This type of flip-flop changes state between logic-one and logic-zero for each positive-going transition of the signal CLK'. The state of the frequency divider 242 is set at the start of each horizontal line by a pulse signal derived from the signal HD provided by the frequency divider circuitry 232. To generate the pulse signal, the signal HD is applied to a delay element 238, which compensates for the processing time through the phase alignment circuitry 236 to produce the final horizontal drive signal, HD_F. The signal HD_F is applied to an edge detector 240 which produces the pulse signal applied to the frequency divider 242. The pulses used in this embodiment of the invention have a pulse width of approximately 20ns. This pulse signal is applied to a preset input terminal of the frequency divider 242. The horizontal drive signal HD_F controls the horizontal deflection circuitry (not shown) of the television receiver partially shown in FIGURE 2.

The signal CLK'', provided by the frequency divider 242 is synchronized to the final horizontal sync signal HD_F so that the first pulse of the signal CLK'' following a pulse of the signal HD_F has a predetermined polarity and occurs within one nano-second of a predetermined time with respect to the final horizontal sync signal HD_F. The signal CLK'' is applied to a delay element 244 which compensates for the processing delay imparted to the video signals Y, I and Q by the sync separator 212, chrominance signal demodulator 214 and/or delay element 215. The signal provided by the delay element 244 is the sampling clock signal, CLK_S.

FIGURES 4A through 4I are waveform diagrams which illustrate the operation of the clock generation

system. FIGURE 4A shows the timing of a positive going transition of the horizontal synchronizing signal component of the composite video signal provided by the source 210. The corresponding transition of the separated horizontal synchronizing signal, HSYNC, is shown in FIGURE 4B. The time delay between the transition in FIGURE 4A and that in FIGURE 4B represents the signal processing delay through the sync separator circuitry 224. FIGURE 4C is a waveform diagram of the component of the separated luminance signal Y' which corresponds to the positive going transition of the horizontal synchronizing signal. The time between the transitions in FIGURE 4A and FIGURE 4C represents the signal processing delay through the luminance/chrominance separation circuitry 212 and the compensating delay element 215.

The signal CLK provided by the VCO 230 is shown in FIGURE 4D. The frequency of this signal may jitter about a nominal frequency as described above in reference to FIGURE 1. The signal HD, generated by the frequency divider 232 from the signal CLK, is shown in FIGURE 4E. The signal HD is advanced with respect to the signal HSYNC by an amount of time t_L , representing the signal processing delay provided by the sync separator 224, and the phase alignment circuitry 236. The phase aligned clock signal CLK', provided by the circuitry 236 is shown in FIGURE 4F. The delay between the positive going transition of the signal HD and the closest positive going transition of the signal CLK' is the signal processing delay through the multiplexer 316 of the phase circuitry 236. The final horizontal drive signal HD_F, and the clock signals CLK'' and CLK_S are shown in FIGURES 4G, 4H and 4I, respectively.

The positive-going transition in the signal HD_F occurs at substantially the same time as the transition in the horizontal line synchronizing signal component of the composite video signal, shown in FIGURE 4A, due to the selection of the delay value t_L . In this embodiment of the invention, t_L is the sum of the processing delay through the sync separator 224 and phase alignment circuitry 236. By advancing the timing of the signal HD by t_L with respect to the signal HSYNC, the delay element 234 compensates for the processing delay through these circuit elements to produce a horizontal drive signal, HD_F, and a clock signal CLK'' that are closely aligned in phase with the horizontal line synchronizing signal components of the video signals provided by the source 210. The clock signal CLK'' is substantially free of jitter with respect to the signal HD_F due to the phase alignment circuitry 236. The sampling clock signal CLK_S, shown in FIGURE 4I is delayed by an amount of time t_C which compensates for the processing delay through the luminance/chrominance separator circuitry 212, and the chrominance demodulator 214 or the delay element 215. The digital samples produced by the ADC's 216, 218 and 220 in response to the clock signal CLK_S

have consistent timing relative to the signal HD_F from line to line and from field to field. In addition, since the signal CLK_S is a line-locked clock signal, the number of samples in each line interval and, so, in each field interval of the sampled video signals is consistent from field to field.

Claims

1. A clock signal generation system comprising:
 - a source of reference signal(224)having a frequency that is substantially equal to a predetermined frequency;
 - a phase locked loop(226,228,230,232)including a controllable oscillator(230)coupled to said source of reference signal for generating an oscillatory signal(clk)that is locked in phase to said reference signal,said oscillatory signal having a nominal frequency of N times said predetermined frequency, N being an integer greater than 1, and is subject to undesirable variations in frequency between predetermined minimum and maximum values,and wherein said phase locked loop includes a divide by N circuit(232)for dividing the frequency of said oscillatory signal by N to generate a further signal having a frequency substantially equal to said predetermined frequency; characterized by:
 - signal phase alignment means(236),coupled to said phase locked loop for generating a clock signal(clk') compensated for the undesirable variations in frequency of said oscillatory signal, including;
 - means(310),responsive to said oscillatory signal for developing M further oscillatory signals representing M respectively different phases of said oscillatory signal where M is an integer greater than 1; and
 - means(312-316)responsive to said oscillatory signal divided by N for continually selecting one of said M oscillatory signals, as said clock signal having a transition which is approximately coincident with a transition in said oscillatory signal divided by N.
2. The clock signal generating system set forth in claim 1, characterized in that;
 - said source provides a television signal including a horizontal line synchronizing signal component;
 - television signal processing means coupled to said source including means for separating the horizontal line synchronizing signal component as said reference signal;
3. The clock signal generating system set forth in claim 2 characterized in that;



system. FIGURE 4A shows the timing of a positive going transition of the horizontal synchronizing signal component of the composite video signal provided by the source 210. The corresponding transition of the separated horizontal synchronizing signal, HSYNC, is shown in FIGURE 4B. The time delay between the transition in FIGURE 4A and that in FIGURE 4B represents the signal processing delay through the sync separator circuitry 224. FIGURE 4C is a waveform diagram of the component of the separated luminance signal Y' which corresponds to the positive going transition of the horizontal synchronizing signal. The time between the transitions in FIGURE 4A and FIGURE 4C represents the signal processing delay through the luminance/chrominance separation circuitry 212 and the compensating delay element 215.

The signal CLK provided by the VCO 230 is shown in FIGURE 4D. The frequency of this signal may jitter about a nominal frequency as described above in reference to FIGURE 1. The signal HD, generated by the frequency divider 232 from the signal CLK, is shown in FIGURE 4E. The signal HD is advanced with respect to the signal HSYNC by an amount of time t_L , representing the signal processing delay provided by the sync separator 224, and the phase alignment circuitry 236. The phase aligned clock signal CLK', provided by the circuitry 236 is shown in FIGURE 4F. The delay between the positive going transition of the signal HD and the closest positive going transition of the signal CLK' is the signal processing delay through the multiplexer 316 of the phase circuitry 236. The final horizontal drive signal HD_F, and the clock signals CLK'' and CLK_S are shown in FIGURES 4G, 4H and 4I, respectively.

The positive-going transition in the signal HD_F occurs at substantially the same time as the transition in the horizontal line synchronizing signal component of the composite video signal, shown in FIGURE 4A, due to the selection of the delay value t_L . In this embodiment of the invention, t_L is the sum of the processing delay through the sync separator 224 and phase alignment circuitry 236. By advancing the timing of the signal HD by t_L with respect to the signal HSYNC, the delay element 234 compensates for the processing delay through these circuit elements to produce a horizontal drive signal, HD_F, and a clock signal CLK'' that are closely aligned in phase with the horizontal line synchronizing signal components of the video signals provided by the source 210. The clock signal CLK'' is substantially free of jitter with respect to the signal HD_F due to the phase alignment circuitry 236. The sampling clock signal CLK_S, shown in FIGURE 4I is delayed by an amount of time t_C which compensates for the processing delay through the luminance/chrominance separator circuitry 212, and the chrominance demodulator 214 or the delay element 215. The digital samples produced by the ADC's 216, 218 and 220 in response to the clock signal CLK_S

have consistent timing relative to the signal HD_F from line to line and from field to field. In addition, since the signal CLK_S is a line-locked clock signal, the number of samples in each line interval and, so, in each field interval of the sampled video signals is consistent from field to field.

Claims

1. A clock signal generation system comprising:
 - a source of reference signal(224)having a frequency that is substantially equal to a predetermined frequency;
 - a phase locked loop(226,228,230,232)including a controllable oscillator(230)coupled to said source of reference signal for generating an oscillatory signal(clk)that is locked in phase to said reference signal,said oscillatory signal having a nominal frequency of N times said predetermined frequency, N being an integer greater than 1, and is subject to undesirable variations in frequency between predetermined minimum and maximum values,and wherein said phase locked loop includes a divide by N circuit(232)for dividing the frequency of said oscillatory signal by N to generate a further signal having a frequency substantially equal to said predetermined frequency; characterized by:
 - signal phase alignment means(236),coupled to said phase locked loop for generating a clock signal(clk') compensated for the undesirable variations in frequency of said oscillatory signal, including;
 - means(310),responsive to said oscillatory signal for developing M further oscillatory signals representing M respectively different phases of said oscillatory signal where M is an integer greater than 1; and
 - means(312-316)responsive to said oscillatory signal divided by N for continually selecting one of said M oscillatory signals, as said clock signal having a transition which is approximately coincident with a transition in said oscillatory signal divided by N.
2. The clock signal generating system set forth in claim 1, characterized in that;
 - said source provides a television signal including a horizontal line synchronizing signal component;
 - television signal processing means coupled to said source including means for separating the horizontal line synchronizing signal component as said reference signal;
3. The clock signal generating system set forth in claim 2 characterized in that;



the television signal provided by said source includes a luminance signal component and a chrominance signal component which includes first and second color difference signal components;

said television signal processing means further includes

means for separating the luminance signal component and the first and second color difference signal components from said television signal; and

analog-to-digital conversion means responsive to said output clock signal for generating first, second and third sampled data digital signals representing, respectively, said separated luminance signal and said separated first and second color difference signals.

4. The clock signal generating system set forth in any preceding claim, characterized in that said phase locked loop includes;

a variable oscillator for generating said oscillatory signal, said variable oscillator being responsive to a control signal for changing the frequency of said oscillatory signal;

signal frequency dividing means, coupled to said variable oscillator, for dividing said first oscillatory signal, in frequency, by a factor of N to develop a second oscillatory signal;

signal delaying means, coupled to said signal frequency dividing means, for delaying said second oscillatory signal by a predetermined amount of time;

phase comparison means, coupled to said signal delaying means, for generating a phase difference signal that is proportional to the difference in phase between said reference signal and said delayed second oscillatory signal; and

means, responsive to said phase difference signal, for generating said control signal to condition said variable oscillator to change frequency in a sense to reduce the magnitude of said phase difference signal.

Patentansprüche

1. Ein Taktsignal-Erzeugungssystem, enthaltend:

- eine Quelle eines Referenzsignals (224) mit einer Frequenz, die im wesentlichen gleich einer vorbestimmten Frequenz ist;
- einen Phasenregelkreis (PLL; 226, 228, 230, 232) mit einem steuerbaren Oszillator (230), der mit der Quelle des Referenzsignals zur Erzeugung eines Schwingungssignals (clk) gekoppelt ist, das phasenstarr mit dem Referenzsignal verriegelt ist, wobei das Schwingungssignal eine Nennfre-

quenz von N mal der vorbestimmten Frequenz hat und N eine ganze Zahl größer als 1 ist, und wobei es unerwünschten Frequenzschwankungen zwischen einem vorbestimmten Minimal- und Maximalwert unterworfen ist und wobei die PLL eine durch N teilende Schaltung (232) zum Teilen der Frequenz des Schwingungssignales durch N enthält, um ein weiteres Signal mit einer Frequenz zu erzeugen, die im wesentlichen gleich der vorbestimmten Frequenz ist; gekennzeichnet durch:

- ein Signalphasen-Abstimm- oder Einstellmittel (236), das mit der PLL zur Erzeugung eines Taktsignals (clk') gekoppelt ist, das hinsichtlich der unerwünschten Frequenzschwankungen des Schwingungssignals kompensiert ist, welches Mittel beinhaltet
 - ein Mittel (310), das auf das Schwingungssignal zum Bilden von M weiteren Schwingungssignalen anspricht, die M jeweils unterschiedliche Phasen des Schwingungssignals repräsentieren, wobei M eine ganze Zahl größer als 1 ist; und
 - ein Mittel (312-316), das auf das durch N geteilte Schwingungssignal anspricht zum fortwährenden Auswählen eines der M Schwingungssignale, wenn das Taktsignal eine Flanke oder einen Übergang hat, der etwa zeitgleich mit der Flanke bzw. dem Übergang in dem durch N geteilten Schwingungssignal auftritt.

2. Taktsignal-Erzeugungssystem nach Anspruch 1, dadurch gekennzeichnet,

- daß die Quelle ein Fernsehsignal bereitstellt, das eine Horizontal-Zellen-Synchronsignal-Komponente enthält;
- daß das Fernsehsignal-Verarbeitungsmittel, das mit der Quelle gekoppelt ist, ein Mittel zum Abtrennen der Horizontal-Zellen-Synchronsignal-Komponente als das Referenzsignal enthält.

3. Taktsignal-Erzeugungssystem nach Anspruch 2, dadurch gekennzeichnet,

- daß das Fernsehsignal, das von der Quelle bereitgestellt wird, eine Luminanzsignal-Komponente und eine Chrominanz-Komponente enthält, die eine erste und eine zweite Farb-Differenzsignal-Komponente enthält;
- daß das Fernsehsignal-Verarbeitungsmittel weiter beinhaltet
 - ein Mittel zum Trennen der Luminanzsignal-Komponente und der ersten und



- zweiten Farb-Differenzsignal-Komponente von dem Fernsehsignal; und
- eine Analog/Digital-Wandlereinrichtung, die auf das Ausgangs-Taktsignal anspricht, zum Erzeugen erster, zweiter und dritter abgetasteter Digitalsignale, die das abgetrennte Luminanzsignal, das abgetrennte erste bzw. zweite Farb-Differenzsignal repräsentieren.

4. Taktsignal-Erzeugungssystem nach einem der vorhergehenden Ansprüche, dadurch gekennzeichnet, daß die PLL beinhaltet:

- einen variierbaren Oszillator zum Erzeugen des Schwingungssignals, der auf ein Steuersignal anspricht zum Ändern der Frequenz des Schwingungssignals;
- ein Signal-Frequenzteiler-Mittel, das mit dem variierbaren Oszillator gekoppelt ist, zum Teilen des ersten Schwingungssignals in seiner Frequenz um einen Faktor N, um ein zweites Schwingungssignal zu bilden;
- ein Signal-Verzögerungsmittel, das mit dem Signal-Frequenzteiler-Mittel gekoppelt ist, zum Verzögern des zweiten Schwingungssignals um einen vorbestimmten Zeitbetrag;
- ein Phasen-Vergleichermittel, das mit dem Signal-Verzögerungsmittel gekoppelt ist, zum Erzeugen eines Phasen-Differenzsignals, das proportional zu der Phasendifferenz zwischen dem Referenzsignal und dem verzögerten zweiten Schwingungssignal ist; und
- ein Mittel, das auf das Phasen-Differenzsignal anspricht, zum Erzeugen des Steuersignals, um den variierbaren Oszillator so zu konditionieren oder zu beeinflussen, daß er seine Frequenz in eine Richtung ändert, um die Größe des Phasen-Differenzsignals zu reduzieren.

Revendications

1. Montage de génération de signaux d'horloge comprenant :

une source de signal de référence (224) comportant une fréquence qui est sensiblement égale à une fréquence prédéterminée ;

une boucle à verrouillage de phase (226, 228, 230, 232) comprenant un oscillateur réglable (230) couplé à ladite source de signal de référence pour générer un signal oscillant (clk) qui est asservi en phase audit signal de référence, ledit signal oscillant possédant une fréquence nominale de N fois ladite fréquence prédéterminée, N étant un nombre entier supérieur à 1 et

est soumis à des variations indésirables en fréquence entre des valeurs minimales et maximales prédéterminées et dans lequel ladite boucle à verrouillage de phase comprend un circuit de division par N (232) pour diviser la fréquence dudit signal oscillant par N pour générer un signal supplémentaire possédant une fréquence sensiblement égale à ladite fréquence prédéterminée ; caractérisé par :

un moyen de réglage de phase du signal (236) couplé à ladite boucle à verrouillage de phase, pour générer un signal d'horloge (clk') corrigé des variations indésirables en fréquence dudit signal oscillant, comprenant :

un moyen (310), sensible audit signal oscillant pour développer M signaux oscillants supplémentaires représentant M phases respectivement différentes dudit signal oscillant ou M est un nombre entier supérieur à 1 ; et

un moyen (312-316) sensible audit signal oscillant divisé par N pour sélectionner de façon continue un desdits M signaux oscillants, en tant que dit signal d'horloge possédant une transition qui est approximativement en coincidence avec une transition dudit signal oscillant divisé par N.

2. Montage de génération de signaux d'horloge selon la revendication 1, caractérisé en ce que :

ladite source fournit un signal de télévision comprenant une composante de signal de synchronisation de ligne horizontale ;

un moyen de traitement du signal de télévision couplé à ladite source comprenant un moyen pour séparer la composante de signal de synchronisation de ligne horizontale en tant que dit signal de référence .

3. Montage de génération de signaux d'horloge selon la revendication 2 caractérisé en ce que ;

le signal de télévision fourni par ladite source comprend une composante de signal de luminance et une composante de signal de chrominance qui inclut les première et seconde composantes de signaux de différence de couleur ;

ledit moyen de traitement du signal de télévision comprend de plus :

un moyen pour séparer la composante de signal de luminance et les première et seconde composantes de signal de signaux de différence de couleurs dudit signal de télévision ; et

un moyen de conversion analogique-numérique sensible audit signal d'horloge de sortie pour générer des premier, second et troisième signaux numériques de données échantillonnées représentant, respectivement, ledit signal de luminance séparé et lesdits premier et second signaux séparés de différence de couleurs.



4. Montage de génération de signaux d'horloge selon l'une quelconque des revendications précédentes, caractérisé en ce que ladite boucle à verrouillage de phase comprend :

un oscillateur variable pour générer ledit signal oscillant, ledit oscillateur variable étant sensible à un signal de commande pour changer la fréquence dudit signal oscillant ; 5

un moyen pour diviser la fréquence de signal couplé audit oscillateur variable destiné à diviser en fréquence ledit premier signal oscillant par un facteur N afin de développer un second signal oscillant ; 10

un moyen de retarder le signal, couplé audit moyen pour diviser la fréquence de signal, destiné à retarder ledit second signal oscillant d'une quantité de temps prédéterminé ; 15

un moyen de comparaison de phase couplé audit moyen pour retarder le signal, afin de générer un signal de différence de phase qui est proportionnel à la différence en phase entre ledit signal de référence et ledit second signal oscillant retardé ; et 20

un moyen, sensible audit signal de différence de phase, destiné à générer ledit signal de commande pour conditionner ledit oscillateur variable en vue de changer la fréquence dans un sens tendant à réduire l'amplitude dudit signal de différence de phase. 25

30

35

40

45

50

55

8