

METAL-OXIDE-SEMICONDUCTOR DYNAMIC RAM.BACKGROUND OF THE INVENTION:

1. Field of the Invention.

The invention relates to the field of semiconductor dynamic memories.

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2. Prior Art.

Metal-oxide-semiconductor (MOS) and complementary MOS (CMOS) dynamic random-access memories (DRAMs) continue to increase in density from, for example, the 1K memories of the late 1960's to the currently used 64K memories of today. The described invention is realized in a 256K CMOS memory, although the inventive concepts described may be utilized in other size memories.

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In DRAMS, typically memory cells each of which include a single transistor and capacitor, are coupled to bit lines. Pairs of bit lines extend from a latch-like sense amplifier. Dummy cells, restore circuits, and architecture employing folded bit lines are commonly used in current DRAMS.

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The capacity of an MOS DRAM can, of course, be increased by employing more memory cells. But unless higher density fabrication is used, that is, smaller cells, etc., the higher capacity memories are not suited for high volume production because the increased substrate area decreases yields. There is, thus, always the continuing goal to shrink the size of the memory cells. However, as the cells are made smaller, they store less charge and it becomes increasingly difficult to sense the binary

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state stored in the cells. It is easier to sense a smaller cell if the bit line capacitance is reduced and this can be achieved with fewer cells on the bit lines allowing them to be shortened. On the other hand, where greater array efficiency is sought, it is helpful if more cells are placed along each of the bit lines. Using shorter bit lines require more sense amplifiers, consequently, some of the increased density gained by using smaller cells with shorter bit lines can be lost because of the additional sense amplifiers and related peripheral circuit (e.g., decoders).

One prior art suggestion, although not commercialized, is to multiplex pairs of bit lines to a single sense amplifier. This technique, in theory, permits use of the shortened bit lines without requiring additional sense amplifiers.

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In some prior art DRAMs, bit lines are precharged to the full power supply potential, for example, five volts. In others, the bit lines are charged to a reference potential such as half the power supply potential. These precharging techniques are used both with and without dummy cells. An obvious advantage to charging to one-half the power supply potential is that the memory consumes less power. However, there are a number of problems with this system. In one case, the bit lines are precharged during an inactive cycle. The power supply potential can vary between the

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time of the precharging and the actual sensing and this variation causes difficulty in sensing. Another problem with precharging the bit lines to half the power supply potential is that poor performance results when the power supply potential is low. With the described invention, the bit lines are charged to half the power supply potential in a unique way and in combination with the multiplexing mentioned above. Not only is less power consumed, but also the peak currents are reduced with the present invention.

For recent discussions of DRAM technology, see (1) "A 90NS 256Kx1B DRAM With Double Level AL Technology", ISSCC Digest of Technical Papers pages 226-227, Feb. 1983, by Fujii, T. et al; (2) "A 64Kb CMOS RAM", ISSCC Digest of Technical Papers pages 258,259, Feb. 1982, by Konishi, S. et al, (3) "A 70NS High Density CMOS DRAM", ISSCC Digest of Technical Papers pages 56-57, Feb. 1983, by Chwang, R. et al; (4) "A 100 ns 5 V Only 64K x 1 MOS Dynamic RAM", IEEE Journal of Solid-State Circuits pp. 839-845, Vol. SC-15, No.5. October 1980 by Chan, J. et al; and (5) "A 5V-Only 64K Dynamic RAM Based on High S/N Design", IEEE Journal of Solid-State Circuits p. 846, Vol. SC-15, No. 5, October 1980 by Masuda, H. et al.

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SUMMARY OF THE INVENTION

According to the present invention there is described a metal-oxide-semiconductor (MOS) dynamic, random-access memory (DRAM) comprising:

a first and second pairs of bit lines;

5 a plurality of memory cells coupled to said bit lines;

a sense amplifier;

10 multiplexing means for selectively coupling one of said first and second pairs of bit lines to said sense amplifier, said multiplexing means coupled to said first and second pairs of bit lines and said sense amplifier;

first and second restoring means for selectively restoring potentials on said first and second pairs of bit lines, respectively, during a read/restore cycle, 15 said restoring means coupled to said pairs of bit lines;

said first and second restoring means being separately activated at different time sequence for restoring potentials on said first and second pairs of bit lines at different times;

20 whereby current peaks for said DRAM are reduced.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 is a plan view of the invented memory used to describe the general architecture.

Figure 2 is an electrical schematic of the presently preferred memory cell, bit lines, sense amplifier, restore circuits, multiplexing means and interconnection of the bit lines to the input/output lines.

Figure 3 are timing diagrams used to describe the operation of the circuit of Figure 2.

Figure 4 illustrates the sense amplifier of Figure 2 redrawn for purposes of explanation.

Figure 5 is a diagram used to describe potential levels in the circuit of Figure 4.

Figure 6 are waveforms used to describe current peaks with the invented memory.

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DETAILED DESCRIPTION OF THE INVENTION:

A metal-oxide-semiconductor (MOS) dynamic random-access memory (DRAM) is described. In the following description, numerous specific details are set forth such as specific arrays, number of 5 cells, etc. It will be obvious to one skilled in the art that the present invention may be practiced without these specific details. In other instances, well-known circuits associated with DRAMs such as decoders, etc., are not illustrated in order not to unnecessarily obscure the present invention.

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OVERVIEW OF PREFERRED EMBODIMENT

In the currently preferred embodiment, the DRAM is fabricated employing CMOS technology. In particular, the array is fabricated in an n-well using double polycrystalline silicon (polysilicon) technology. The n-well/substrate junction is reverse 15 biased and acts as a minority carrier barrier which reduces soft errors induced by alpha particles. The overall structure of the cell is shown in copending U.S. application, entitled "CMOS DRAM", Serial No. 470,454, filed February 28, 1983, and assigned to the assignee of the present invention.

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In the currently preferred embodiment, the memory is organized as a 256Kx1 memory. Gate oxide thicknesses (second layer of polysilicon) of 250A are used. The cells have an area of approximately $70 \mu\text{m}^2$ with a storage capacitance of approximately

- 55fF. The word line drivers employ a negative "boosted" potential which yields an average cell stored charge of approximately 275fC. The bit line to cell capacitance ratio is approximately 12-to-1 providing a 190mV signal for sensing over a wide operating range.
- 5 The memory operates from a five volt potential and draws an average current of 45mA and a standby current of 1mA. A 256 cycle refresh arrangement is used at intervals of 4mS. The substrate on which the entire memory is fabricated includes four redundant rows and columns.
- 10 Access times of less than 100ns. are obtained with row accessing. The memory employs static column circuits, thus permitting a faster "Ripplemode" (a static column mode) access where 512 bits can be accessed with an access time of approximately 40nS. per bit and with a reduced active current of approximately 25mA.

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ARCHITECTURE OF PREFERRED EMBODIMENT

The 256Kx1 organization is realized in the presently preferred embodiment with 16K arrays 10 as shown in Figure 2. The arrays 10 are paired and each pair is separated by a row of sense amplifiers 14. The restore circuits 16 are formed in rows generally parallel to the sense amplifiers at the outer edges of each pair of arrays 10. The column decoders and data input/output lines are formed in the elongated central portion 12 of the memory. All data transferred into and from the arrays occurs through these centrally disposed input/output lines. The outer arrays communicate with the 25 input/output lines through the bit lines of the inner arrays as will be described in detail in conjunction with Figure 2.

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The row decoders and word line drivers 18 are formed in two horizontal bands. Dual row decoders are used in these bands. The peripheral circuits, for the most part, are located in the regions 20. These include the input/output buffering for data, the 5 buffering for addresses and timing signals such as the standard RAS/ and CAS/ signals. As is commonly done, these buffers provide TTL to MOS signal level shifting.

SENSE AMPLIFIER MULTIPLEXING AND RESTORE CIRCUITS

In Figure 2, two pairs of bit lines, lines 23 and 24, and 10 lines 25 and 26, are selectively coupled to the sense amplifier 30 through transistors 33 and 32, respectively. The bit lines 23 and 24 are connected to the complementary input/output lines 40 and 41 through transistors 43. These transistors are selected by the column decoders. For purposes of explanation, the bit lines 23 and 15 24 are referred to as the inside bit lines (BLI and BLI/) and the bit lines 25 and 26 as the outside bit lines (BLO and BLO/). The designation inside and outside represents the bit line pairs' position relative to the input/output lines and sense amplifier 30. (Note the designation "left" and "right" may create ambiguities 20 since the left and right lines would be reversed for the two pairs of bit lines extending to the other side of the input/output lines 40 and 41, shown as lines 54 and 55.) The sense amplifier 30 includes a pair of cross coupled p-type transistors and four capacitors formed from p-channel transistor-like structures. The 25 amplifier receives a sense amplifier strobe (SAS) signal as is commonly used with DRAM sense amplifiers. The operation of the sense amplifier is discussed in detail in conjunction with Figure 4.

A plurality of cells is connected to each of the bit lines, each cell comprises a transistor such as transistor 36 and a storage capacitor such as capacitor 37. Word lines in the array select a single capacitor for coupling to one of the bit lines (of one pair) 5 for reading, writing or refreshing. Note no dummy cells are employed along the bit lines.

Transistors 45 and 46 receive the precharge signal and provide for precharging of the bit lines. In typical operation, after restoration, one bit line is at the full power supply 10 potential (five volts) and the other at ground. Thus, lines 24 and 25 may be at five volts and lines 23 and 26 at ground. The precharging signal causes transistors 45 and 46 to conduct, the charge on the bit line pairs is divided and the bit lines are brought to approximately half the power supply potential, for 15 instance, 2 1/2 volts if the power supply potential is a full five volts. Since the bit lines are only changed to 1/2 the supply potential the active power is reduced by approximately a factor of 2. During this precharging, transistors 32 and 33 conduct, assuring that the nodes within the sense amplifier are also precharged to 20 this one half V_{CC} potential. (In actuality, the bit lines are above 50% of the power supply potential (e.g., at 55%). There is some inherent bootstrapping which occurs from the restore circuits and also the capacitance associated with the junctions is non-linear (e.g., function of voltage). This variation from the 50% figure is 25 process dependent.)

A restore circuit 48 is coupled to the ends of the bit lines

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25 and 26 and similarly, a restore circuit 49 is coupled to the ends of the bit lines 23 and 24. Each of the restore circuits comprises a pair of cross coupled n-type transistors. The restore circuit 48 includes transistor 50 which couples the cross coupled transistors to ground. Similarly, the restore circuit 49 includes transistor 51 which couples the pair of cross coupled transistors in circuit 49 to ground. As will be described in detail, transistors 50 and 51 permit the restore circuits 48 and 49 to be separately activated. This distributes the current consumed for restoring the bit lines into separate periods, thus limiting the peak current. Also, the waveforms used to active the transistors 50 and 51 cause these transistors to conduct gradually, further reducing current peaks.

GENERAL OPERATION OF THE CIRCUIT OF FIGURE 2

Before referring to the detailed timing diagram, it will be helpful to have a general understanding of the operation of the circuit of Figure 2. The circuit operates differently depending upon whether data is being read from the inside bit lines or outside bit lines.

Assume first that data is to be read from one of the outside bit lines, for example, from the cell comprising transistor 37 and capacitor 37. Initially, both transistor pairs 32 and 33 conduct, and the precharging transistors 45 and 46 also conduct. This causes the sense amplifier nodes and both pairs of bit lines to be held at the same potential, approximately $1/2 V_{CC}$. Next, transistors 33 and the precharging transistors 45 and 46 are turned off. The word line is then selected, causing transistor 36 to conduct and line 25 to be either additionally charged, or the charge on the line is

reduced. (Capacitor 37 stores a full potential (e.g., 5V or 0V). An imbalance is caused by the charge from capacitor 37 on the metal bit line 25 and the nodes of the sense amplifier 30. Now transistors 32 are turned off and sensing within the sense amplifier 5 30 occurs. Importantly, this sensing occurs with neither pair of bit lines being connected to the sense amplifier. After sensing occurs, transistors 33 conduct. The amplified data from the capacitor 37 is thus transferred onto the outside bit lines where it can be transferred to the I/O lines 40 and 41. (The specific timing 10 is discussed later for these events.) A restore signal is applied to transistor 51 to restore the inside bit lines. Transistors 32 are also caused to conduct again so that the data sensed by the sense amplifier 30 is transferred onto the outside bit lines. The outside restore circuit 48 is activated by the application of a 15 signal to transistor 50 restoring the outside bit lines, thereby returning capacitor 37 to its original state.

Therefore, when data is sensed on an outside bit line, it is first transferred onto an inside bit line for coupling to the input/output lines. The inside bit lines are restored first, 20 followed by the restoration of the outside bit lines.

Assume now that data is to be sensed along the inside bit line 24. Once again, initially both transistors 32 and 33 are on, and when the transistors 45 and 46 conduct, all the bit lines and the nodes of the amplifier 30 are brought to approximately $1/2$ 25 V_{CC} . After the precharge signal goes low, transistors 32 are turned off and the word line is activated, causing charge to flow onto or from the bit line 24. Then, transistors 33 are turned off

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and sensing occurs within the amplifier 30 by application of the (SAS). When transistors 33 are again turned on, the data is transferred onto lines 40 and 41 as transistors 43 conduct (after restoring the potential on these lines.) The inside bit lines are restored first. Later, transistors 32 are also permitted to conduct, allowing the outside restore circuit 48 to operate as part of precharge cycle.

As was the case with sensing from outside bit lines, the inside bit lines are isolated from the sense amplifier before data from one of these lines is sensed by the sense amplifier. Similarly, one pair of bit lines are restored at a different time than the other pair of bit lines to assure that the current peaks are reduced.

As is apparent from Figure 2, the sense amplifier and cells are all p-channel devices. The cells are fabricated in n-wells spaced-apart from the wells containing the sense amplifiers. The restore circuits and column select transistors are n-channel transistors and are fabricated outside the n-well, in the p-type substrate. (The n-well itself is connected to the positive power supply potential.) By way of example, the full power supply potential of V_{CC} is placed across capacitor 37 assuming that the circuit 48 is set to charge capacitor 37. The word lines are bootstrapped (driven negatively approximately 3 volts below ground potential) to assure complete transfer of charge onto and from capacitor 37 and like capacitors. A full V_{CC} potential is applied to one bit line while the other is connected to ground during restoring. (Full V_{CC} is obtained from the SAS signal and

ground from circuits 48 and 49.)

Decoders are employed to examine each address and determine which ones of the transistors 32 and 33 are to remain coupled to the sense amplifier after the precharge and prior to the sensing. Such
5 decoders are well-known and may be similar to those used for activating dummy loads, or dummy cells, in prior art DRAMs.

It should be noted that since the bit lines are charged to approximately $1/2 V_{CC}$, there is no difficulty transferring charge over transistors 32 and 33.

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WAVEFORMS OF FIGURE 3

Referring to Figure 3, at the beginning of the active cycle, the row address strobe signal (RAS/) as shown by waveform 80, drops in potential. This initiates an active memory cycle. Following the RAS/ signal's drop in potential, precharging occurs. This is
15 indicated by the waveform 81. Unlike prior art memories, precharging occurs during the active cycle. This does not add to access time since decoding of addresses, etc. is accomplished during this precharging. This assures that the precharge potential is referenced to the current V_{CC} . Note that the sense amplifier's
20 strobe signal is on until the precharging occurs and then drops as shown by waveform 82.

In Figure 3, the waveform coupled to the gates of transistors 32 is shown as T1 and for transistors 33 as T2. Waveforms 83 and 84 are for sensing data on an outside bit lines.
25 Initially both sets of transistors 32 and 33 are conducting then transistors 33 are turned off, followed by transistors 32. Transistors 33 are turned on after sensing occurs as indicated by

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the line 86, and sometime later, transistors 32 are then turned on.

The word line potential drops to approximately -3 volts as shown by waveform 85 to fully transfer charge from a cell. For the outside bit line sensing shown, the potentials on these bit lines are shown by waveforms 87. Initially, one line is at five volts and the other at ground, then during the precharge period, both are brought to one-half V_{CC} . One line changes potential slightly when the word line is activated, the other remains at one-half V_{CC} .

- 10 The potentials on the sense amplifier nodes are shown by waveforms 88. Once again, one of these potentials are initially at V_{CC} and the other at ground. After precharge, the nodes are equalized and there is a slight change on one node before sensing begins. Sensing occurs when the SAS signal rises in potential.
- 15 Waveforms 89 represent the potentials on the inside bit lines. Note that as previously discussed, even though a cell is selected on one of these bit lines, they are not restored until after the active cycle as indicated by the rise in potential in waveform 91, the restore signal for the outside restore circuit. Waveform 90
- 20 illustrates that the inside restore occurs first and line 92 shows the separation in time between the inside and outside restoring. The column selection signal rises in potential as shown by waveform 93 shortly after the inside restore signal rises in potential. Thus, the differential on the inside bit lines will be a full
- 25 V_{CC} . The data on the I/O lines is indicated by waveforms 94; and, waveforms 95 illustrates when the data is valid.

All of the above waveforms may be generated with well-known

circuits commonly used in DRAMs. For this reason, the timing circuits have not been shown.

The timing signals for sensing on inside bit lines are substantially the same as those of Figure 3 with the differences 5 discussed above, particularly the timing for transistors 32 and 33.

In the presently preferred embodiment, during a write cycle, no restore circuits are used. They are temporarily deactivated. The bit lines are driven directly from the input/output lines shown in Figure 2. This speeds up the writing cycles. In the prior art, the 10 restore circuits are activated since there is no way of decoupling them. With the present invention, these circuits can be selectively activated as they are during a read/restore cycle and also, both circuits can be left deactivated as they are during a write cycle.

SENSE AMPLIFIER OF FIGURE 4

15 The sense amplifier of Figure 2 has been redrawn in Figure 4 so that both the true and complementary bit lines (both inside and outside) are shown on the same level. Capacitors 61 and 62 are coupled between the nodes 67 and 68 and similarly, capacitors 63 and 64 are coupled between these nodes. The p-channel transistor 50 is 20 coupled between nodes 67 and the node 57 (source of the SAS signal). Its gate is coupled to node 68. Transistor 60 has its gate coupled to node 67, one of its terminals is coupled to node 68 and the other terminal to node 57.

For reasons that will be explained, capacitors 61 and 64 25 have the same capacitance and capacitors 62 (C_1) and 63 (C_2) also have the same capacitance. The capacitance of C_2 is slightly larger than the capacitance of C_1 , by approximately 5%

in the presently preferred embodiment (the specific difference of 5% is not crucial to the present invention).

Ideally, when sensing either a binary one or a binary zero, the swing on the bit line should be the same, although in opposite directions. There are a number of effects which prevent this ideal condition. For instance, when the negative potential is applied to the word line, the capacitive coupling between the word line and bit line (e.g., gate of transistor 36 and line 25 of Figure 2) brings the bit line more negative. Also, the bit line capacitance is not linear with respect to voltage for a number of reasons such as the parasitic capacitance associated with the source and drain regions of transistors 32 and 33. Another effect previously discussed is that the actual precharge potential on the bit lines is not precisely $V_{CC}/2$. The capacitance of the cells themselves is also not linear with respect to voltage. There are other effects which cause deviation from the ideal condition and which make it difficult to sense data particularly as the cell size is reduced.

Briefly in Figure 5, line 71 represents the ideal voltage on the bit lines after precharging. The swing of this line in the more negative direction at section 72 indicates the pull on one of the bit lines which occurs when the word line is activated. (The charge from the cell is being ignored for this explanation.)

The capacitors 61 through 64 provide compensation for the above-described effects among others. From ordinary decoding of the address signals, it can be determined if a cell is to be accessed on either a true bit line or a complementary bit line. Assume that a cell along line 25 is to be accessed. A potential is applied to

line 74 (not line 75). Since capacitor C2 is larger than capacitor C1, line 67 is driven less negatively providing compensation for the above-described effects. This is shown by 73 in Figure 5.

Similarly, if a cell is selected along the true bit lines 23 or 26, the signal is applied to line 75 causing line 68 to be higher in potential than the other bit line providing like compensation.

The capacitors discussed above permit more precise adjustment than can be obtained from using dummy cells, especially where smaller cells are employed. Additionally they provide a D.C. offset which improves gain and compensation in both directions.

REDUCTION IN CURRENT PEAKS

In Figure 6, three waveforms are shown to illustrate the distribution of current that occurs since half the array is restored at one time and the other half at another time. Once again, the RAS/ signal is shown dropping in potential; this initiates an active cycle. During the active cycle, and before the data is valid, restoration of half the bit lines occurs. Later, and in fact, during a precharge cycle (after RAS/ rises in potential) the other half of the bit lines are restored. This reduces peak currents and distributes these large current demands into two separate periods. Also, while not shown in detail in Figure 3, the signals used to activate the restore circuits are ramped. This further reduces the peak current during both restore cycles. These techniques reduce peak currents without adding to access time.

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Thus, a CMOS dram has been described which employs two pairs of bit lines multiplexed onto a single sense amplifier. No dummy cells are employed in the described memory. The bit lines are charged to one-half the voltage supply potential. Peak currents are reduced since half the bit lines are restored during one period of time and the other half are restored during another period of time.

The present application has been divided out of our copending U.K. Patent Application No.8502632 in which there is described a metal-oxide-semiconductor (MOS),dynamic random-access memory (DRAM) comprising:

- a first and a second plurality of memory cells;
- a sense amplifier;
- a first pair of bit lines, coupled to said first cells;
- a first switching means for selectively coupling said first pair of bit lines to said sense amplifier,said first switching means being coupled to said first bit lines and said sense amplifier;
- a second pair of bit lines, coupled to said second cells;
- a second switching means for selectively coupling said second pair of bit lines to said sense amplifier,said second switching means being coupled to said second bit lines and said sense amplifier;
- precharging means for precharging said first and second pairs of bit lines;
- one of said first and second pairs of bit lines being coupled to said sense amplifier by one of said first and second switching means when one of said memory cells on said one pair of bit lines is selected;
- said one switching means decoupling said one pair of bit lines from sense amplifier as said sense amplifier senses data from said one memory cell;
- whereby effective sensing of data in said memory cells is achieved where said bit line pairs are selectively coupled to said sense amplifier.

In our co-pending U.K. Patent Application No. 8700440 there is described and claimed a metal-oxide-semiconductor (MOS) dynamic, random-access memory (DRAM) comprising:

- 5 a first pair of bit lines;
 a plurality of memory cells coupled to said first pair of bit lines;
 a sense amplifier coupled to said first pair of bit lines, said sense amplifier including pairs of imbalanced capacitors which receive signals during sensing, said
10 imbalanced capacitors providing compensation for parasitic coupling of signals to said first pair of bit lines;
 restoring means for selectively restoring potentials
15 on said first pair of bit lines during a read/store cycle, coupled to said first pair of bit lines; and
 precharging means for precharging said bit lines to approximately 1/2 the power supply potential used by said DRAM;
20 whereby improved sensing of signals on said first pair of bit lines occurs.

In our co-pending U.K. Patent Application No. 8700441, there is described and claimed a metal-oxide-semiconductor (MOS) dynamic, random-access memory (DRAM) comprising:

- 25 a first pair of bit lines;
 a plurality of memory cells coupled to said first pair of bit lines;
 a sense amplifier coupled to said first pair of bit
30 lines;
 restoration means for selectively restoring potentials on said first pair of bit lines during a read/store cycle, said restoration means coupled to said bit lines, said restoration means applying a potential
35 approximately equal to the power supply potential to one of said lines while coupling the other of said lines to ground potential;

precharge means for precharging said pair of bit lines to a potential approximately equal to one-half said power supply potential, said precharge means coupling said first pair of bit lines together during
5 an active memory cycle, to cause charges on said pair of bit lines to be divided and to bring said pair of bit lines to said potential approximately equal to one-half said power supply potential,
whereby a low power DRAM is achieved.

CLAIMS

1. A metal-oxide-semiconductor (MOS) dynamic, random-access memory (DRAM) comprising:

a first and second pairs of bit lines;

a plurality of memory cells coupled to said bit lines;

a sense amplifier;

multiplexing means for selectively coupling one of said first and second pairs of bit lines to said sense amplifier, said multiplexing means coupled to said first and second pairs of bit lines and said sense amplifier;

first and second restoring means for selectively restoring potentials on said first and second pairs of bit lines, respectively, during a read/restore cycle said restoring means coupled to said pairs of bit lines;

said first and second restoring means being separately activated at different time sequence for restoring potentials on said first and second pairs of bit lines at different times;

whereby current peaks for said DRAM are reduced.

2. The DRAM defined by claim 1 wherein both said restoring means are deselected for writing into said DRAM.

3. The DRAM defined by claim 1 wherein said sense amplifier is fabricated from devices of a first conductivity type and said restoring means are fabricated from transistors of a second conductivity type.

4. The DRAM defined by claims 1 or 3 including pre-charging means to precharge said pairs of bit lines to one-half the power supply potential used by said DRAM.

5. The DRAM defined by claim 4 wherein said first and second restoring means causes one line from said first pair of bit lines and one line from said second pair of bit lines



to be charged to said full power potential and the other line of said first and second pairs of bit lines to be coupled to ground and wherein said precharging means couples said lines together.

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6. The DRAM defined by claim 1 wherein said second pair of bit lines are selectively coupled to complementary input/output lines.

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7. The DRAM defined by claim 1 wherein said sense amplifier includes pairs of imbalanced capacitors which receive signals during sensing, said imbalanced capacitors providing compensation for parasitic coupling of signals to said bit lines.

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8. The memory defined by claim 3 wherein said first conductivity type is p-type and second conductivity type is n-type.

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