CLAIMS

1. A semiconductor memory device comprising:

a memory cell array including a source line provided above a first surface of a semiconductor substrate, and a word line provided above the source line;

a wall surrounding the memory cell array in a plane along the first surface, including a plurality of conductive layers arranged in a direction crossing the first surface of the semiconductor substrate from a layer of the source line to a layer of the word line, and including a recess at an inner surface extending from an upper surface to a lower surface; and

an insulating layer provided from a position of the upper surface of the wall to a position of the lower surface and being in contact with the inner surface of the wall in the recess.

2. The semiconductor memory device according to claim 1, wherein

the memory cell array comprises:

a selection gate line provided above the word line;

a first region and a second region which are adjacent to each other along a first direction and include the word line and the selection gate line; and

a third region in which the selection gate line in the first region is connected to an interconnect, and

the recess is provided in a region of the inner surface of the wall, facing the third region.

3. The semiconductor memory device according to claim 2, wherein

the memory cell array includes a plurality of interconnects stacked in a direction crossing the first surface of the semiconductor substrate between the source line and the selection gate line, and

the plurality of conductive layers of the wall are located at the same layers as the plurality of interconnects, respectively.