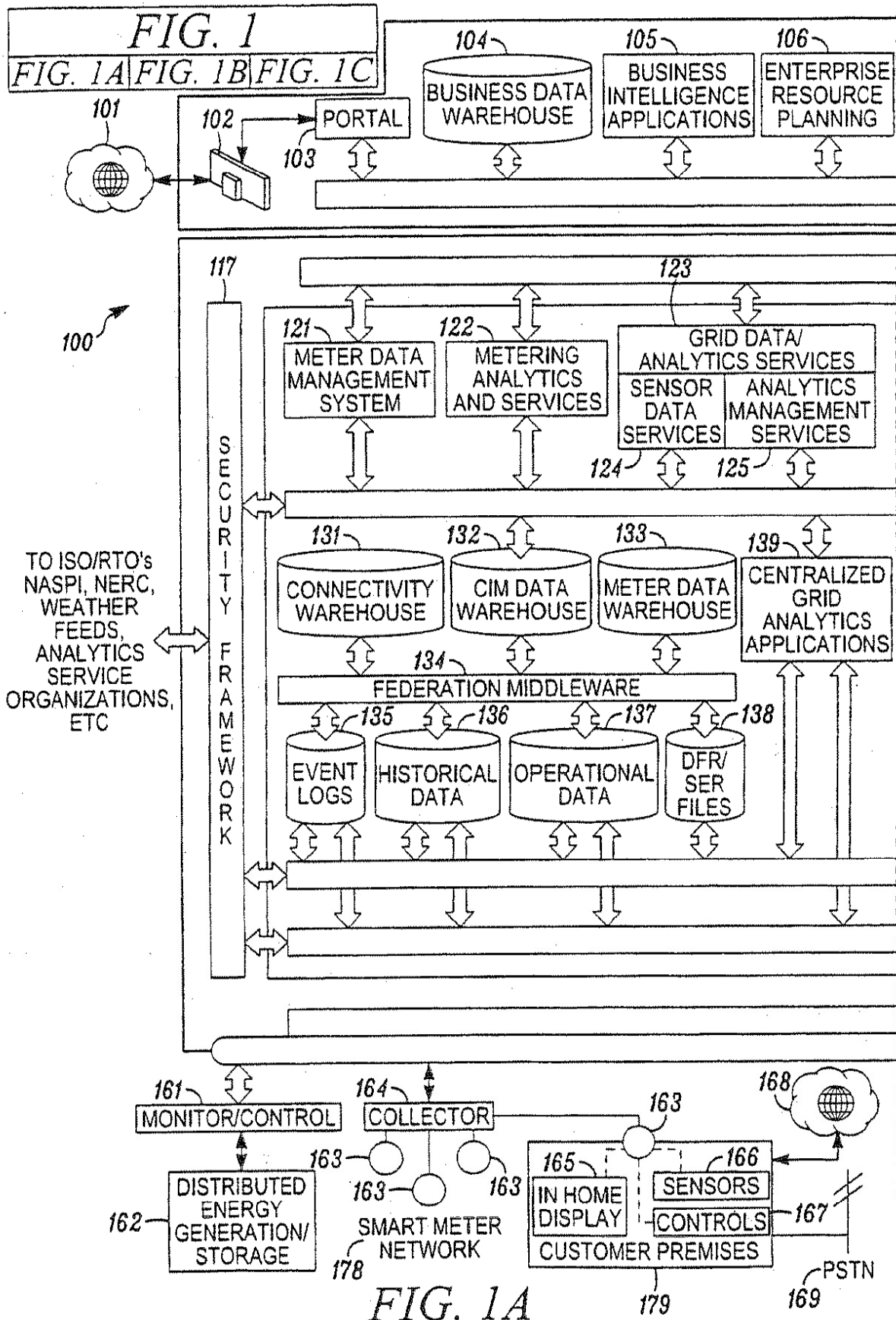




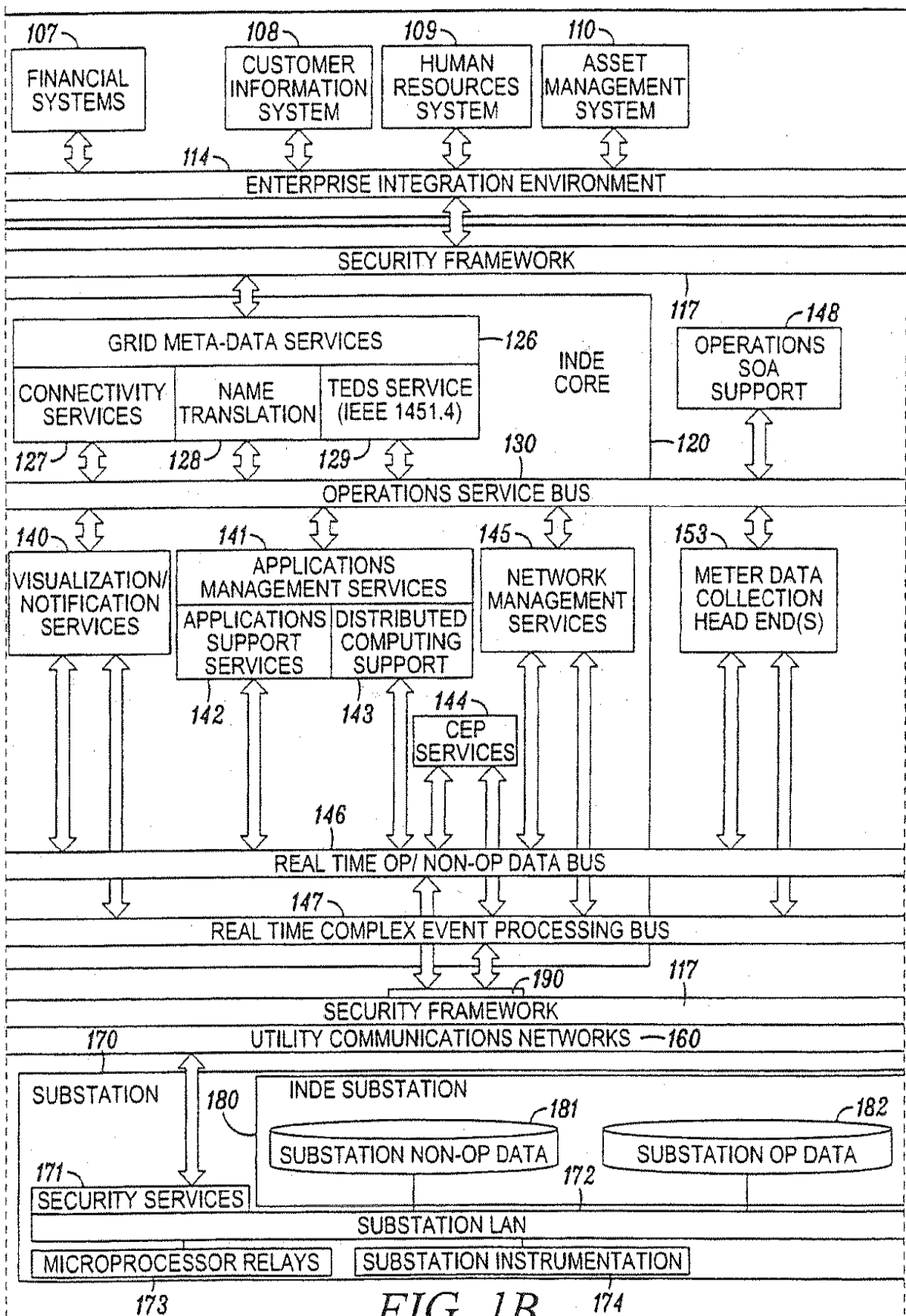


FIG. 1B

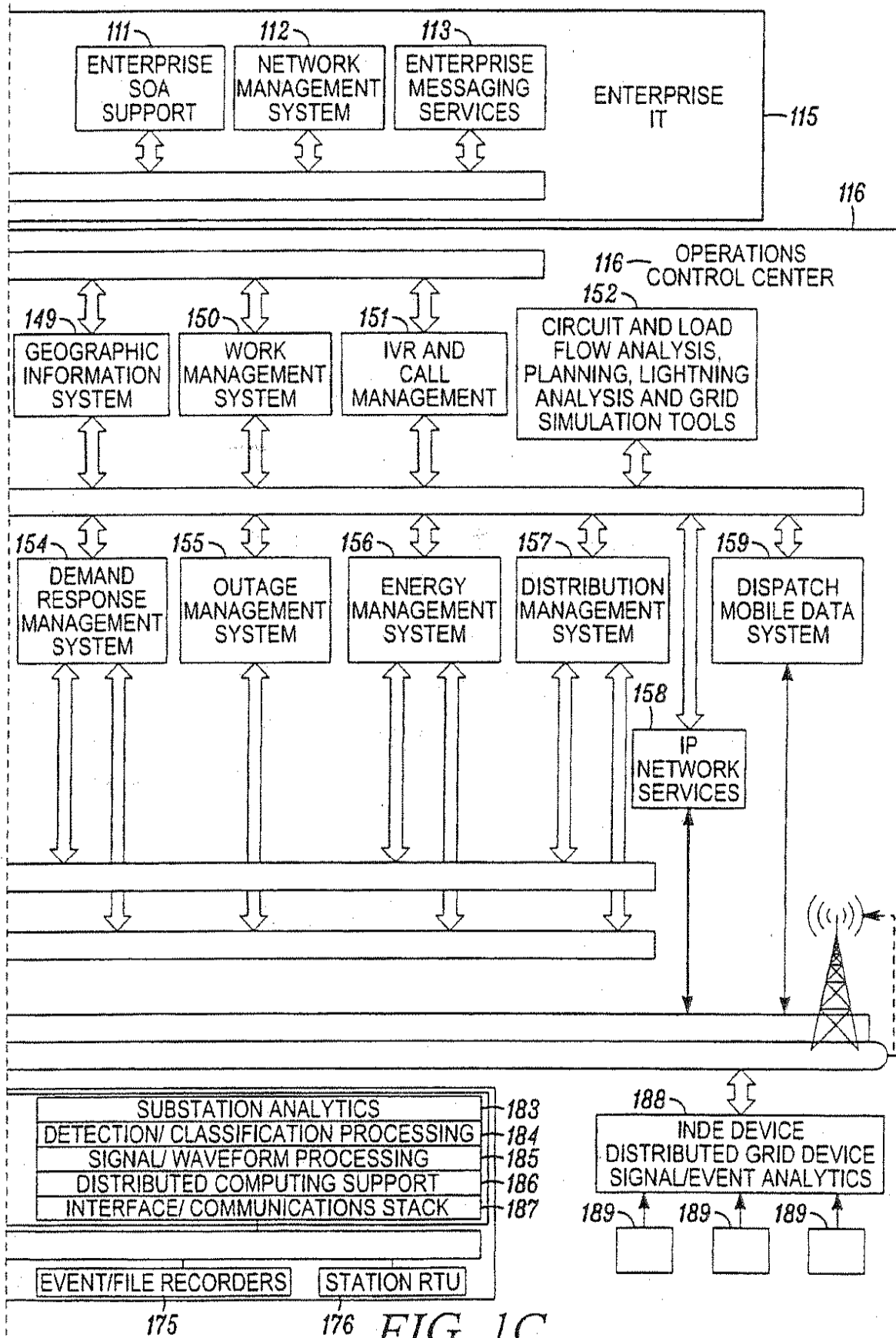


FIG. 1C

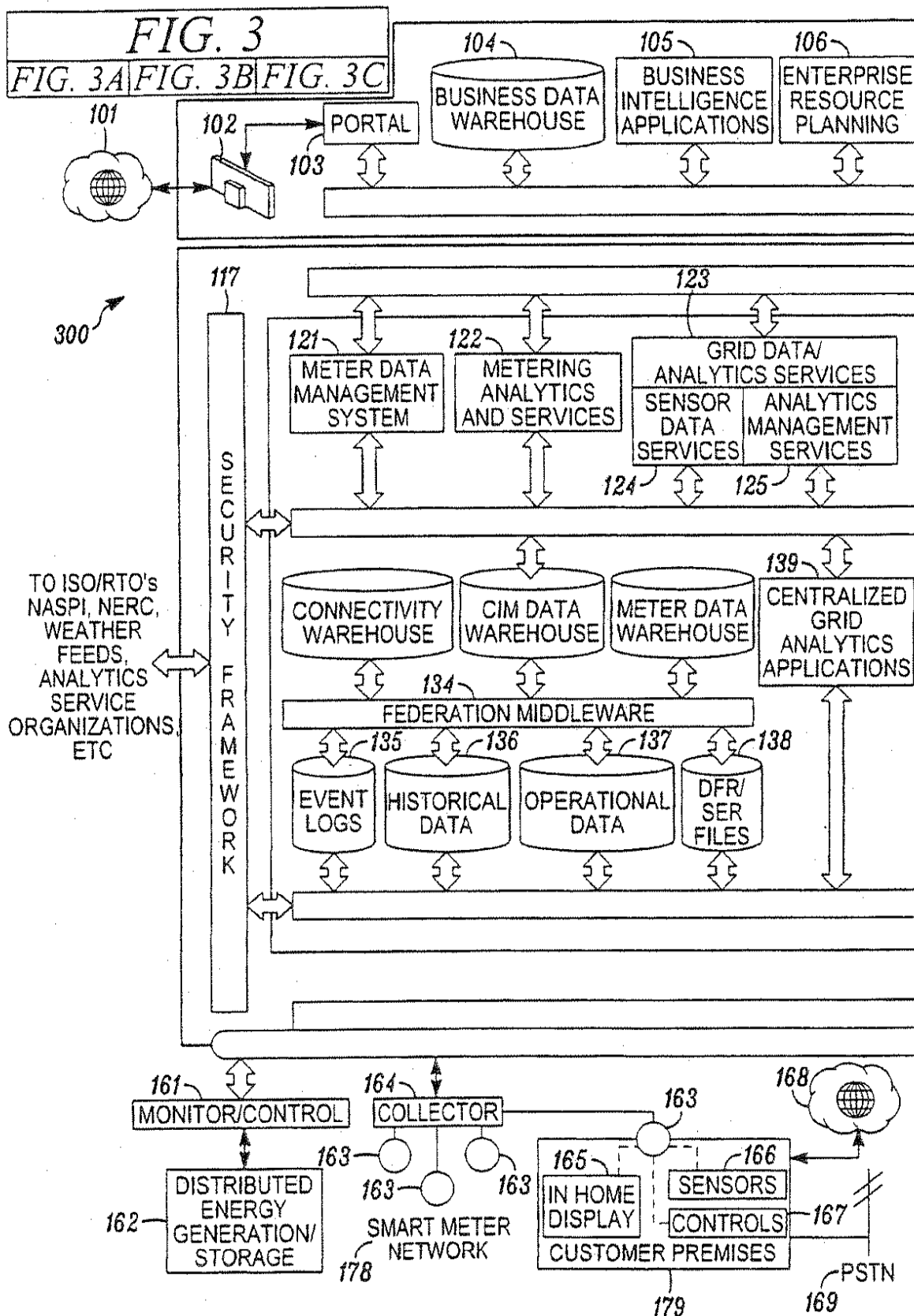
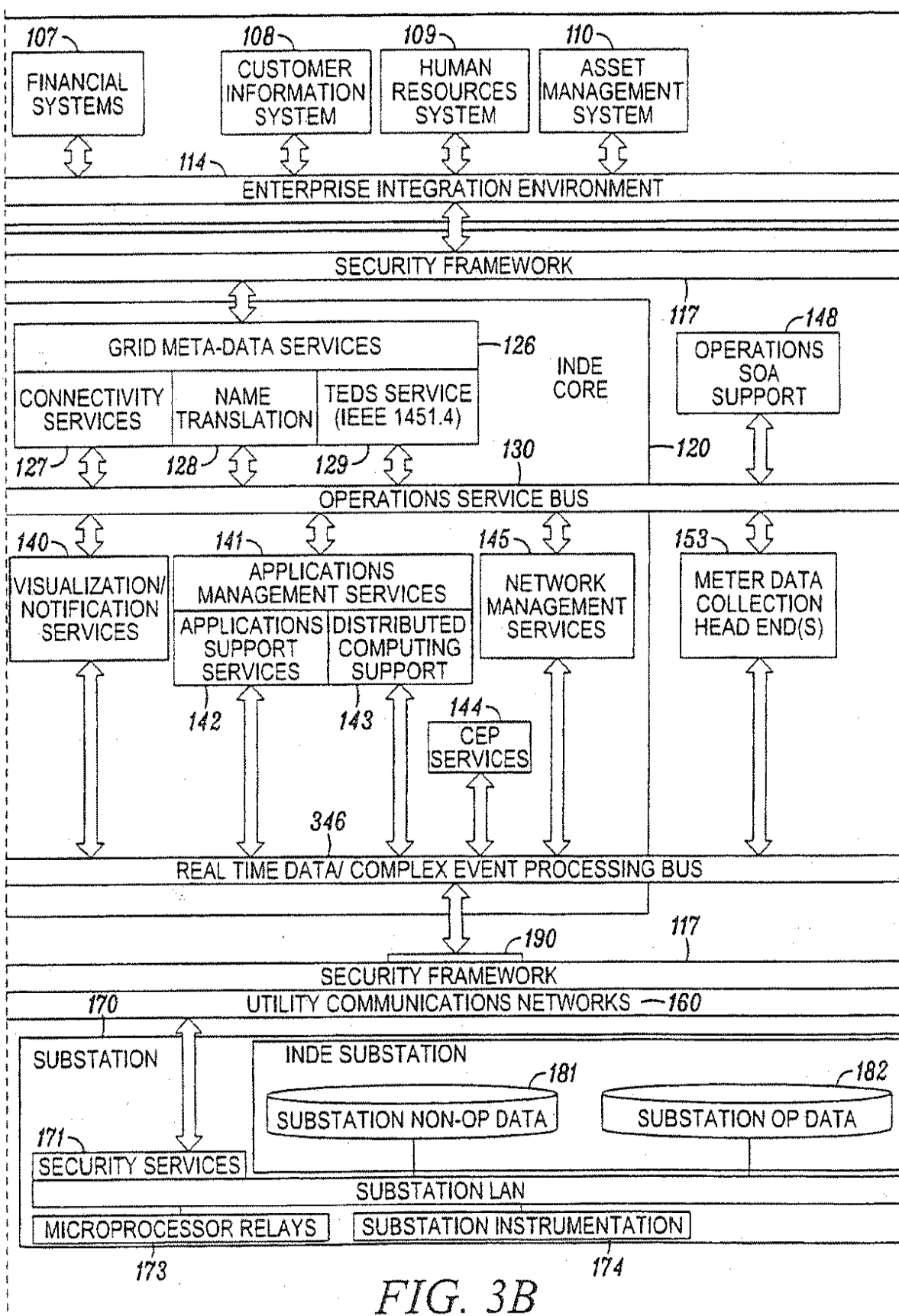


FIG. 3A



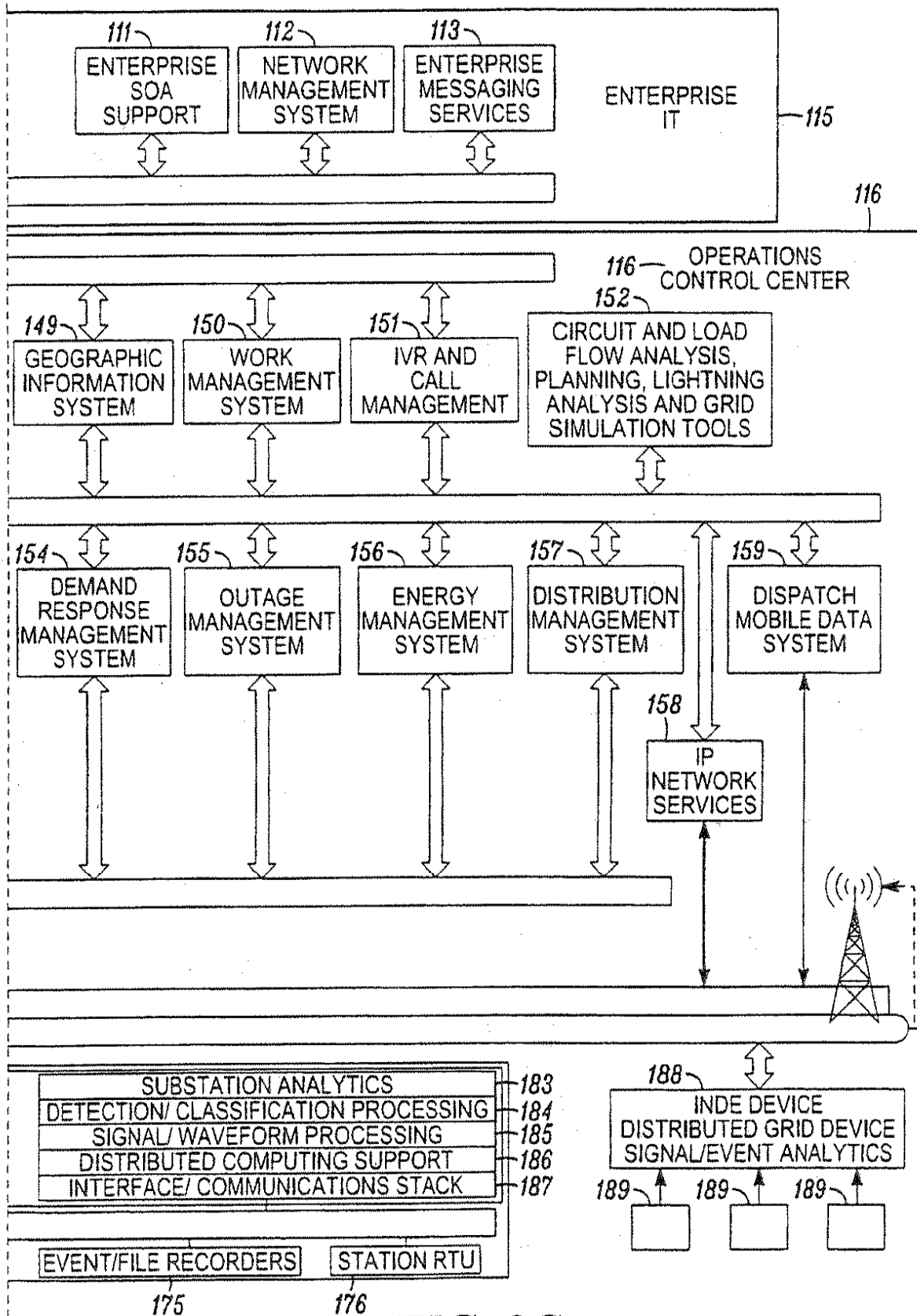


FIG. 3C

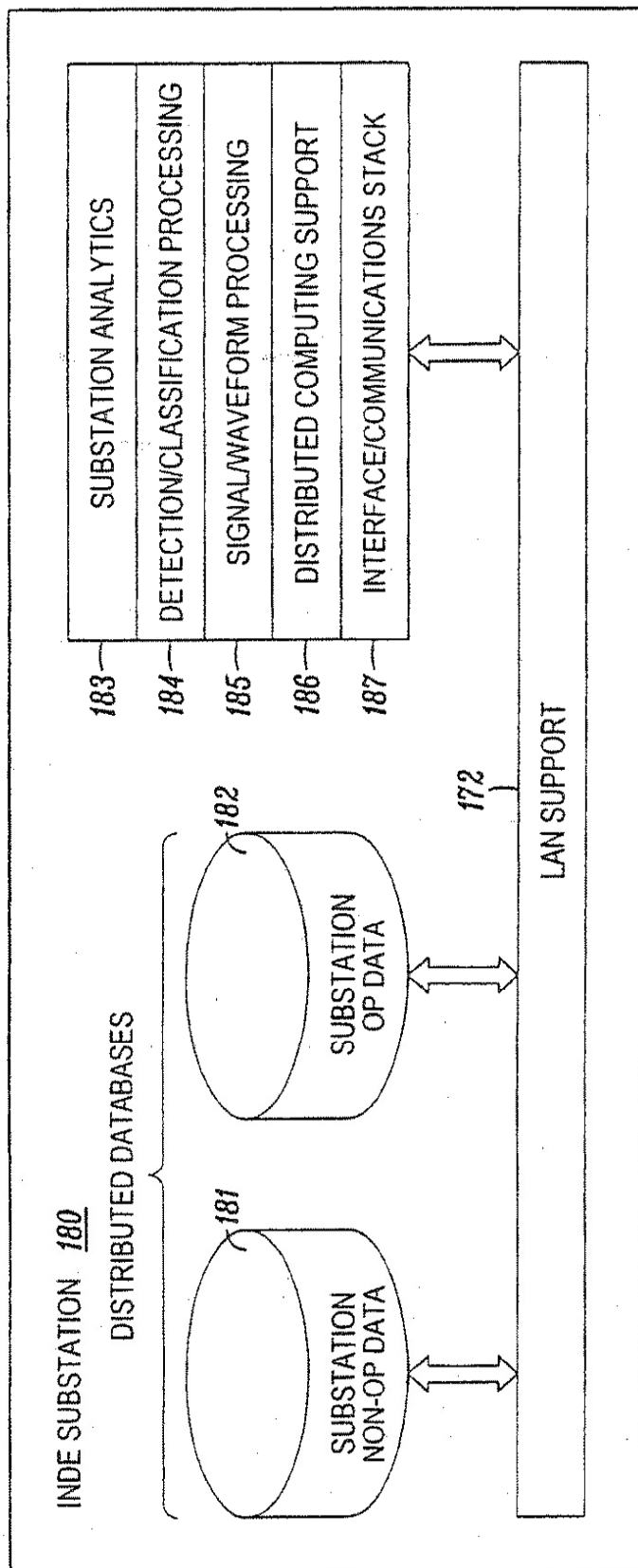


FIG. 4

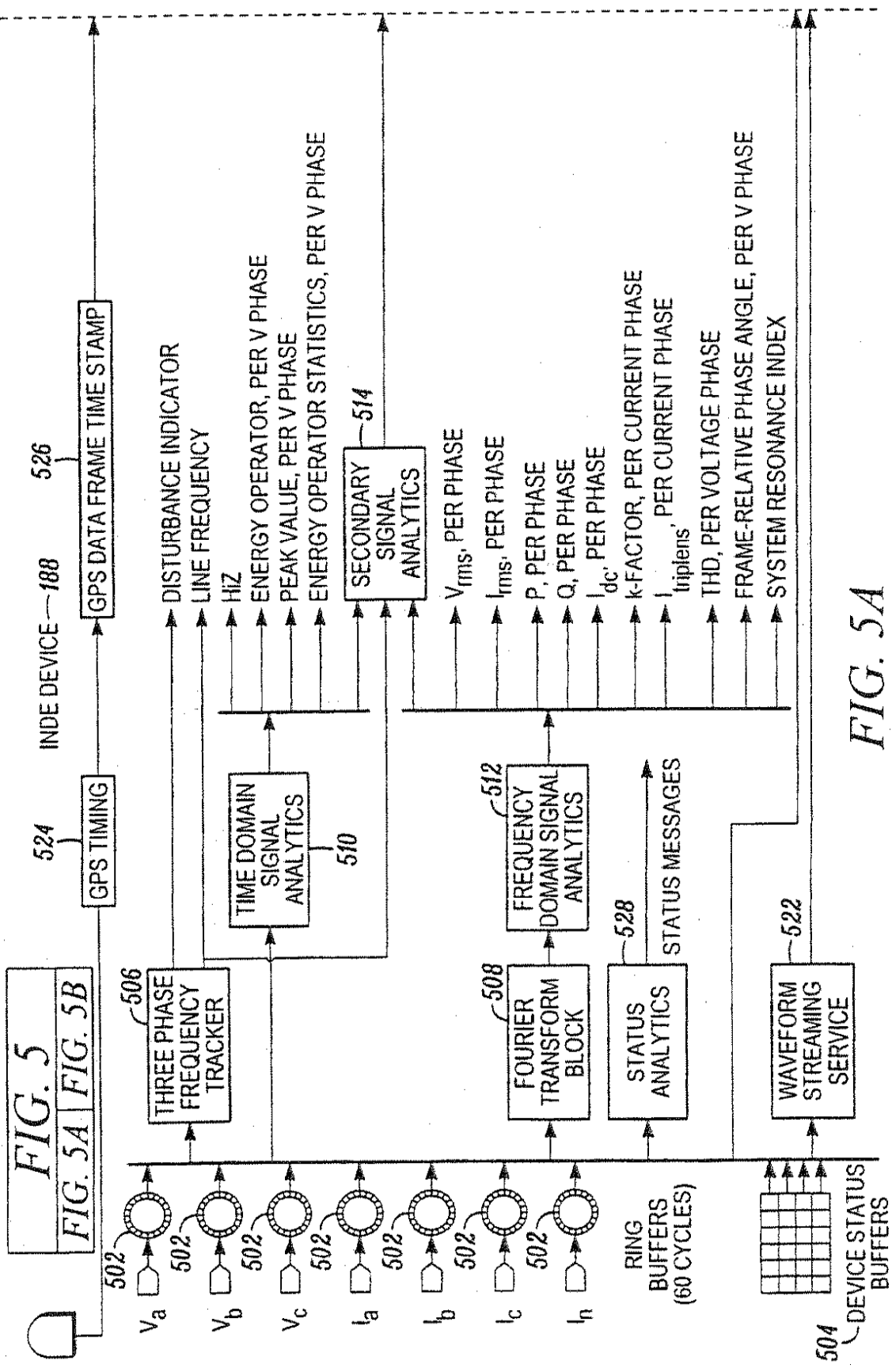


FIG. 5A

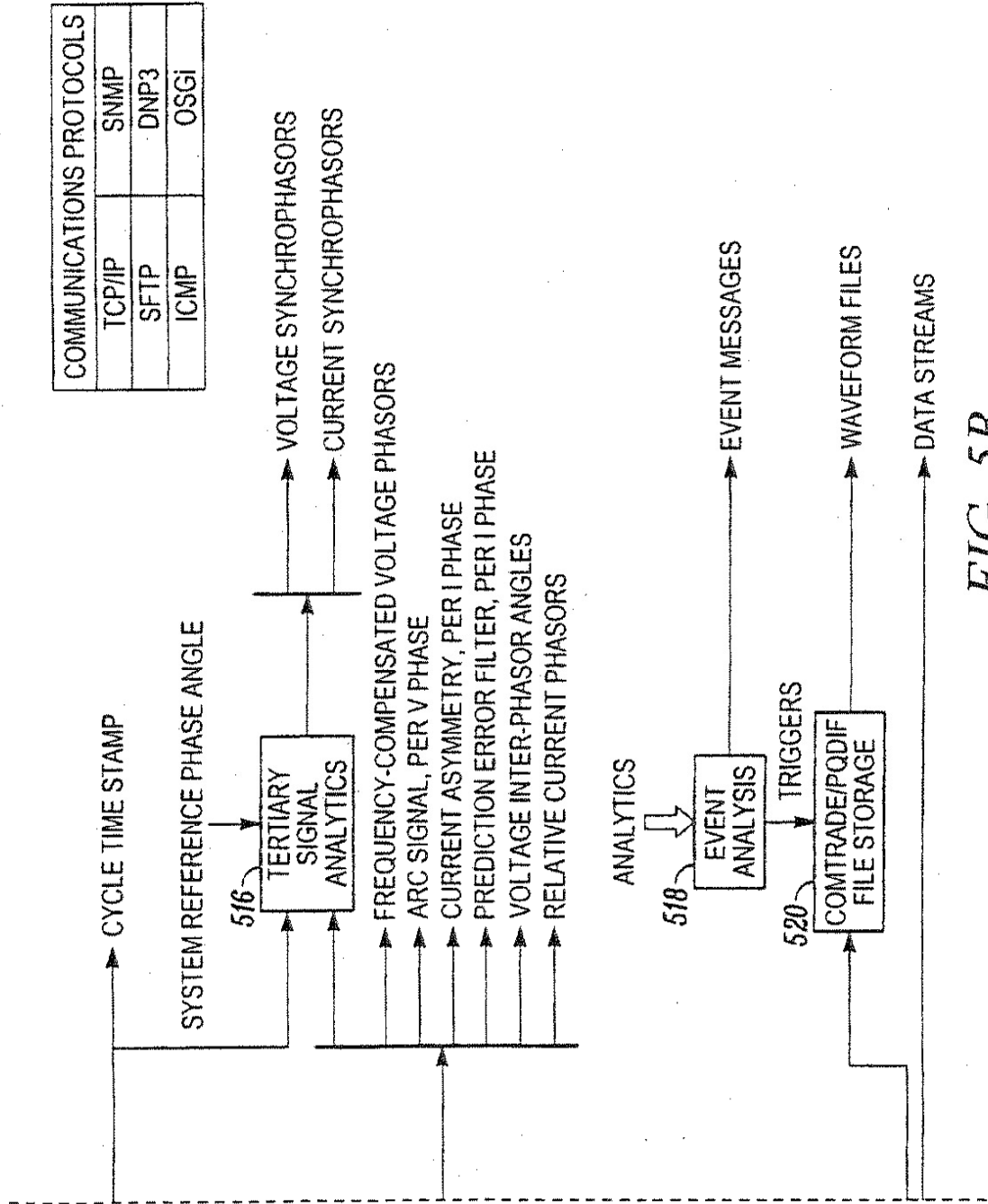
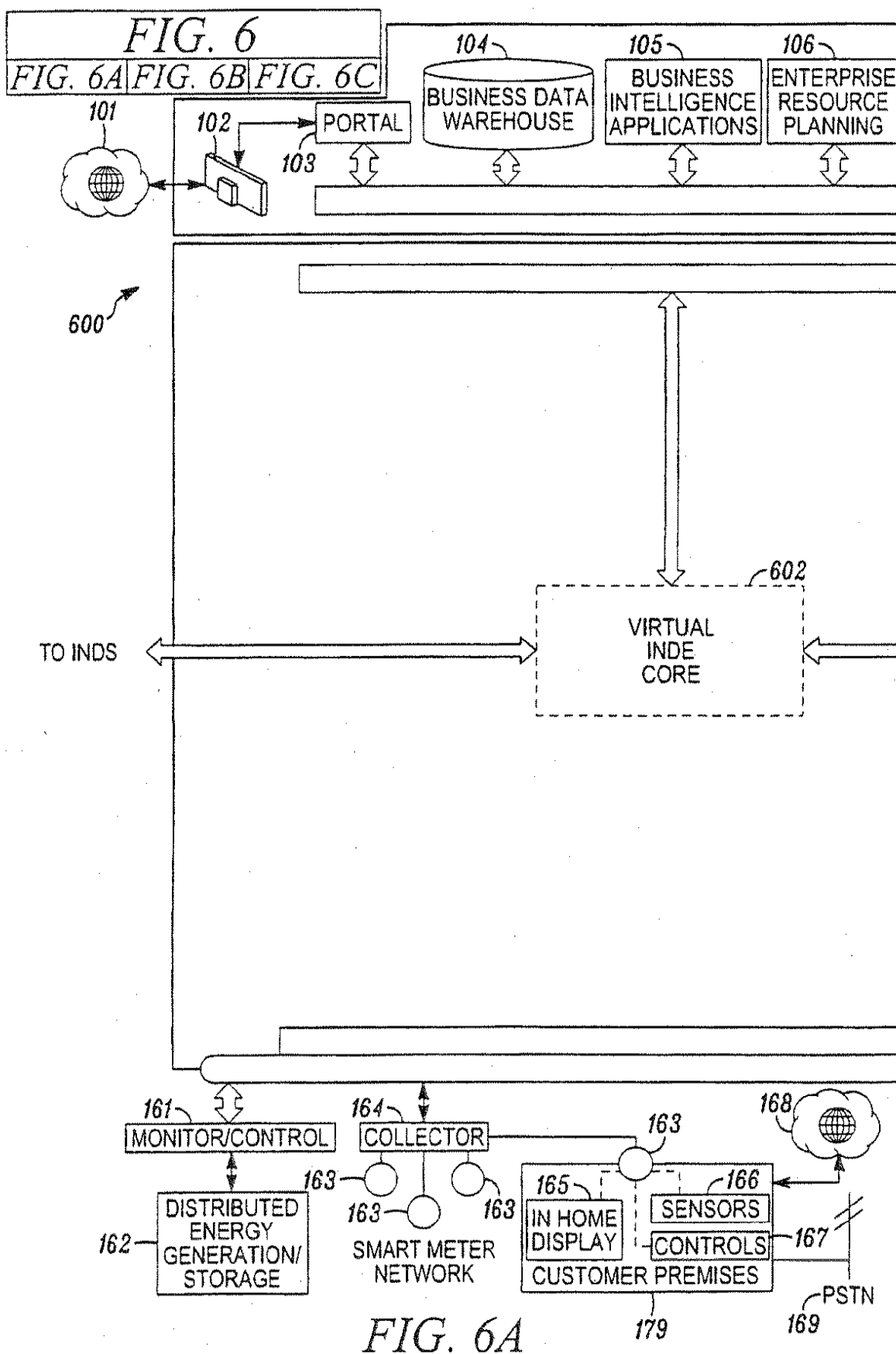


FIG. 5B



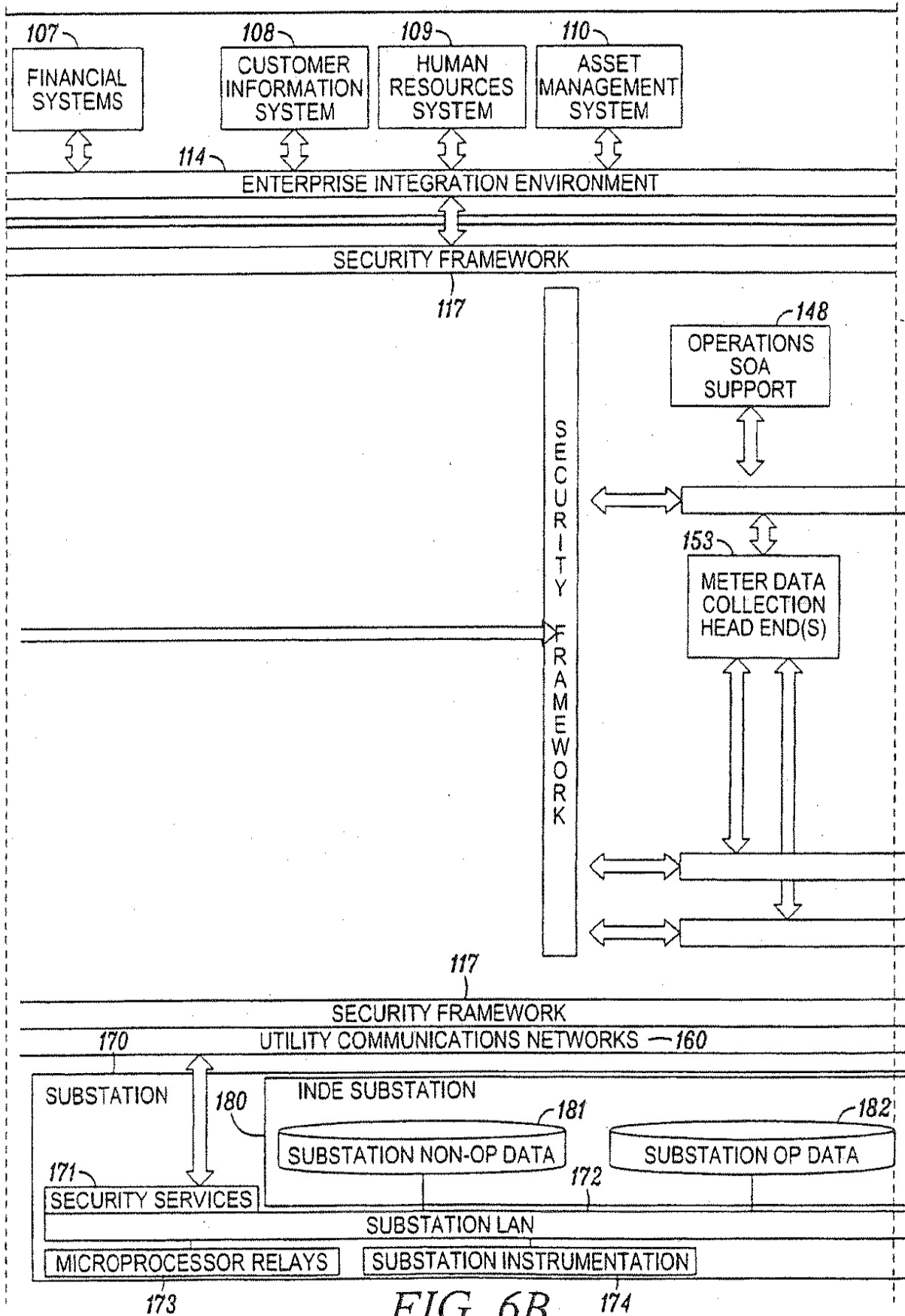


FIG. 6B

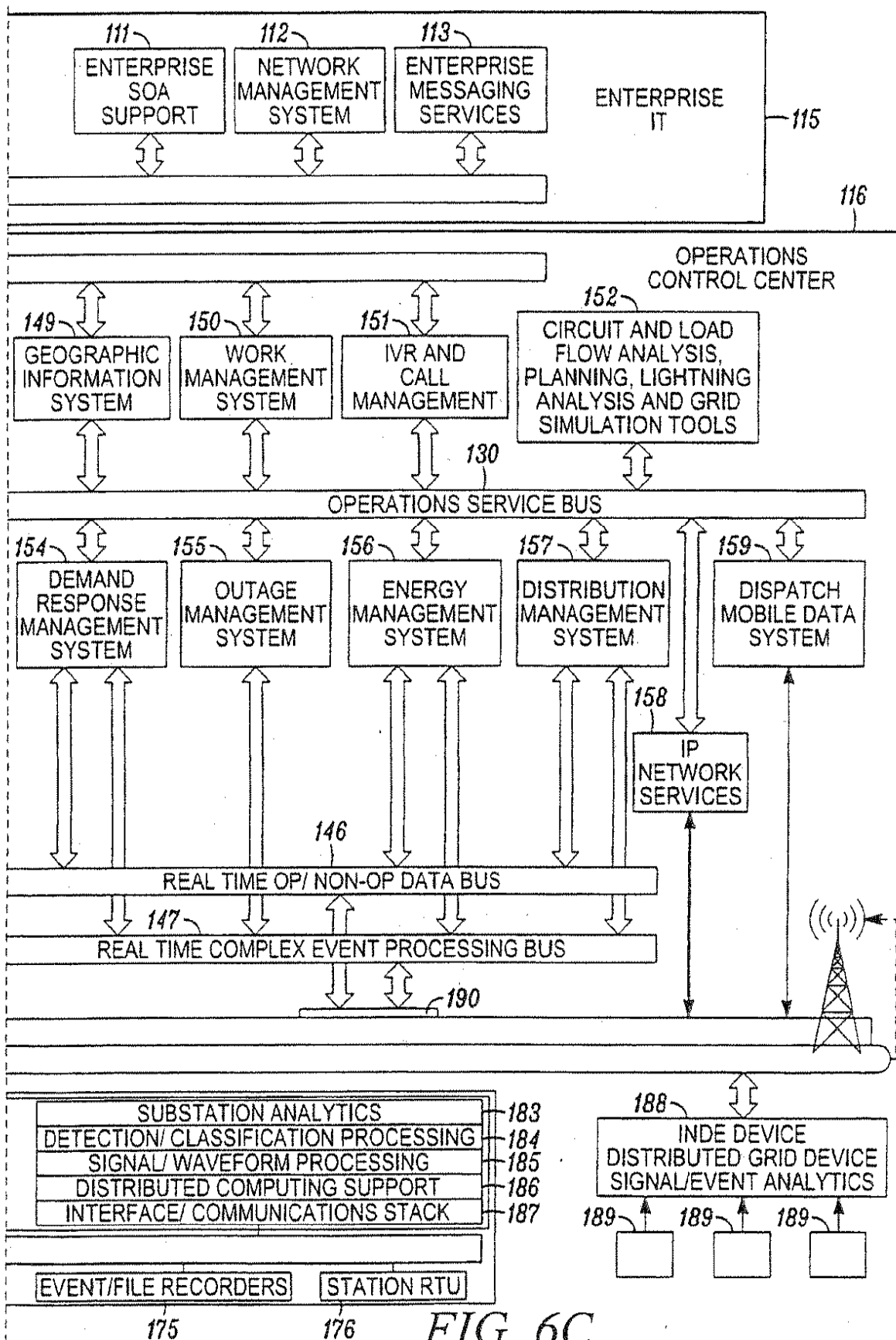


FIG. 6C

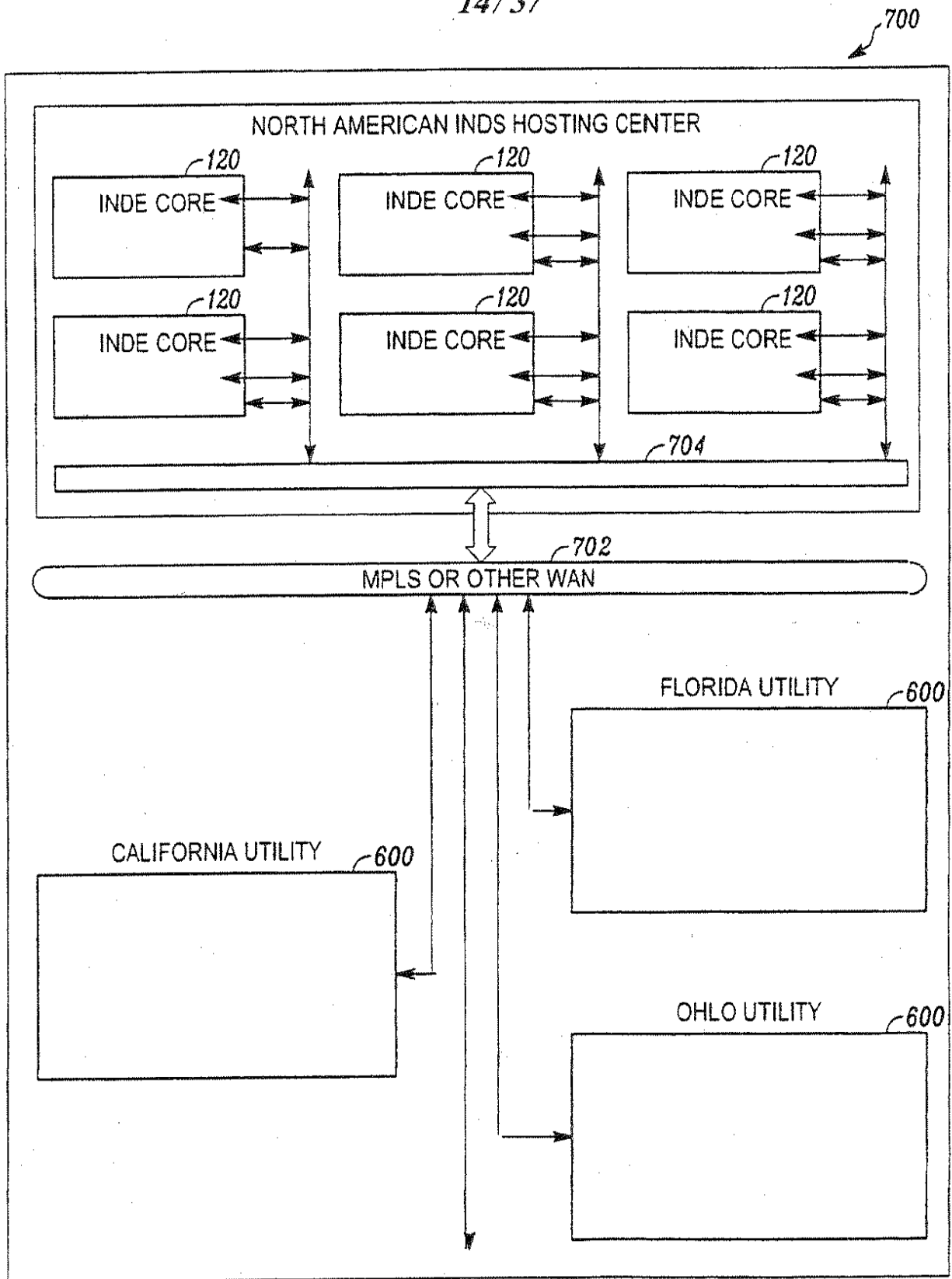


FIG. 7

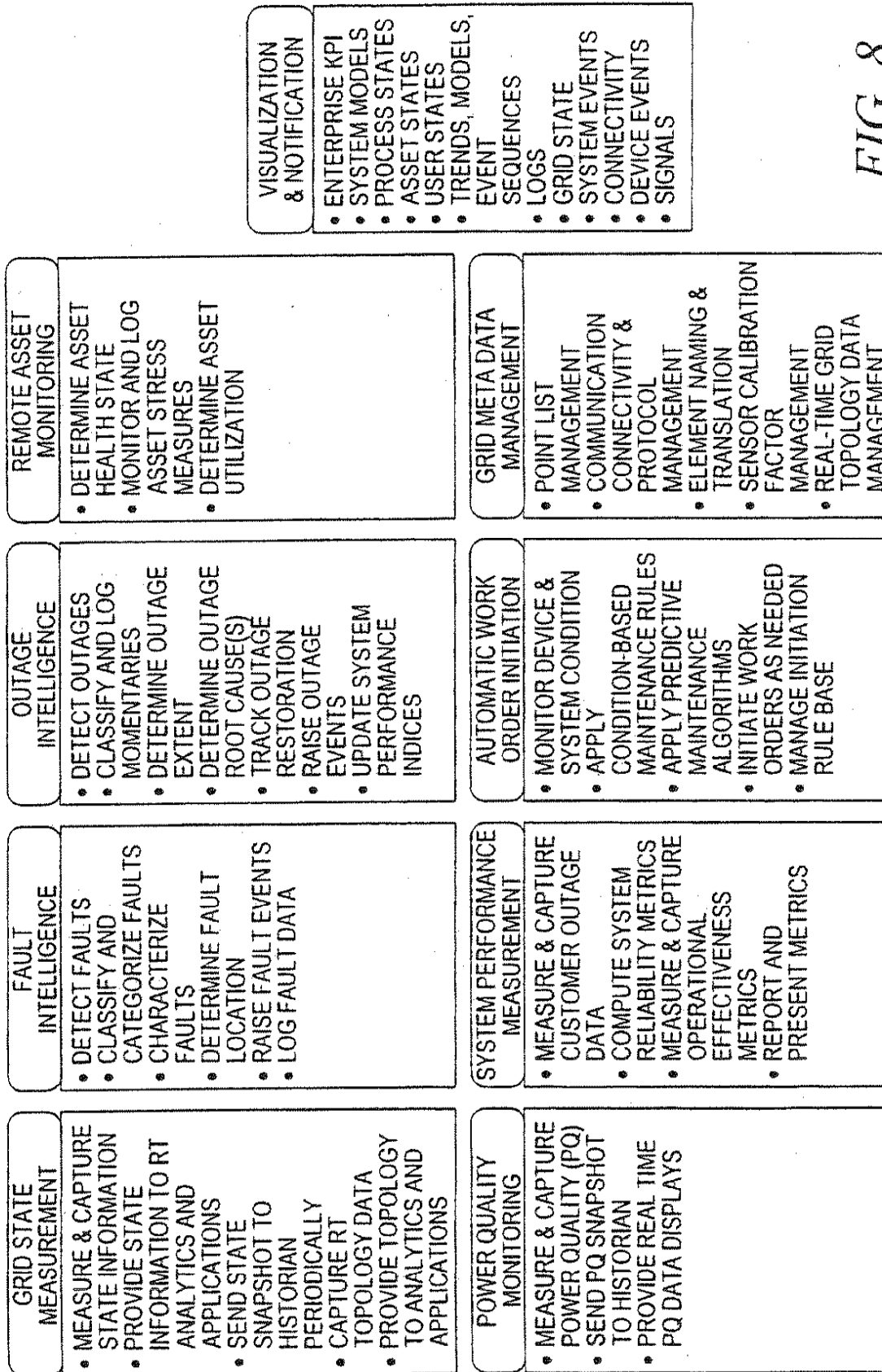


FIG. 8

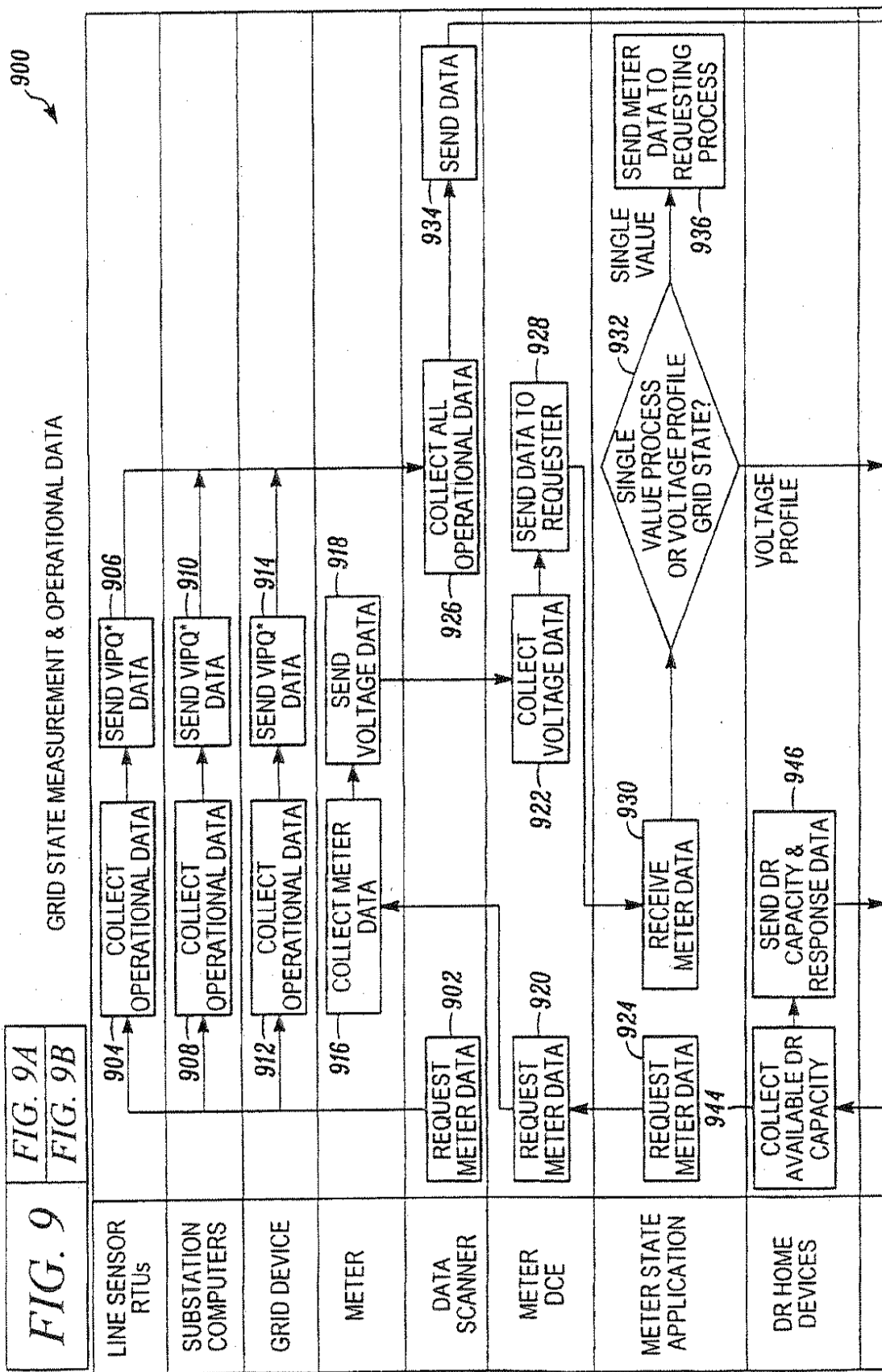
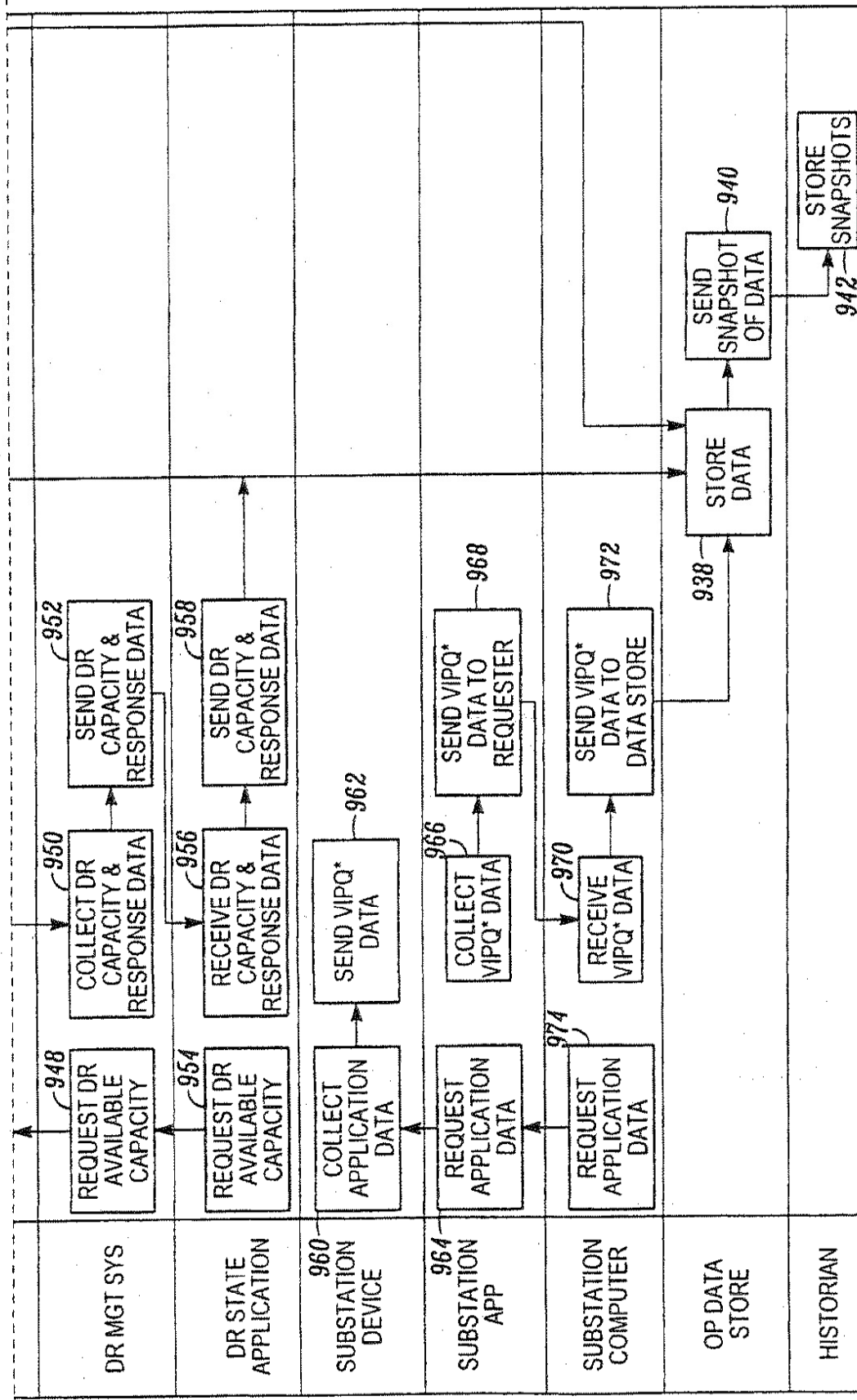


FIG. 9A



* V = VOLTAGE, I = CURRENT, P = REAL POWER, Q = REACTIVE POWER

FIG. 9B

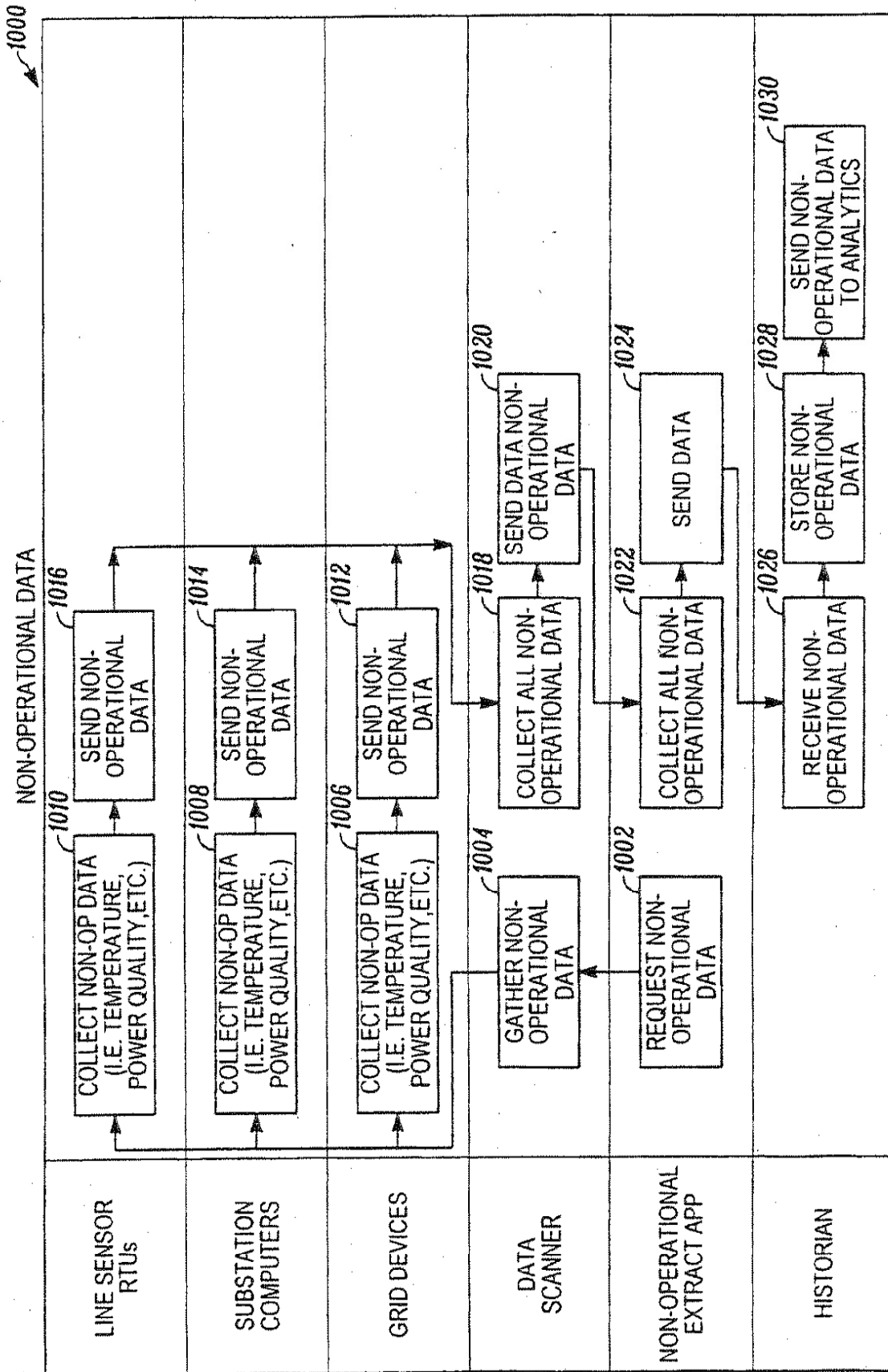


FIG. 10

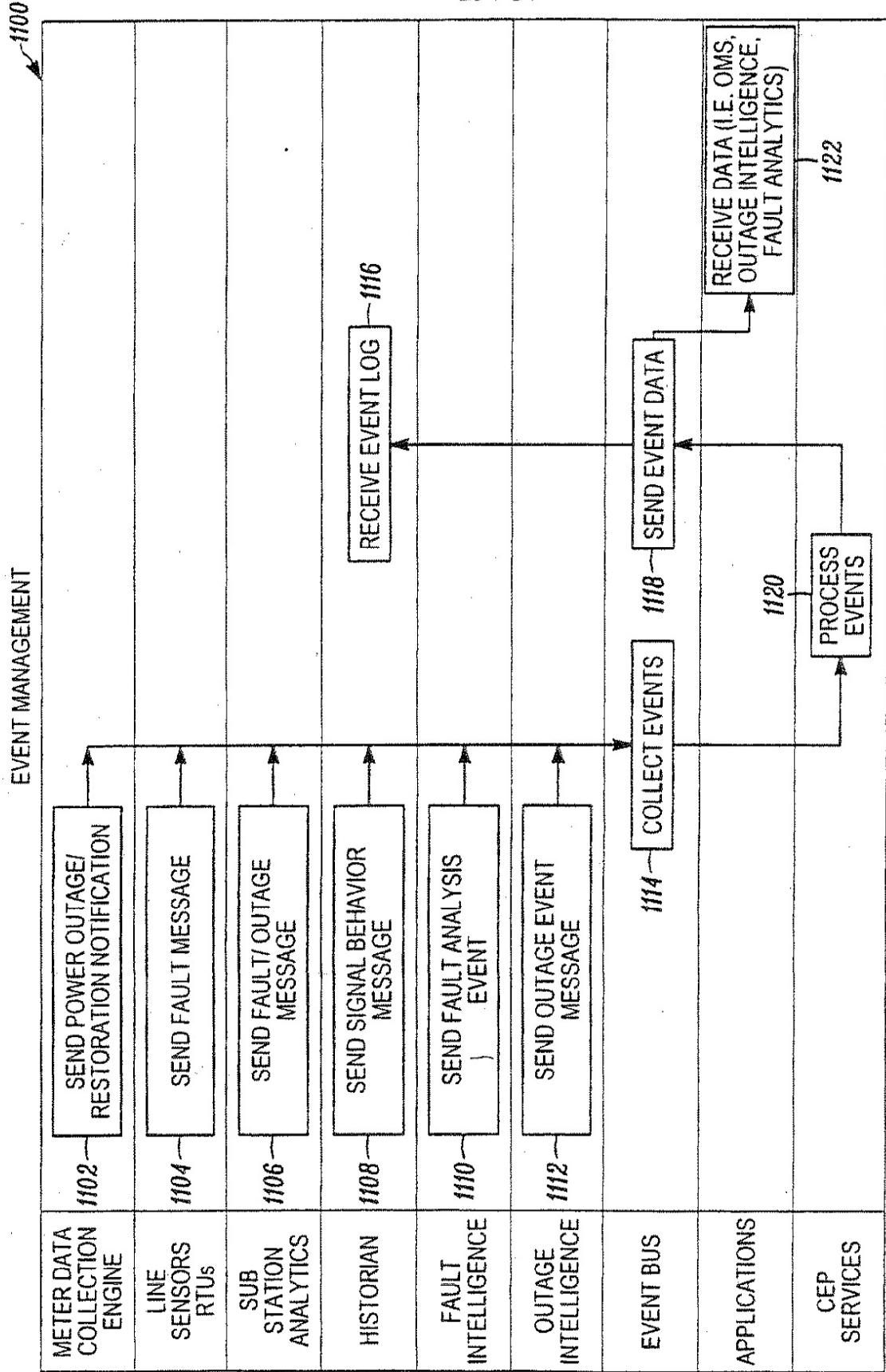


FIG. 11

FIG. 12A	FIG. 12B	FIG. 12C
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DR SIGNALING

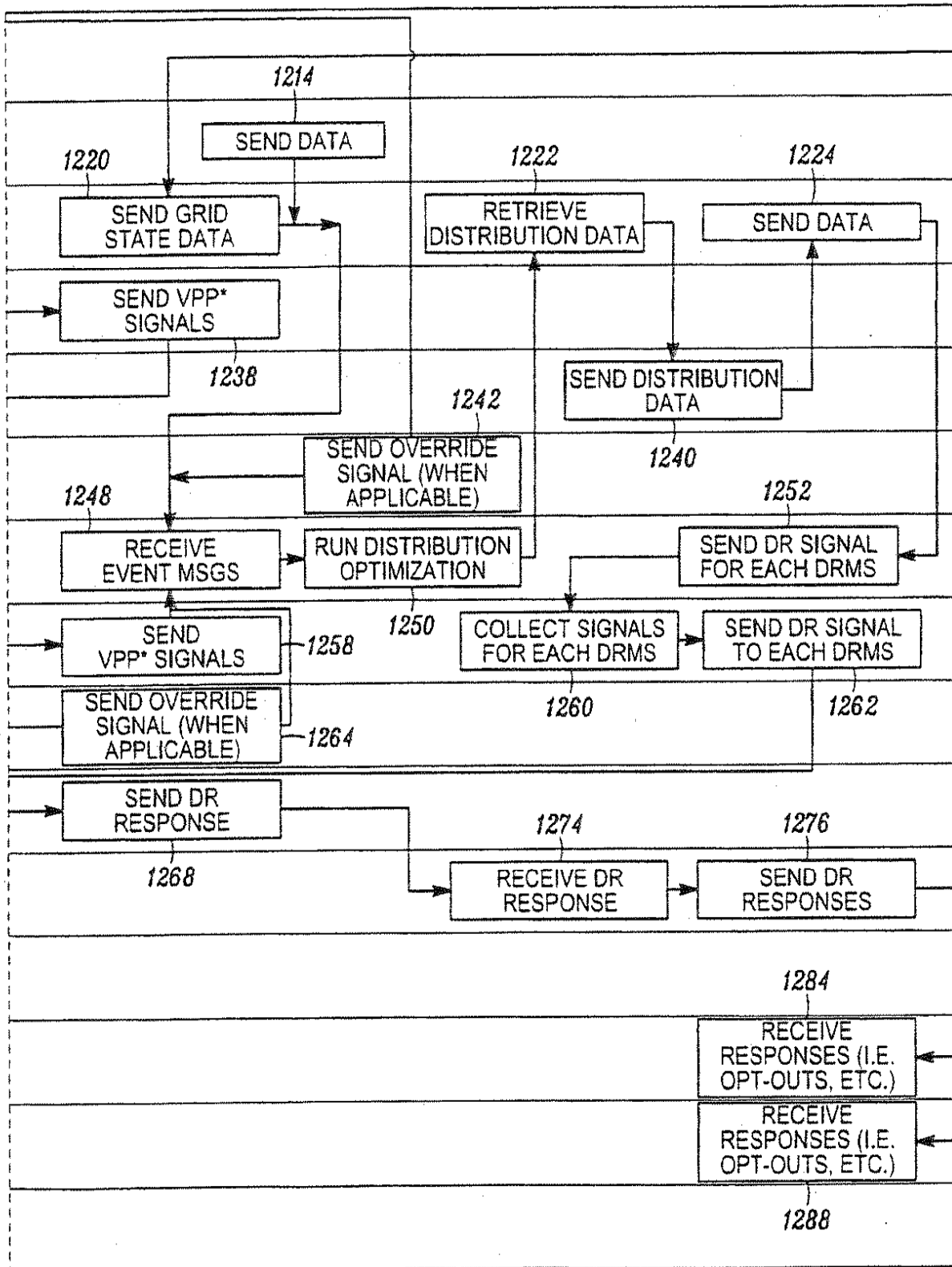


FIG. 12B

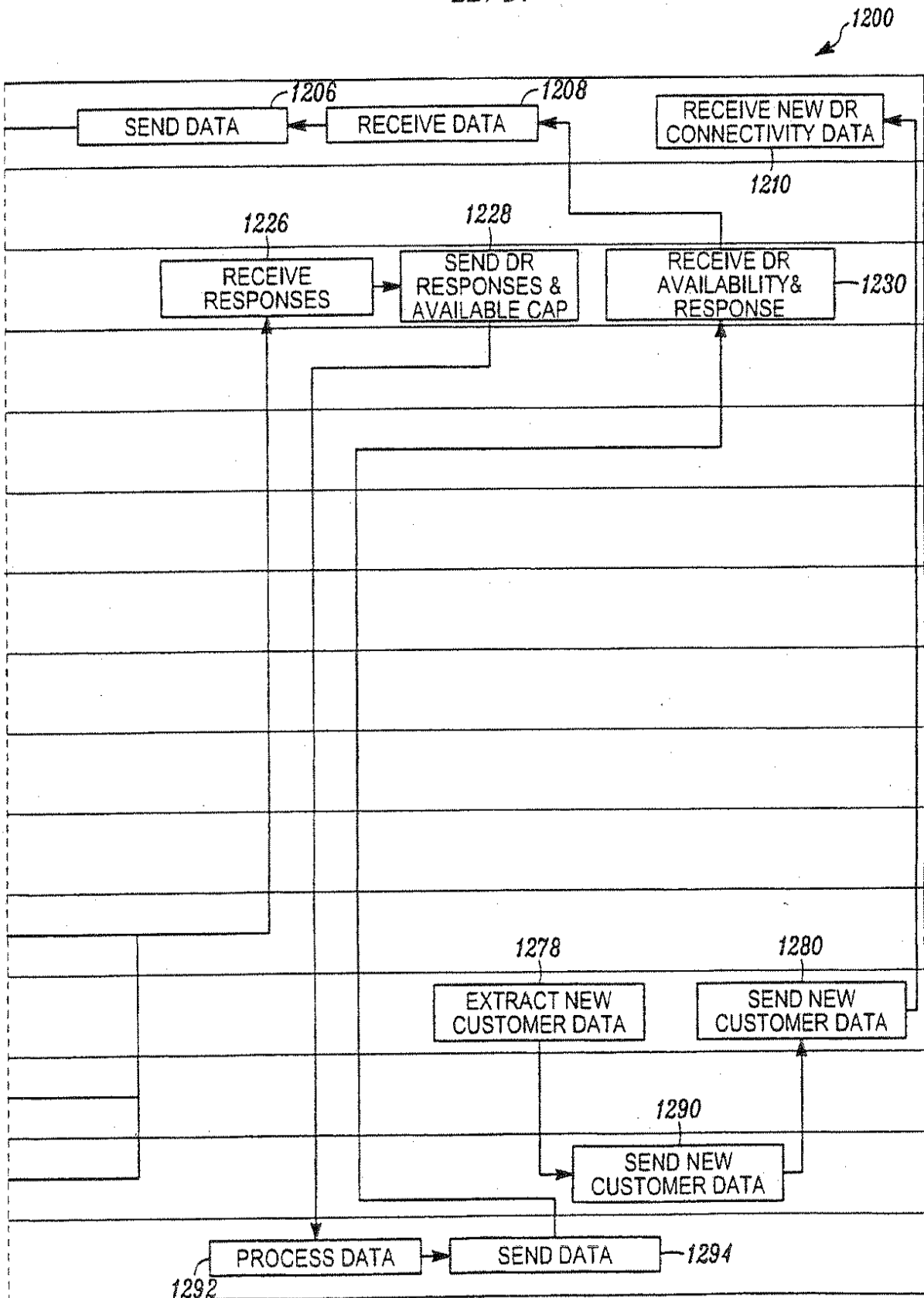


FIG. 12C

FIG. 13
FIG. 13A **FIG. 13B**

OUTAGE INTELLIGENCE

1300

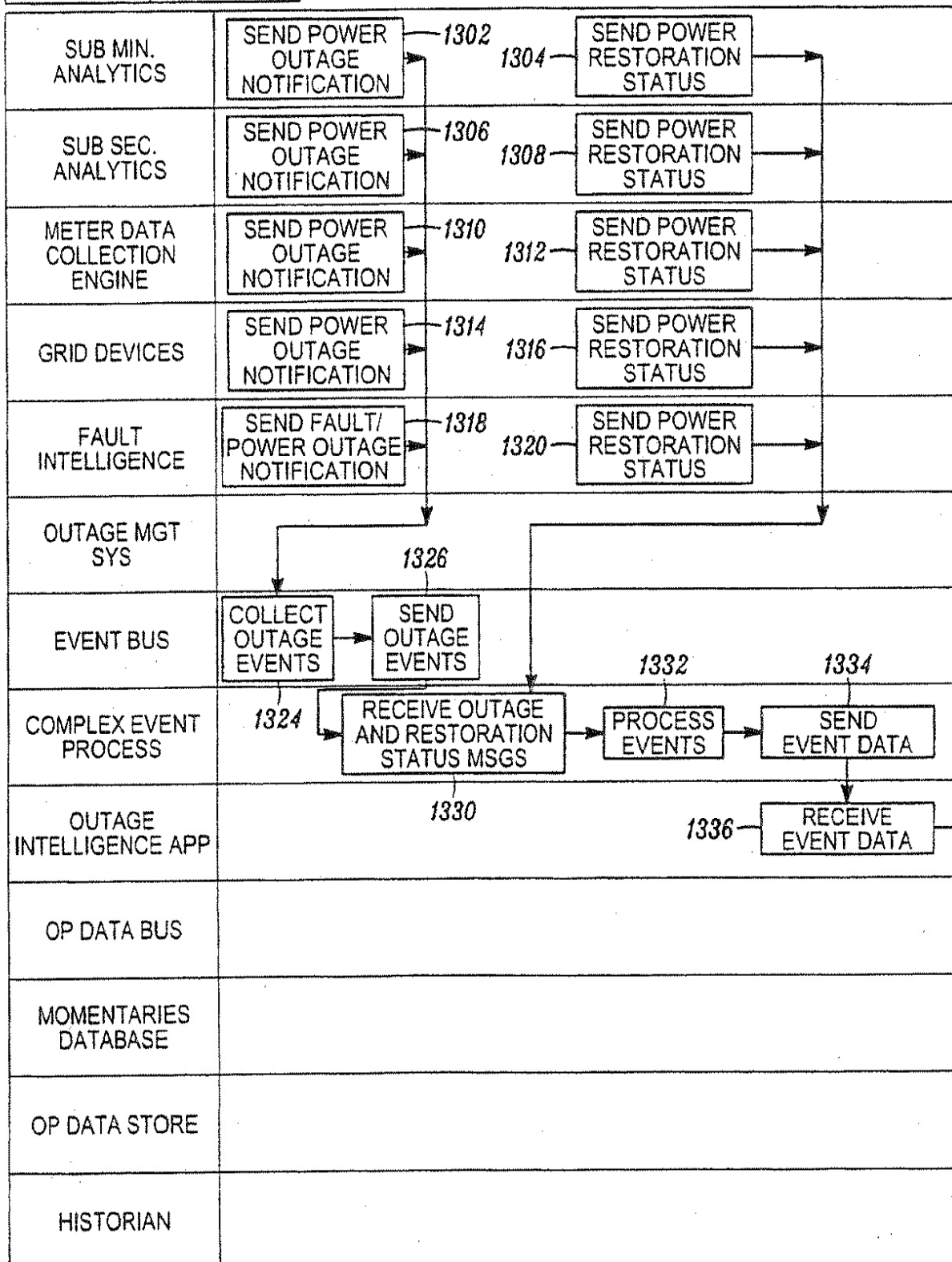


FIG. 13A

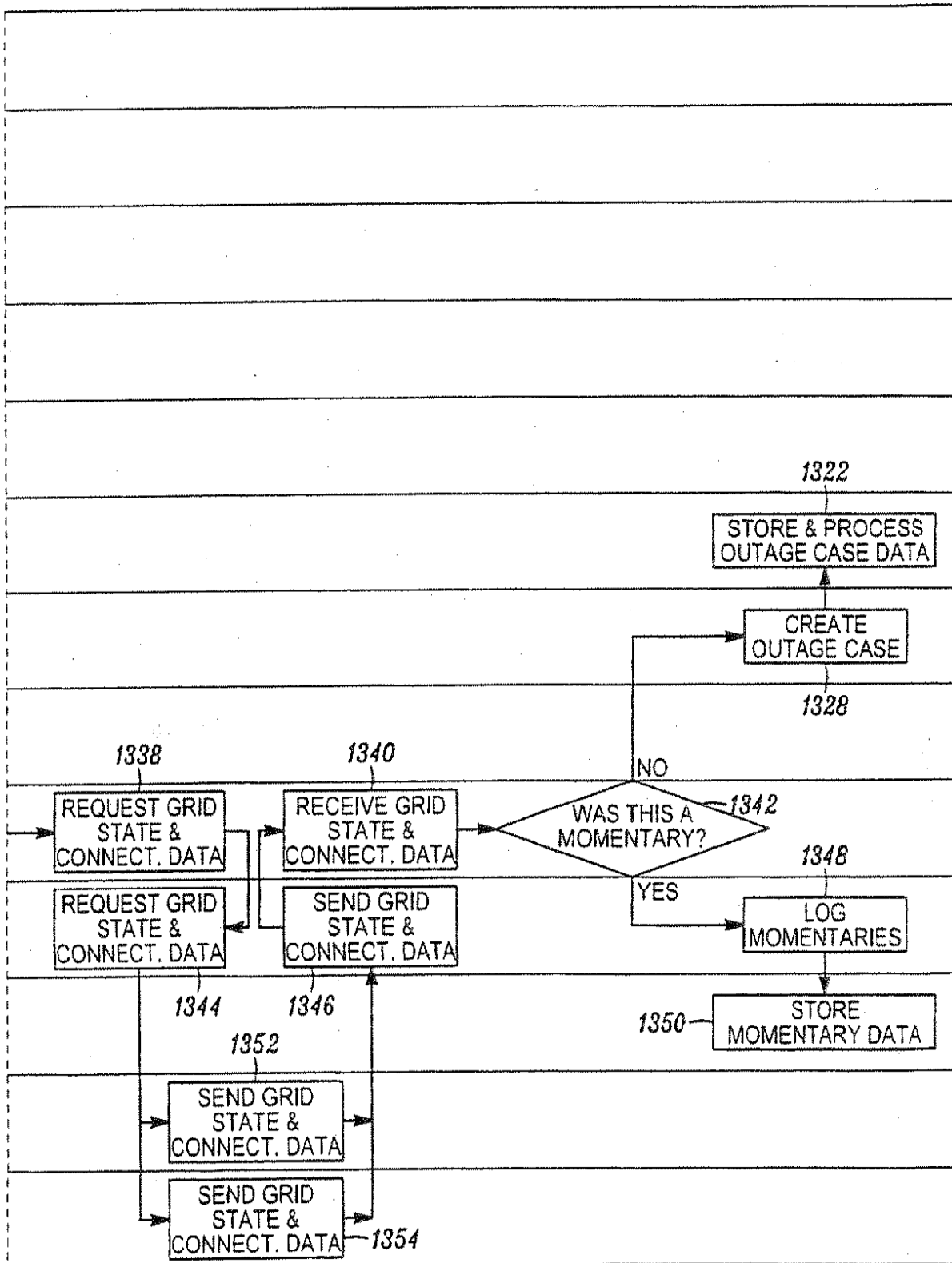
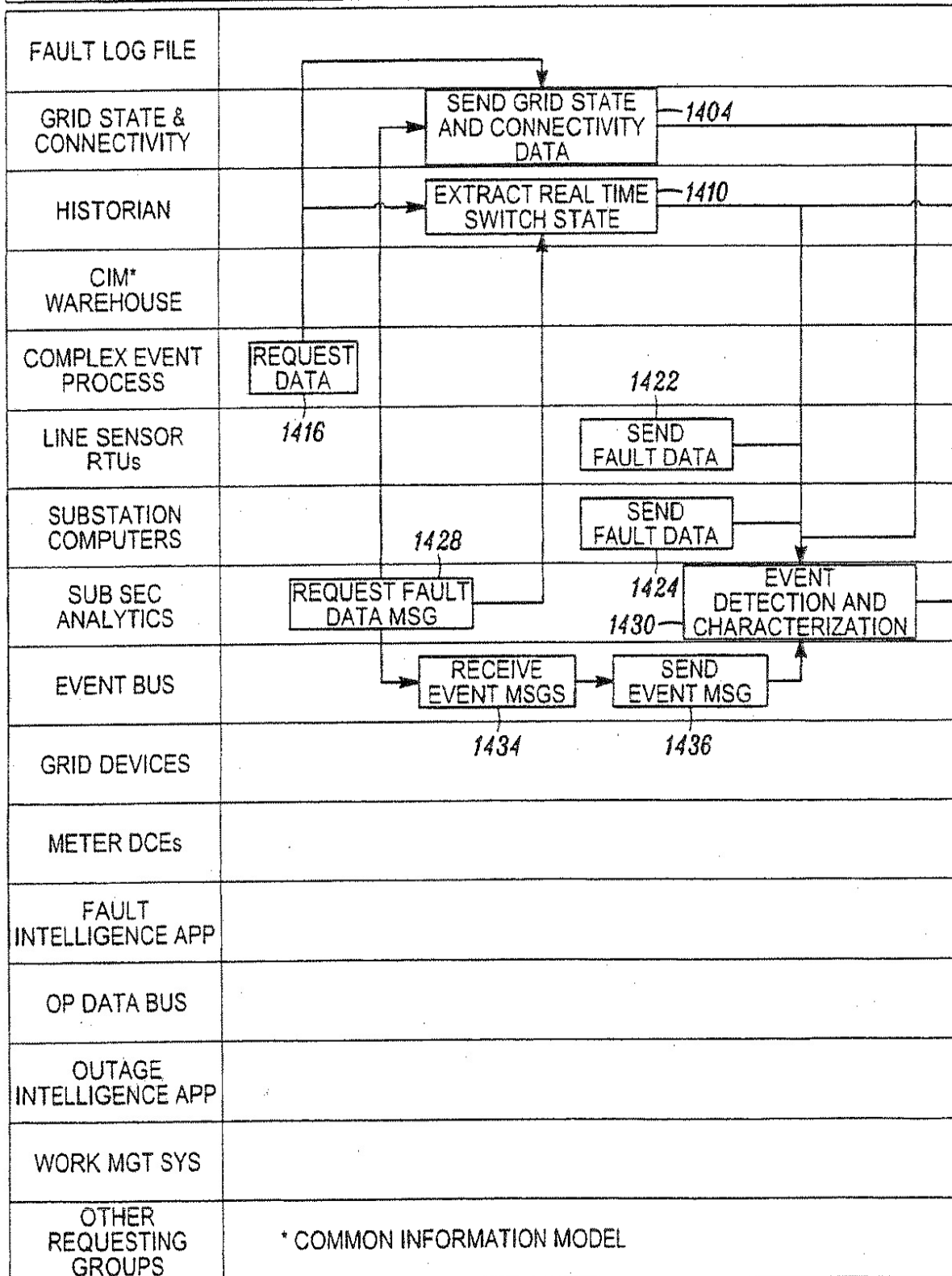


FIG. 13B

FIG. 14**FIG. 14A** | **FIG. 14B** | **FIG. 14C****FIG. 14A**

FAULT INTELLIGENCE

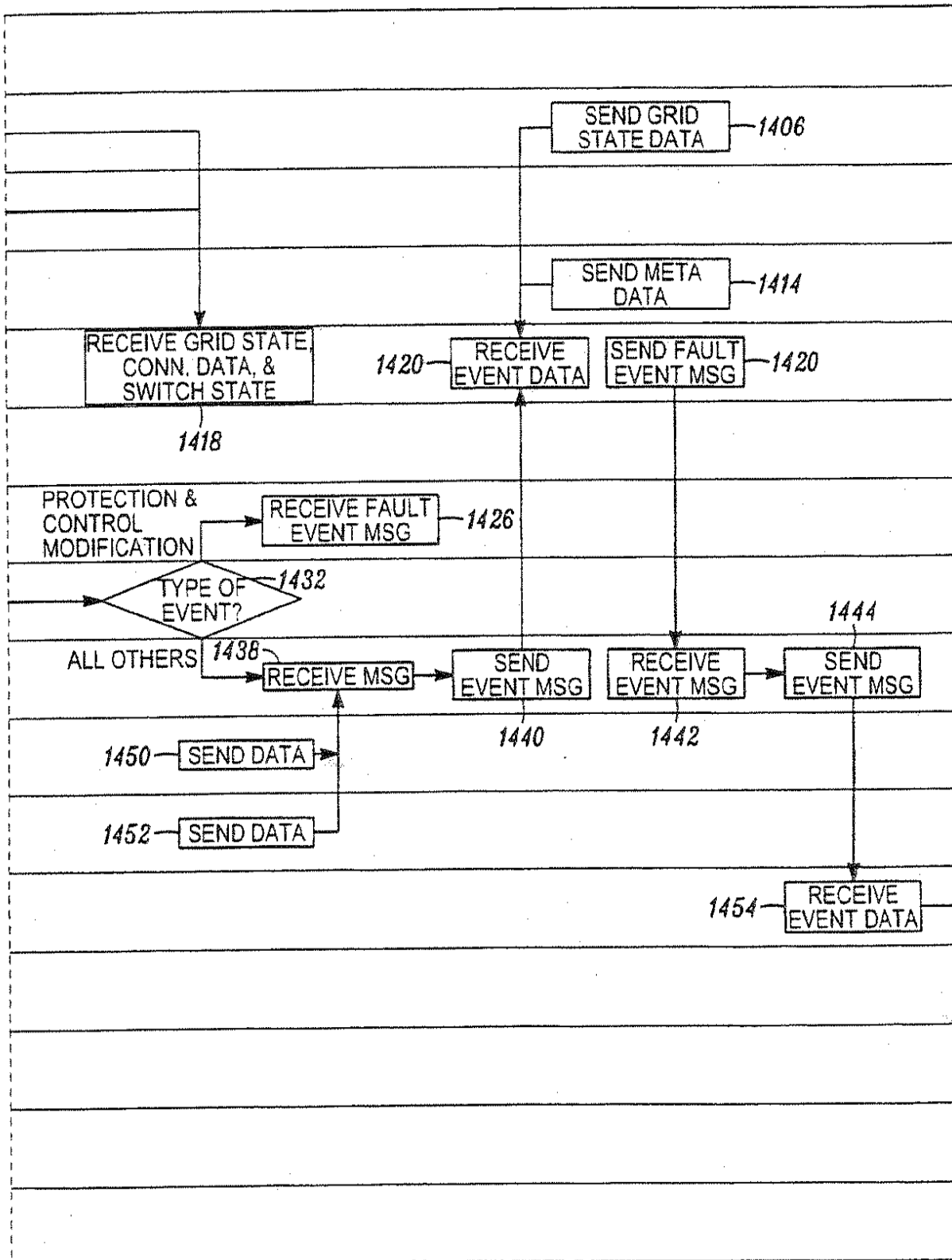


FIG. 14B

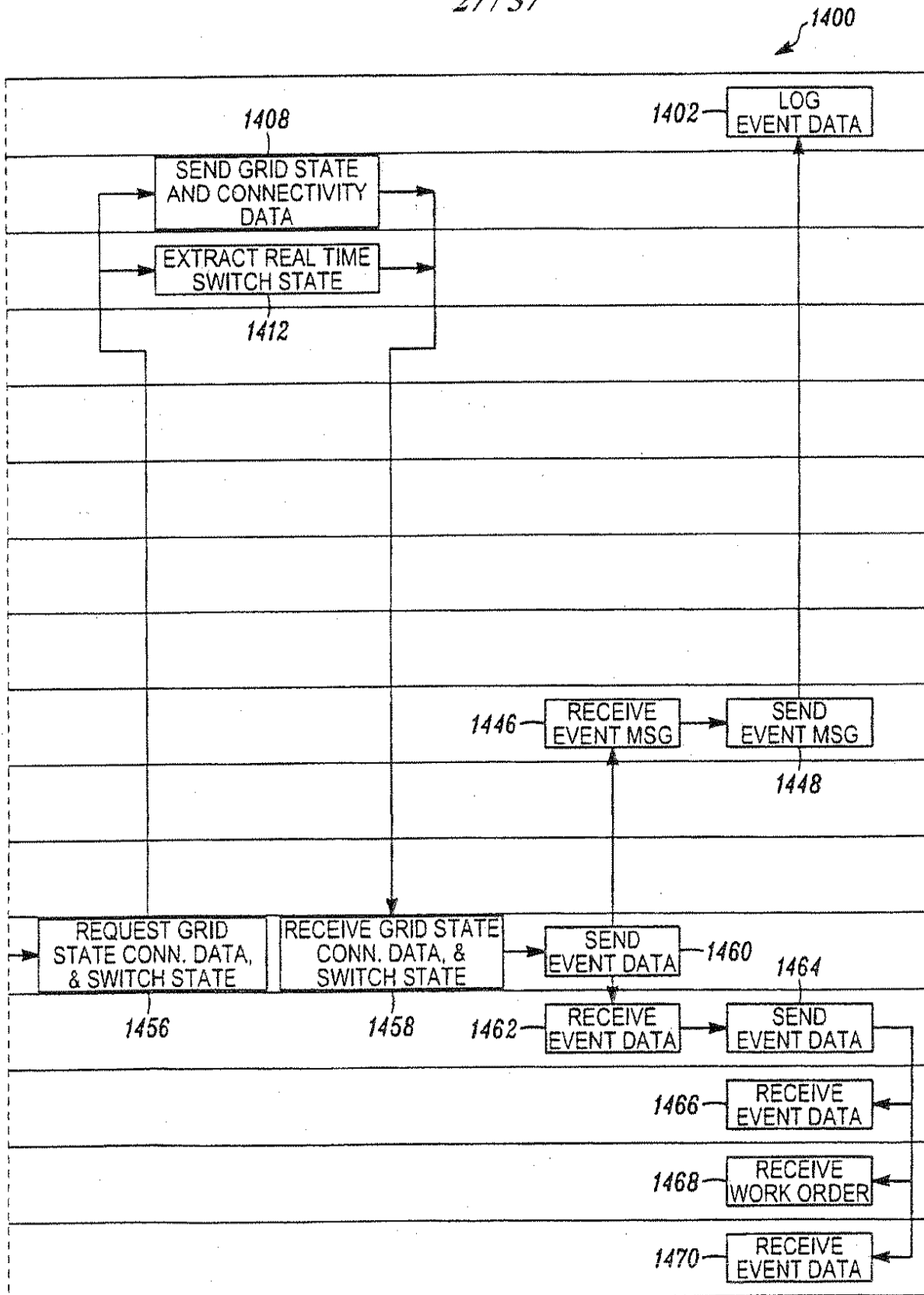
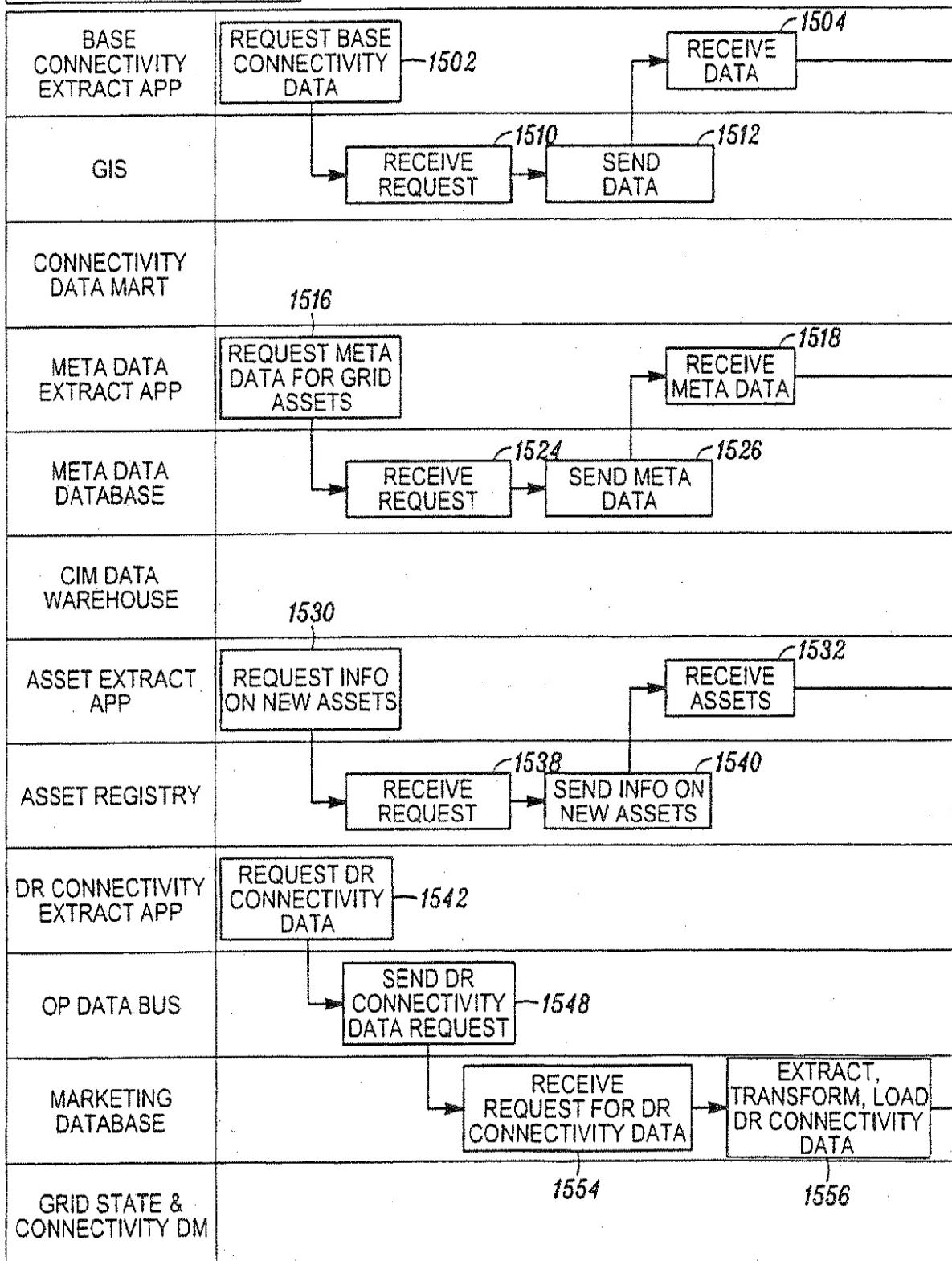


FIG. 14C

FIG. 15**FIG. 15A | FIG. 15B****FIG. 15A**

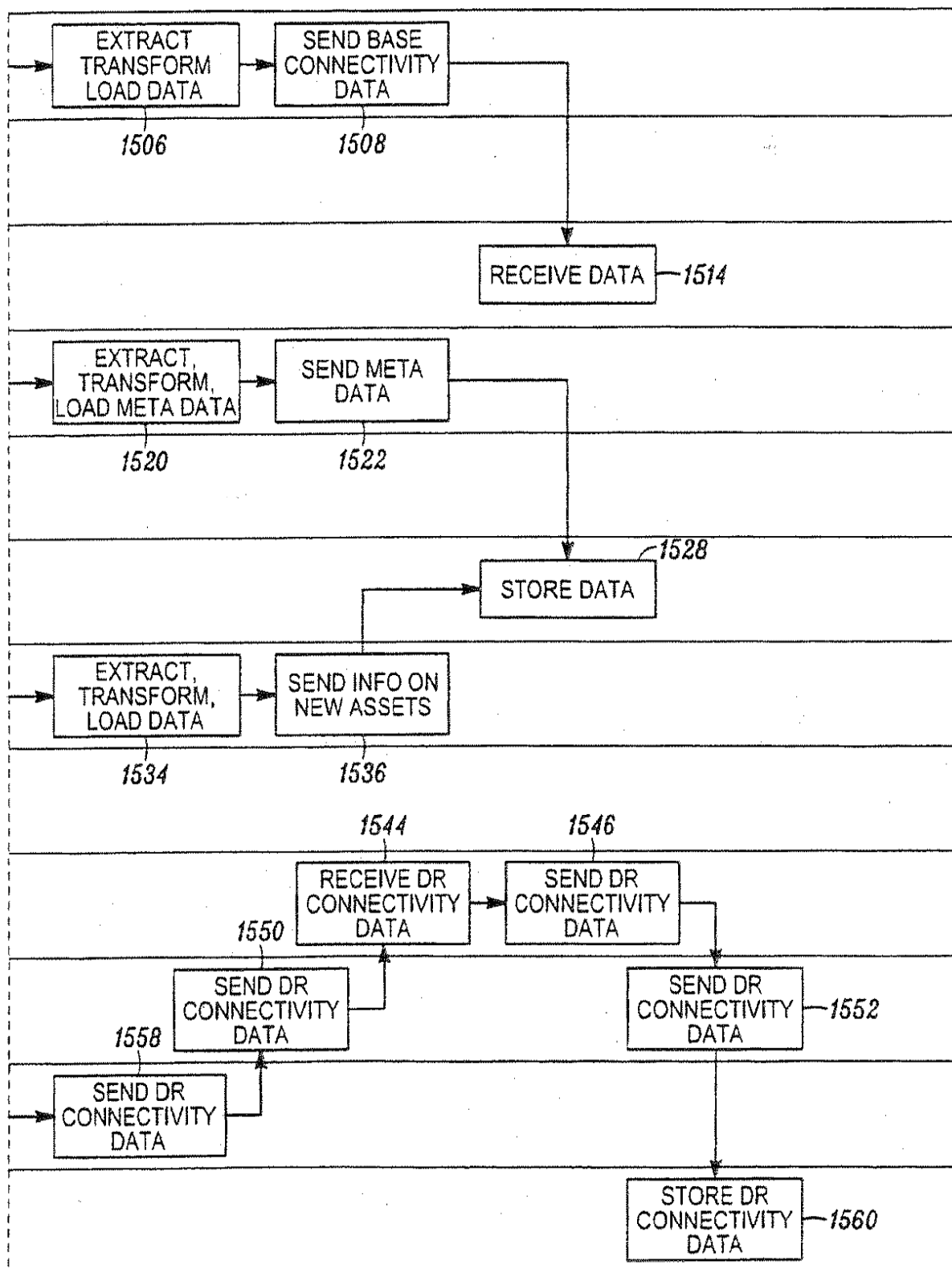


FIG. 15B

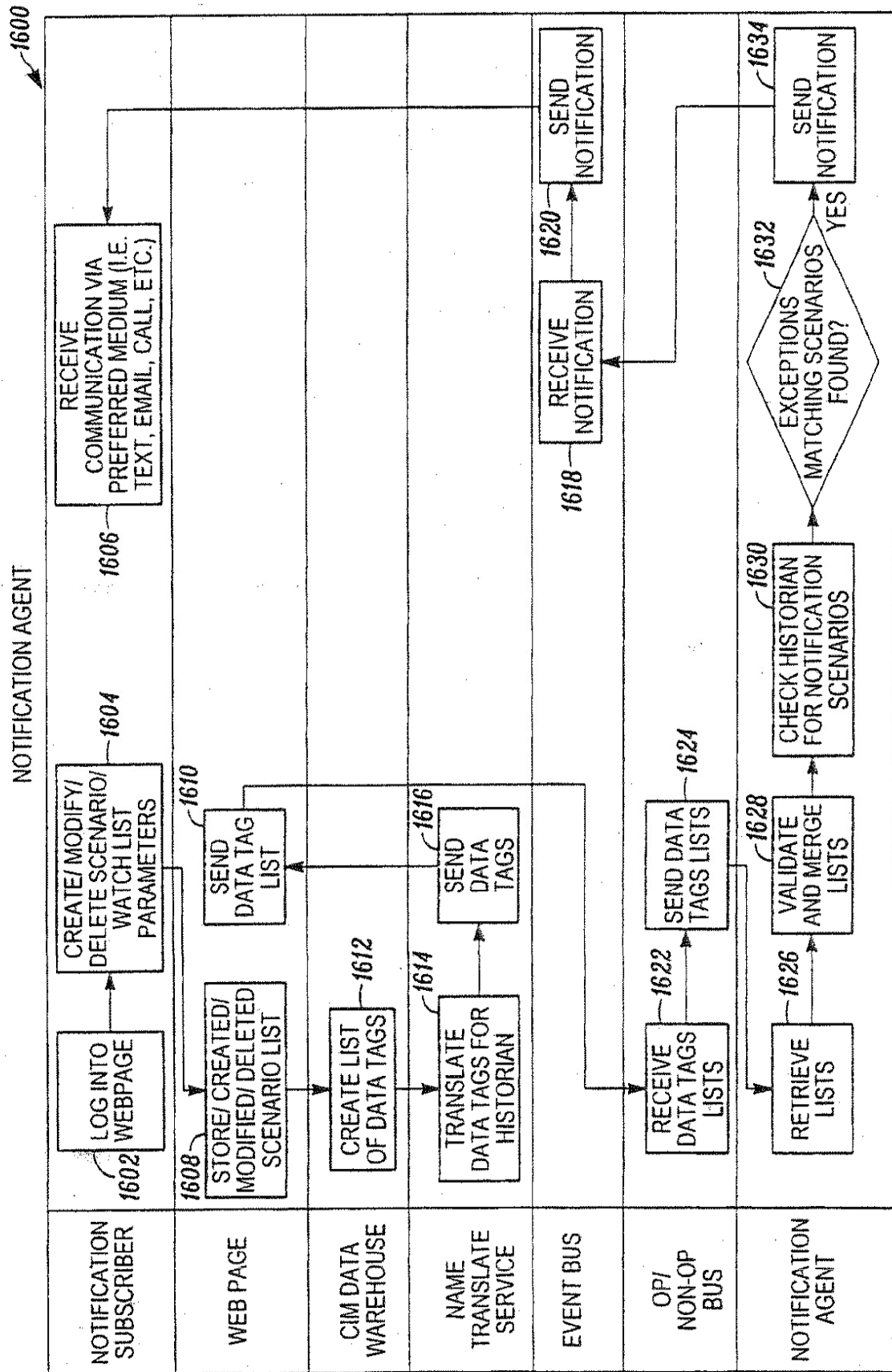


FIG. 16

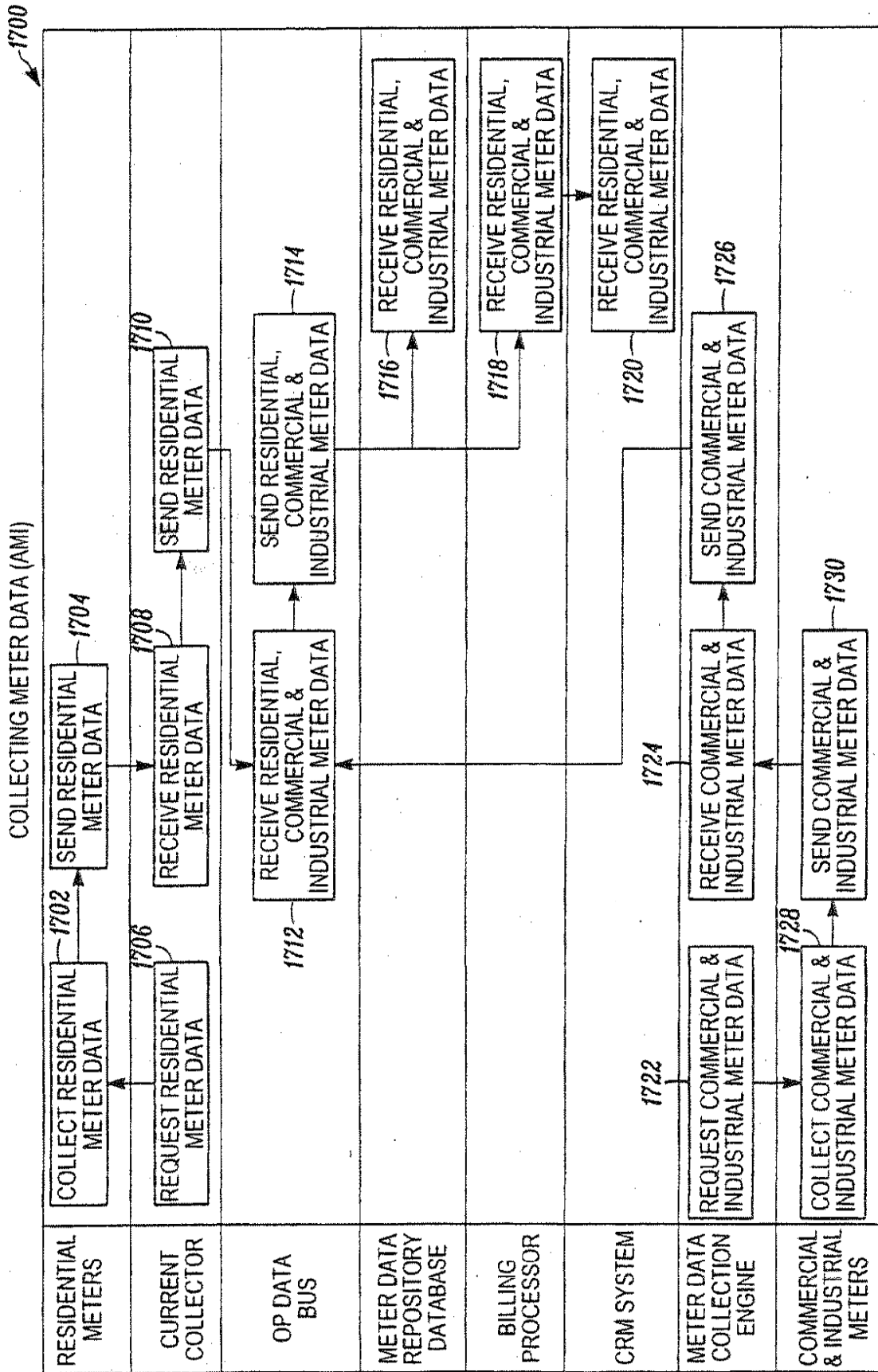
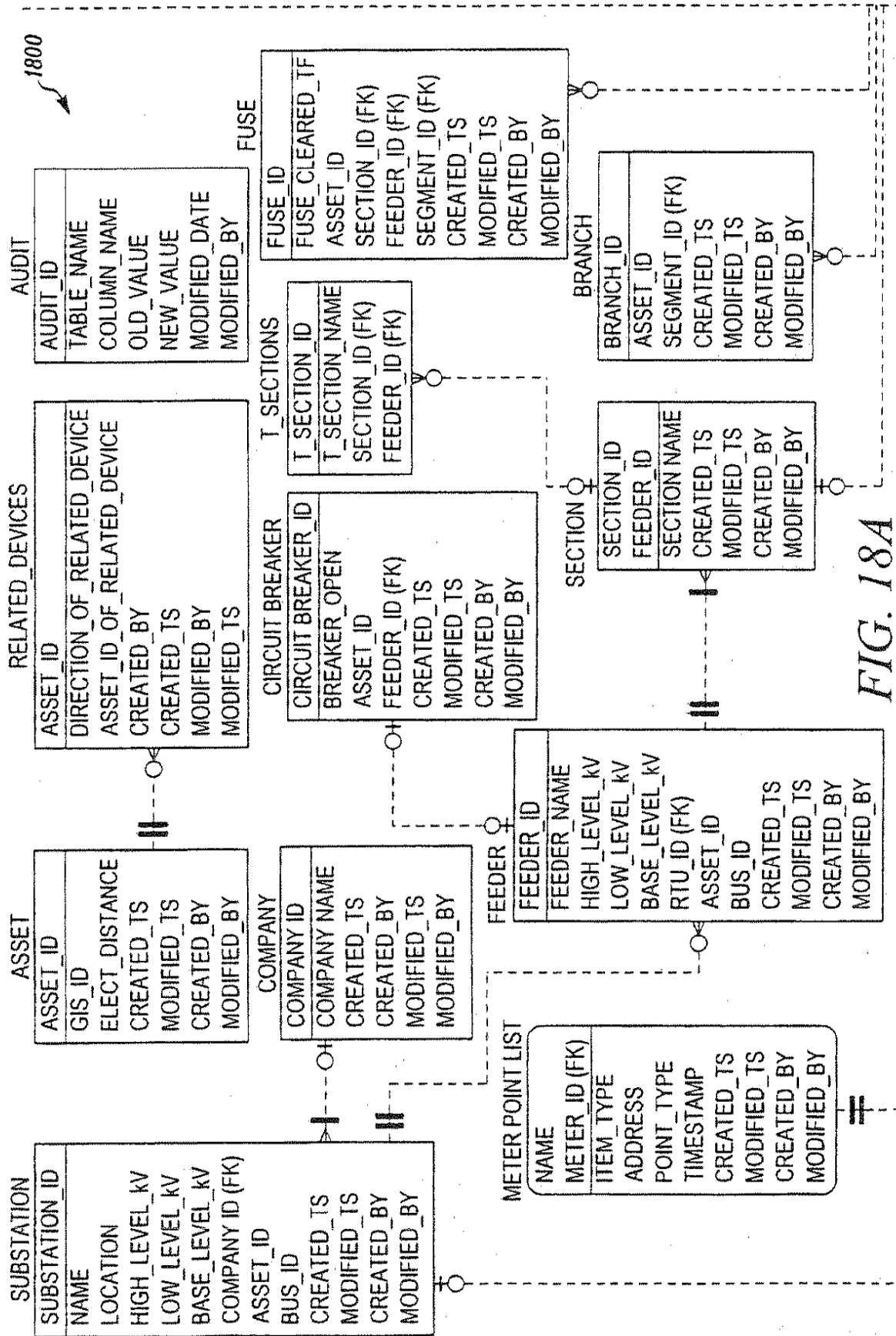
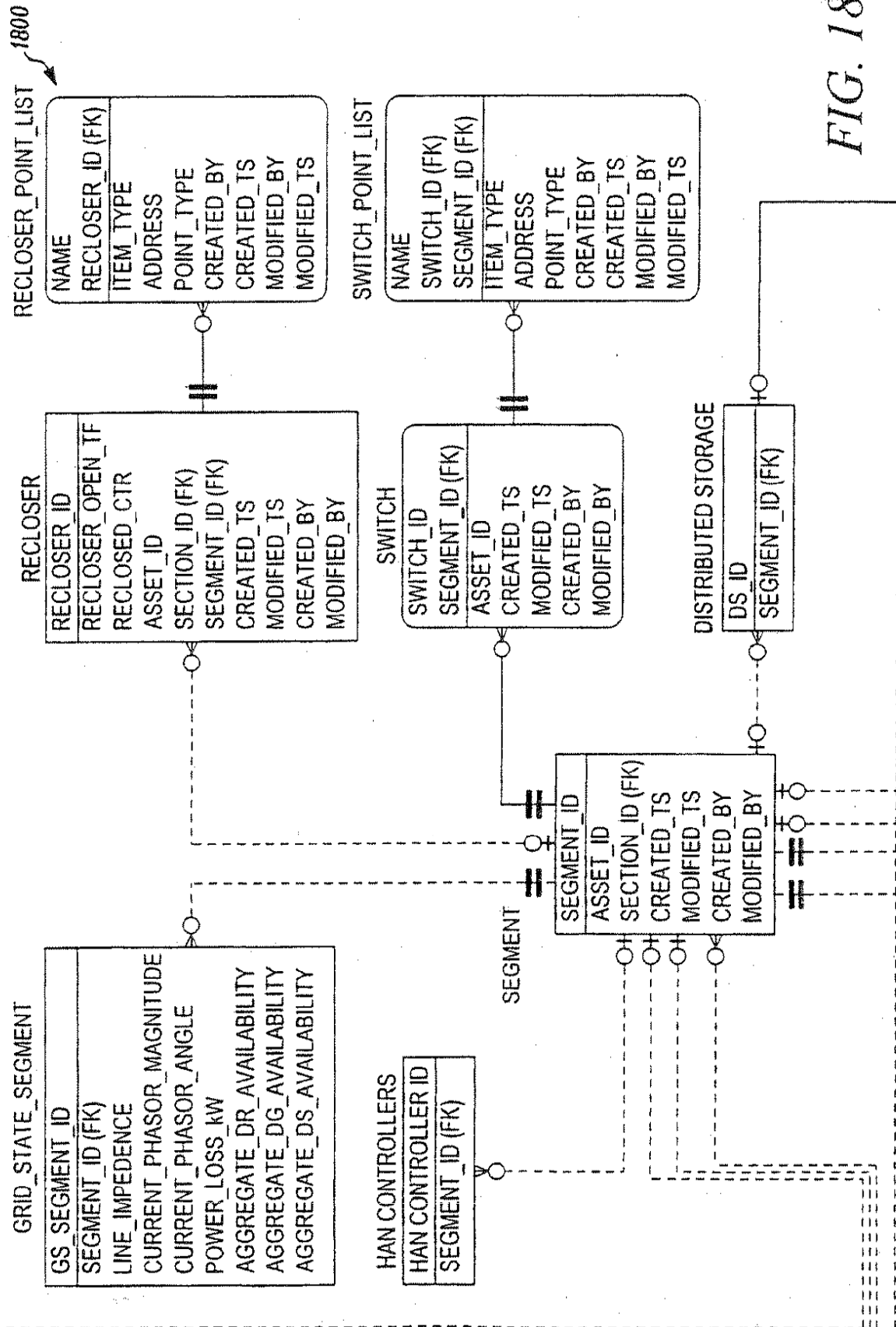


FIG. 17





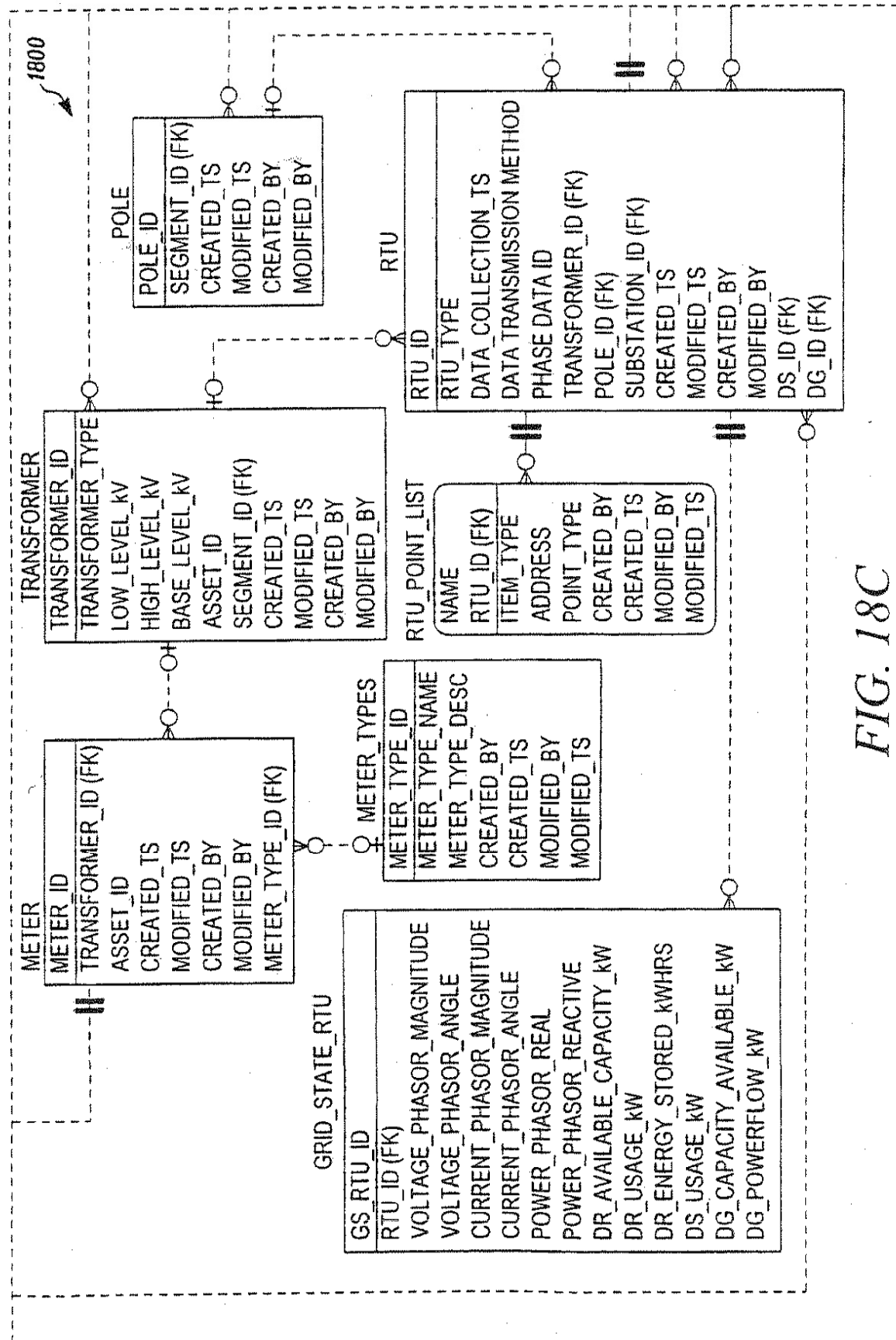


FIG. 18C

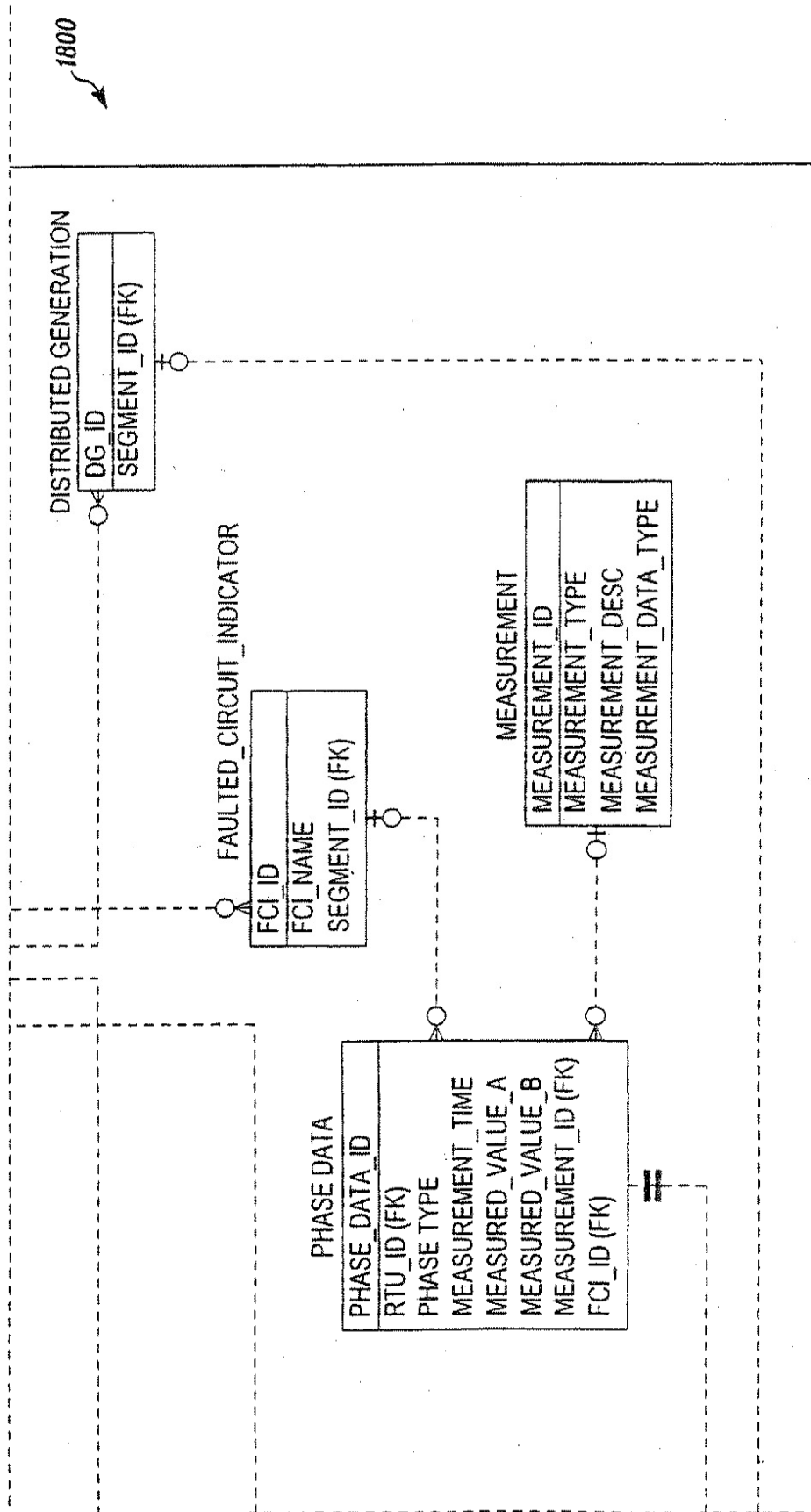
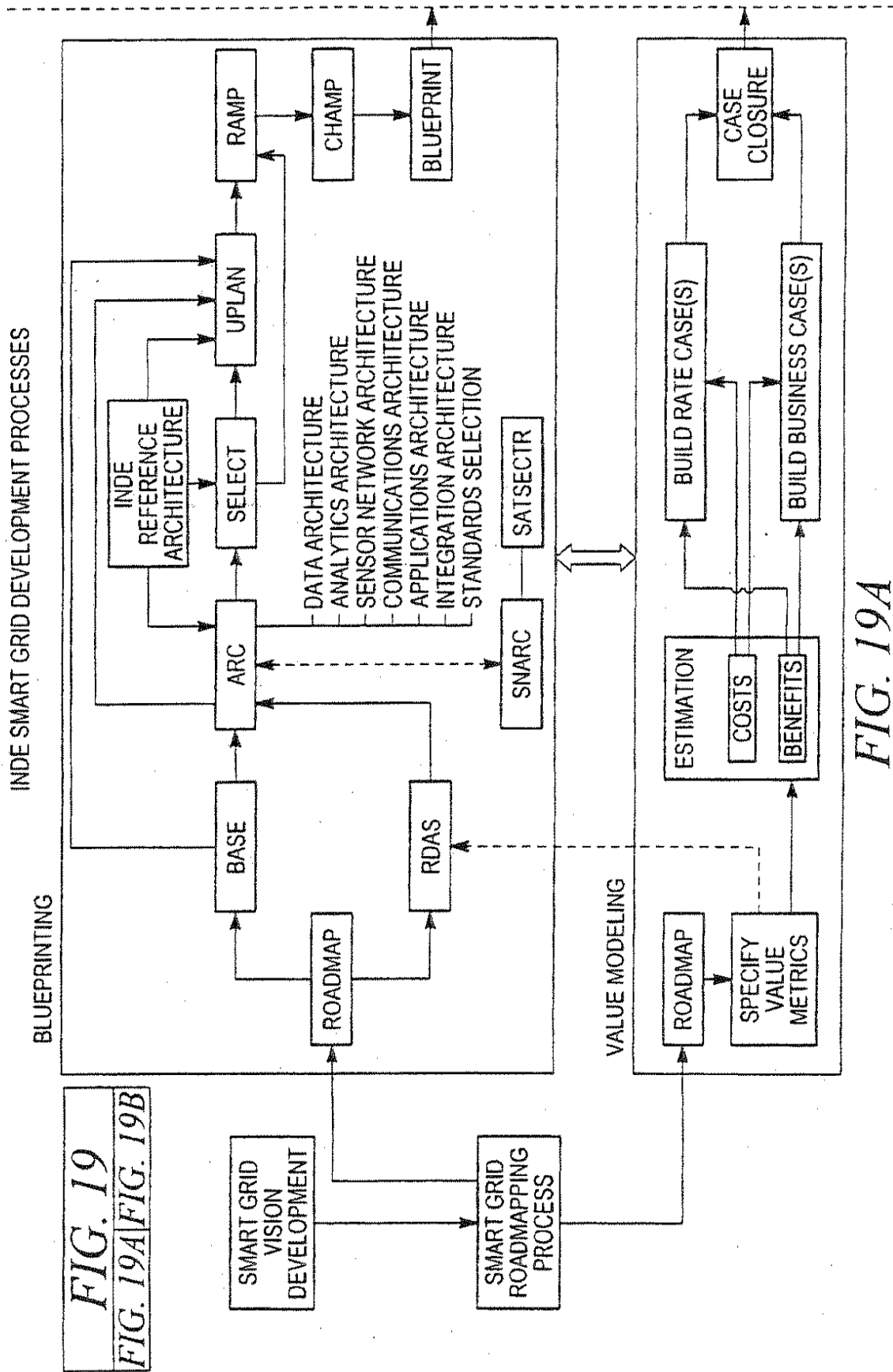


FIG. 18D



BLUEPRINT PROCESS LIST

BASE	BASELINE AND SYSTEMS EVALUATION
RDAS	REQUIREMENTS DEFINITION AND ANALYTICS SELECTION
ARC	ARCHITECTURE CONFIGURATION
SELECT	SOLUTION ELEMENT EVALUATION AND COMPONENTS TEMPLATE
UPLAN	UPGRADE PLANNING FOR APPLICATIONS AND NETWORKS
RAMP	RISK ASSESSMENT AND MANAGEMENT PLANNING
CHAMP	CHANGE ANALYSIS AND MANAGEMENT PLANNING
SNARC	SENSOR NETWORK ARCHITECTURE CONFIGURATION
SATSECTR	SENSOR ALLOCATION VIA T-SECTION RECURSION

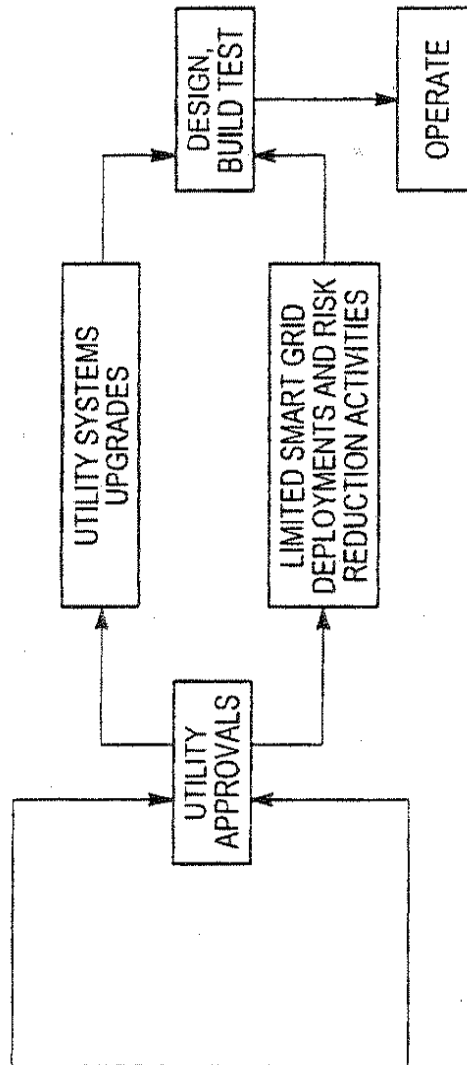


FIG. 19B