Description

Technical field

The present invention relates to devices fabricated by metal-oxide-semiconductor techniques.

Background of the invention

Conventional scaled metal-oxide-semiconductor (MOS) technology has been designed for the implementation of complex large scale integrated circuits containing both analog and digital functional elements. These circuits are generally capable of moderately high speed operation. Operation in the range of gigabits per second is impaired for these circuits because of parasitic capacitances which arise as a result of the fabrication process.

An important parasitic capacitance, in this regard, is the capacitance caused by the gate overlap over the source and the drain regions in the substrate. This overlap is illustrated in Fig. 6 of a technical article by H. Fu et al., *Hewlett-Packard Journal*, pp. 21-7 (1982). Typically, the overlap capacitance is on the order of 0.5 fF/μm.

Another important parasitic capacitance which limits operating speeds for these MOS circuits is the junction capacitance between the regions of different conductivity, i.e., between source (drain) and substrate and between source (drain) and channel.

Summary of the invention

Parasitic capacitances are significantly reduced in accordance with the principles of the invention by differentially oxidizing a substrate and a gate mesa thereon prior to ion implantation and "drive-in" of the drain source regions. This results in a channel region being formed in the substrate beneath and substantially coextensive with the gate mesa. The conductivity of the channel region is different from the conductivity of the adjacent source and drain regions.

Other parasitic capacitances are significantly reduced by differentially oxidizing the substrate and a source layer, a drain layer and a gate mesa thereon prior to ion implantation and "drive-in" of the source and drain regions. The source and drain layers and the gate mesa are heavily doped to an opposite conductivity type from that of the substrate. This results in the channel region being formed in the substrate beneath and substantially coextensive with the gate mesa. Furthermore, source and drain regions are formed beneath the respective source and drain layers and extending up to the channel region.

Brief description of the drawing

A more complete understanding of the invention may be obtained by reading the following description of a specific illustrative embodiment of the invention in conjunction with the appended drawing in which:

Figs. 1 through 3 show an exemplary substrate and polycrystalline silicon layer at various stages of the metal-oxide-semiconductor device fabrication process in accordance with aspects of the present invention.

Detailed description

Fig. 1 shows an exemplary substrate 1 having a semiconductor layer 2 grown or deposited thereon. In general, substrate 1 has been processed by a conventional scaled MOS technology well known to those skilled in the art. This previous processing includes defining active device areas, ion implantation to change thresholds for enhancement or depletion device operation and the like. See, for example, a text by E. H. Nicollian et al. entitled "MOS (Metal Oxide Semiconductor) Physics and Technology" (J. Wiley & Sons, Inc. 1982) or the aforementioned circle by Fu et al.

Substrate 1 is comprised of a doped semiconductor material such as p-type silicon whose doping concentration decreases with distance from the junction with layer 2. An exemplary variation in doping concentration for a 200 to 300 μm thick substrate 1 is from $3.0\times10^{16}/cm^3$ near layer 2 to $1.0\times10^{15}/cm^3$ within several micrometers of layer 2.

Layer 2, in an exemplary embodiment, is comprised of polycrystalline silicon. The conductivity of layer 2 is opposite to the conductivity of substrate 1. Typically, layer 2 is heavily doped to n-type conductivity with phosphorus or arsenic to a concentration of $1.0\times10^{20}/cm^3$ over a thickness of approximately 0.5 μm.

Layer 3 is an optional layer of silicon nitride (Si_3N_4) which is used to protect the top of the source and drain layers (Fig. 2, 21 and 23) and the gate mesa (Fig. 2, 22) from oxide growth during differential oxidization.

Standard photolithographic masking and etching techniques are employed to define source layer 21, gate mesa 22, and drain layer 23. Only gate mesa 22 is insulated from substrate 1 by a thin (~20 nm) insulator or oxide (e.g., SiO_2) layer 43. Layers 31, 32 and 33 result from the photolithographic processing of layer 3 (Fig. 1). Photolithographic processing also exposes substrate surfaces 14 and 15.

There exists a sharp difference in doping concentrations between substrate 1 (exposed substrate surface 14 and 15) and layers 21, 22 and 23. This difference is quite apparent when traversing the perimeter of the wells formed by the sides of gate mesa 22 and source layer 21 and substrate surface 14 (source-gate well) and by the sides of gate mesa 22 and drain layer 23 and substrate surface 15 (drain-gate well). By judicious use of this difference, it is possible to grow a wet oxide at low temperature in the wells as shown in Fig. 2. When oxide growth is complete, oxide layer 41 occupies the source-gate well and oxide layer 42 occupies the drain-gate well. The doping concentration difference causes the oxide layers 41 and 42 to be thicker on the sides of the source/gate/drain layers than on the exposed substrate surfaces. In an example from experimental practice, the sidewalls of oxide layers 41 and 42 are three

times thicker than the bottom, i.e., 0.15 µm versus 0.05 µm. The step of forming an oxide in this manner is known as differential oxidization. Examples of this type of oxidization are given in the following articles: H. Sunami, *J. Electrochem. Soc.*, pp. 892-7 (1978) and T. Kamins, *J. Electrochem. Soc.*, pp. 838—844 (1979).

Ion implantation is then performed into substrate surfaces 14 and 15. Exemplary dopant ions are selected from the group consisting of phosphorus and arsenic. The thick sides of oxide layers 41 and 42 inhibit implantation of dopant ions near to the sides of gate mesa 22. In one sense, the thick sides can be viewed as spacers to keep the implanted ions for the source and drain regions away from the gate mesa 22. In turn, this reduces the capacitance of the gate-drain/source overlap because the overlap resulting from diffusion during "drive-in" is negligible.

Drive-in is a thermal process whereby the source, gate and drain layers and the substrate are heated to a high temperature (~500—1200 degrees Centigrade) for a sufficient time to permit diffusion of the implanted dopant ions into substrate 1. The MOS structure resulting after is shown in Fig. 3.

As shown in Fig. 3, there is a deep diffusion (~0.5—0.6 µm) of the dopants from source layer 21 into the substrate to form deep source region 11. Similarly, the implanted ions through substrate surface 14 diffuse shallowly (~0.1—0.3 µm) to form shallow source region 12. Deep source region 11 and shallow source region 12 form the entire source region. A similar process occurs on the drain side and deep drain region 13 and shallow drain region 12 combine to form the entire drain region. The deep diffusion is caused by using phosphorus ions to dope layers 21 and 23; the shallow diffusion is caused by implanting arsenic ions into substrate surfaces 14 and 15. This type of deep/shallow diffusion is advantageous for reducing the parasitic capacitance between the source (drain) region and the p-substrate 10. The shallow diffusion produces a relatively short, high capacitance junction whereas the deep diffusion produces a relatively long, low capacitance junction with the lower-doped portion of substrate 10.

A channel region defined between n^+-type regions is substantially beneath and coextensive with gate mesa 22. Because of the adjacent shallow source (drain) regions 12, the channel region is electronically controlled almost entirely by gate mesa 22 and the possibility of punch-through is substantially eliminated.

In an example from experimental practice, the channel length measured between regions 12 is in the range 0.5 µm to 1.0 µm. Also, exemplary doping concentrations for the deep regions 11 (13) gradually varies from $1.0\times10^{20}/cm^3$ near the source layer 21 (drain layer 23) to $10^{15}/cm^3$ or $10^{16}/cm^3$ near the lower junction with p-substrate 10. The shallow region 12 exhibits a similar range of variation.

While it has been shown that a deep-shallow diffusion reduces parasitic capacitance, it is contemplated that a deep/deep diffusion or a shallow/shallow diffusion could be used with a degradation because of increased parasitics. These latter diffusions result from using similar dopant ions in layer 21 and 23, in the implant step, through substrate surfaces 14 and 15.

Moreover, it will be obvious to those skilled in the art that the silicon nitride layer 3 is not necessary to protect the tops of layers 21 through 23. Ion milling or reactive ion etching can be used to remove oxide grown on top of layers 21 through 23.

It should also be apparent to those skilled in the art that the teachings contained herein are applicable to all variations of MOS device processing technology. It should be equally clear that, for some MOS device processing techniques, it is necessary to change the conductivity types from those shown in the Figures and described above, i.e., change p-type to n-type and n-type to p-type.

Claims

1. A method of producing semiconductor devices by a metal-oxide-semiconductor process which includes defining a channel region in a silicon substrate (1) of first type conductivity, the substrate (1) having thereon, insulated (43) from the substrate (1), a highly doped polycrystalline silicon gate mesa (22), the method comprising the steps of differentially oxidizing the mesa (22) and the substrate (1) to cause an oxide layer to grow thicker on the sides of the mesa (22) than on an exposed surface of the substrate (1), implanting dopant ions of second type conductivity into the substrate (1) using the gate mesa (22) and the said oxide on the sides thereof as a mask, and heating the resulting structure to diffuse the dopant ions into the substrate (1), thereby forming portions (12) of source and drain regions, defining therebetween the channel region which is substantially coextensive with the gate mesa (22).

2. A method according to claim 1 wherein the mesa is of the second type conductivity.

3. A method of producing semiconductor devices according to claim 1 or 2, wherein the gate mesa (22) is interposed between and separated from a source mesa (21) and drain mesa (23) provided directly on the substrate (1), the source and drain mesas (21, 23) being of highly doped polycrystalline silicon doped with second dopant ions of the second type of conductivity, whereby during the said heating step said second dopant ions out-diffuse from the source and drain mesas (21, 23) to form respectively further portions (11, 13) of the source and drain regions.

4. A method as defined in claim 1 or 2 wherein the said dopant ions of second type conductivity are phosphorus or arsenic ions.

Patentansprüche

1. Verfahren zum Herstellen von Halbleiteran-

times thicker than the bottom, i.e., 0.15 µm versus 0.05 µm. The step of forming an oxide in this manner is known as differential oxidization. Examples of this type of oxidization are given in the following articles: H. Sunami, *J. Electrochem. Soc.*, pp. 892-7 (1978) and T. Kamins, *J. Electrochem. Soc.*, pp. 838—844 (1979).

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Claims

1. A method of producing semiconductor devices by a metal-oxide-semiconductor process which includes defining a channel region in a silicon substrate (1) of first type conductivity, the substrate (1) having thereon, insulated (43) from the substrate (1), a highly doped polycrystalline silicon gate mesa (22), the method comprising the steps of differentially oxidizing the mesa (22) and the substrate (1) to cause an oxide layer to grow thicker on the sides of the mesa (22) than on an exposed surface of the substrate (1), implanting dopant ions of second type conductivity into the substrate (1) using the gate mesa (22) and the said oxide on the sides thereof as a mask, and heating the resulting structure to diffuse the dopant ions into the substrate (1), thereby forming portions (12) of source and drain regions, defining therebetween the channel region which is substantially coextensive with the gate mesa (22).

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3. A method of producing semiconductor devices according to claim 1 or 2, wherein the gate mesa (22) is interposed between and separated from a source mesa (21) and drain mesa (23) provided directly on the substrate (1), the source and drain mesas (21, 23) being of highly doped polycrystalline silicon doped with second dopant ions of the second type of conductivity, whereby during the said heating step said second dopant ions out-diffuse from the source and drain mesas (21, 23) to form respectively further portions (11, 13) of the source and drain regions.

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Patentansprüche

1. Verfahren zum Herstellen von Halbleiteran-

* C L M S *

ordnungen durch einen Metall-Oxid-Halbleiterprozeß, der die Definition einer Kanalzone in einem Siliciumsubstrat (1) des ersten Leitungstyps umfaßt, wobei das Substrat (1) hierauf und gegenüber ihm isoliert (43) eine stark dotierte polykristalline Siliciumgate-Mesa (22) aufweist, und wobei das Verfahren die Schritte umfaßt

—differenziertes Oxidieren der Mesa (22) und des Substrates (1), um das Aufwachsen einer Oxidschicht auf den Seiten der Mesa (22) zu veranlassen, und zwar mit einer größeren Dicke als auf einer freiliegenden Fläche des Substrates (1),

—Implantieren von Dotierstoffionen des zweiten Leitungstyps in das Substrat (1) unter Verwendung der Gate-Mesa (22) und des Oxides auf deren Seiten als eine Maske und

—Erwärmen der resultierenden Struktur, um die Dotierstoffionen in das Substrat (1) zu diffundieren und dadurch Teile (12) von Source- und Drainzonen zu erzeugen, die zwischen sich eine im wesentlichen mit der Gate-Mesa (22) koextensive Kanalzone definieren.

2. Verfahren nach Anspruch 1, bei dem die Mesa vom zweiten Leitungstyp ist.

3. Verfahren zum Herstellen von Halbleiteranordnungen nach Anspruch 1 oder 2, bei dem die Gate-Mesa (22) zwischen einer direkt auf dem Substrat (1) vorgesehenen Source-Mesa (21) und einer Drain-Mesa (23) sowie im Abstand von diesen angeordnet ist, und die Source- und Drain-Mesen (21, 23) aus stark dotiertem polykristallinem Silicium, das mit zweiten Dotierstoffionen des zweiten Leitungstyps dotiert ist, sind, wodurch während des Erwärmungsschrittes die zweiten Dotierstoffionen aus den Source- und Drain-Mesen (21, 23) diffundieren, um je weitere Teile (11, 13) der Source- und Drainzonen zu bilden.

4. Verfahren wie in Anpruch 1 oder 2 definiert, wobei die Dotierstoffionen des zweiten Leitungstyps Phosphor- oder Arsenionen sind.

Revendications

1. Un procédé de fabrication de dispositifs à semiconducteurs par un processus métal-oxyde-semiconducteur qui comprend la définition d'une région de canal dans un substrat en silicium (1) d'un premier type de conductivité, le substrat (1) portant une structure mésa de grille (22) en silicium polycristallin fortement dopé, qui est isolée (43) du substrat (1), le procédé comprenant les étapes qui consistent à oxyder de façon différentielle la structure mésa (22) et le substrat (1) pour faire croître une couche d'oxyde avec une épaisseur plus élevée sur les côtés de la structure mésa (22) que sur une surface à nu du substrat (1), à implanter des ions de dopant d'un second type de conductivité dans le substrat (1), en utilisant en tant que masque la structure mésa de grille (22) et l'oxyde qui se trouve sur les côtés de celle-ci, et en chauffant la structure résultante pour faire diffuser les ions de dopant dans le substrat (1), pour former ainsi des parties (12) de régions de source et de drain, définissant entre elles la région de canal qui a pratiquement la même étendue que la structure mésa de grille (22).

2. Un procédé selon la revendication 1, dans lequel la structure mésa est du second type de conductivité.

3. Un procédé de fabrication de dispositifs à semiconducteurs selon la revendication 1 ou 2, dans lequel la structure mésa de grille (22) est intercalée, en en étant séparée, entre une structure mésa de source (21) et une structure mésa de drain (23) qui sont directement formées sur le substrat (1), les mésas de source et de drain (21, 23) étant en silicium polycristallin fortement dopé, qui est dopé avec des seconds ions de dopant du second type de conductivité, grâce à quoi pendant l'étape de chauffage, les seconds ions de dopant diffusent vers l'extérieur à partir des structures mésa de source et de drain (21, 23), pour former respectivement des parties supplémentaires (11, 13) des régions de source et de drain.

4. Un procédé selon la revendication 1 ou 2, dans lequel les ions de dopant du second type de conductivité sont des ions phosphore ou arsenic.

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