read memories 2NR (the anti-fuse memories 2a and 2b) are connected.

[0038] Thereafter, the selected reading bit voltage of 0 V is applied to the selected reading bit line BLc. Thereby, in the selected read memory 2R, the selected reading word voltage of 1.2 V is applied from the selected reading word line WLc to the P-type semiconductor region 8 of the rectifier element 3 while the selected reading bit voltage of 0 V is applied from the selected reading bit line BLc to the diffusion region 5 disposed at an end of the memory capacitor 4.

[0039] Since the memory gate insulating film 6 of the memory capacitor 4 in the selected read memory 2R has been broken down and data has been programmed into the selected read memory 2R, a forward bias voltage is applied from the P-type semiconductor region 8 to the N-type semiconductor region 7 of the rectifier element 3 due to the selected reading word voltage of 1.2 V applied to the selected reading word line WLc. Thereby, in the selected read memory 2R, the selected reading word voltage applied from the selected reading word line WLc is applied from the rectifier element 3 through the memory capacitor 4 to the selected reading bit line BLc.

[0040] As a result, a voltage which is lowered from the selected reading word voltage of 1.2 V by the value of the built-in potential through the selected read memory 2R (the anti-fuse memory 2C) is applied to the selected

[0080] In the anti-fuse memory 22b, to which data is not to be programmed and which is connected to the nonselected programming bit lines BL1b and BL2b to each of which the nonbreakdown bit voltage of 3 V is applied, the voltage difference between the memory gate electrode Ga (Gb) and the corresponding diffusion region 5 in the memory capacitor 24a (24b) becomes as small as 3 V. Hence, even when the memory gate insulating films 6a and 6b below the memory gate electrodes Ga and Gb in the memory capacitors 24a and 24b in the anti-fuse memory 22b have not been broken down, the dielectric breakdown of the memory gate insulating films 6a and 6b does not occur and remain insulated. Thus the anti-fuse memory 22b maintains a state in which no data has been programmed.

[0081] For example, even when the memory gate insulating films 6a and 6b of the memory capacitors 24a and 24b in the anti-fuse memory 22b, to which the nonbreakdown bit voltage of 3 V is applied from the nonselected programming bit lines BL1b and BL2b, have been broken down, a channel is not formed in the memory capacitors 24a and 24b because the nonbreakdown word voltage of 0 V is applied to the nonselected programming word line WLb. Hence the memory capacitors 24a and 24b blocks the nonbreakdown bit voltage of 3 V applied from the nonselected programming bit lines BL21b and BL22b, so that the nonbreakdown bit voltage is prevented from being applied to the memory gate electrodes Ga and Gb through

the memory gate insulating films 6a and 6b that have been broken down.

[0082] However, in a case where the positions of the dielectric breakdown of the memory gate insulating films 6a and 6b are extremely close to the diffusion regions 5 connected to, for example, the bit lines BL21 and BL22, respectively, the potentials of the bit lines BL21 and BL22 may not be blocked by the channels of the memory capacitors 24a and 24b. In this case, the nonbreakdown bit voltage of 3 V applied to the diffusion regions 5 may be applied to the memory gate electrodes Ga and Gb.

[0083] In the anti-fuse memory 22b, the nonbreakdown bit voltage of 3 V applied from each of the memory gate electrodes Ga and Gb to the rectifier element 23 is a reverse bias applied from the N-type semiconductor region to the P-type semiconductor region in the rectifier element 23, because the rectifier element 23, which performs rectification (commutation) due to the semiconductor junction structure of the N-type semiconductor region and the P-type semiconductor region, is connected to the memory gate electrodes Ga and Gb of the memory capacitors 24a and 24b.

[0084] In the anti-fuse memory 22a, into which data is not to be programmed and which is connected to the nonselected programming word line WLb, to which the nonbreakdown word voltage of 0 V is applied, and the nonselected programming bit lines BL1b and BL2b, to each

[0126] Here, for example, in the anti-fuse memory 22c according to the above second embodiment as shown in FIG. 5, the respective memory gate electrodes Ga and Gb of the memory capacitors 24a and 24b are connected to one rectifier element 23. Hence, in a case where the memory gate insulating films 6a and 6b of the memory capacitors 24a and 24b have been broken down, the memory capacitors 24a and 24b may be electrically connected. In this case, in anti-fuse memory 22c according to the second embodiment, the bit lines BL11 and BL12 may be electrically connected through the memory capacitors 24a and 24b. In a case where the breakdown bit voltage of 0 V is being applied to the bit line BL11, it is difficult to maintain the nonbreakdown bit voltage of 3 V applied to the bit line BL12 in the process described in “(2-2-2) Sequentially programming the same data into a plurality of memory capacitors”.

[0127] In the anti-fuse memory 37c according to the third embodiment shown in FIG. 7, the rectifier elements 3a and 3b are provided for the respective memory capacitors 4a and 4b. The memory capacitors 4a and 4b are electrically insulated from each other. Hence, the bit lines BL11 and BL 12 are prevented from being electrically connected through the memory capacitors 4a and 4b even when the memory gate insulating films 6a and 6b of the memory capacitors 4a and 4b have been broken down.

memory gate insulators 6a and 6b below the memory gate electrodes Ga and Gb of the memory capacitors 44a and 44b break down, respectively. Thereby the diffusion regions and the respective memory gate electrodes Ga and Gb become conductive state, with a low resistance. Thus, the selected program memory 2W achieves a state in which the same data has been programmed into the memory capacitors 44a and 44b.

[0144] In the anti-fuse memory 42b, to which the nonbreakdown bit voltage of 3 V is applied from the nonselected programming bit line BLb, a channel is not formed in the memory capacitors 44a and 44b and the memory capacitors 44a and 44b block the nonbreakdown bit voltage of 3 V applied from the nonselected programming bit line BLb because the nonbreakdown word voltage of 0 V is applied to the nonselected programming word line WLb even when, for example, the memory gate insulating films 6a and 6b of the memory capacitors 44a and 44b have been broken down. Hence, the nonbreakdown bit voltage is not applied through the memory gate insulating films 6a and 6b, which have been broken down, to the memory gate electrodes Ga and Gb.

[0145] However, in a case where the positions of the dielectric breakdown of the memory gate insulating films 6a and 6b are extremely close to the diffusion regions connected to, for example, the nonselected programming bit line BLb, the channels of the memory capacitors 44a

and 44b cannot block the potential of the nonselected programming bit line BLb, so that the nonbreakdown bit voltage of 3 V applied to the diffusion regions may be applied to the memory gate electrodes Ga and Gb.

[0146] In the anti-fuse memory 42b, the rectifier element 23 is disposed between the word line WL1 and the memory gate electrodes Ga and Gb of the memory capacitors 44a and 44b. The rectifier element 23 performs rectification through a semiconductor junction structure of the N-type semiconductor region and the P-type semiconductor region. Hence, in a case where the nonbreakdown bit voltage is applied from each of the memory gate electrodes Ga and Gb to the rectifier element 23, the nonbreakdown bit voltage is a reverse bias in the rectifier element 23. Thus, the rectifier element 23 prevents the voltage from being applied to the word line WL1.

[0147] The descriptions for the anti-fuse memories 42a, 42b, and 42d, into which data is not to be programmed, are omitted to avoid the repetition of the above-described “(2-2-1) Simultaneously programming the same data into a plurality of memory capacitors”.

[0148] Data of a desired memory, the anti-fuse memory 42c, of the semiconductor memory device 41 of the fourth embodiment is read by following the above-described “(2-3) Data reading operation”, and the descriptions thereof are omitted.

[0149] (4-3) Operations and Effects

applied from the memory gate electrode G1 to the word line WL.

[0168] In the anti-fuse memory 50 including the rectifier element 51, which includes the MOS transistor structure, the rectifier element gate electrode G2 of the rectifier element 51 and the memory gate electrode G1 of the memory capacitor 47 are disposed within one wiring layer (the same layer). The thickness of the rectifier element gate electrode G2 is the same as the thickness of the memory gate electrode G1 of the memory capacitor 47. Hence, the overall thickness of the anti-fuse memory 50 is reduced.

[0169] At the time of data programming operation in the anti-fuse memory 50, the breakdown word voltage of 5 V is applied to the word line WL, and the breakdown bit voltage of 0 V is applied to the bit line BL. A voltage of 5 V, which is the same as the breakdown word voltage, is applied through the well control terminal VNW to the well on which the rectifier element 51 is disposed. In a case where the potential of the source region of the rectifier element 51 is approximately 0 V, the rectifier element 51 turns on. In a case where the threshold voltage is -0.7 V, the source region is charged to 4.3 V.

[0170] Hence, in the memory capacitor 47, the breakdown word voltage of 5 V is applied from the rectifier element 51 to the memory gate electrode G1. Since 0 V is applied to the bit line, the memory capacitor 47 is turned on. The channel potential becomes 0 V. As a result, a large

electrode G1 is connected to a source region of the rectifier element 46. In the rectifier element 46, the rectifier element gate electrode G2 and the drain region are connected to the word line WL1. The rectifier element 46 is turned off in accordance with the voltage values applied to the memory gate electrode G1 and the word line WL1. Thereby the voltage applied from the memory gate electrode G1 of each of the memory capacitors 47a, 47b, and 47c to the source region is prevented from being applied to the word line WL1.

[0180] In the anti-fuse memories 56a, 56b, 56c, and 56d, the same voltage is applied from the word line WL1 (WL2) through the rectifier element 46 to the memory gate electrode G1 of each of the memory capacitors 47a, 47b, and 47c, while the turned-off rectifier element 46 blocks the voltage applied from the memory gate electrode G1 of each of the memory capacitors 47a, 47b, and 47c to the word line WL1 (WL2).

[0181] FIG. 10 shows voltage values at the respective sites in a case where data is simultaneously programmed only into the memory capacitors 47a, 47b, and 47c of the anti-fuse memory 56c, which is disposed at the intersection of the second row and the first column, and data is not programmed into the anti-fuse memories 56a, 56b, and 56d. In this case, in the semiconductor memory device 55, the breakdown bit voltage of 0 V is applied to each of the bit lines BL11, BL12, and BL13 (the selected