A SEMICONDUCTOR DEVICE LAYOUT AND CHANNELING IMPLANT PROCESS

Background of Invention

1) Field of the Invention

This invention relates generally to fabrication of semiconductor devices particularly to the fabrication of implanted doped regions in a semiconductor device that has a graded junction

2) Description of the Related Art

With higher levels of integrated circuits on semiconductor chips and the need for faster transistors in these circuits, the FET transistor must maximize all aspects of semiconductor physics to fabricate transistors in these circuits with faster switching speed.

As the transistor scaling to smaller dimension, the inventor have found that high Vt NMOS transistor is facing a problem with voltage limitation. Thermal cycle was limited because of the consideration of logic device in the wafer. An aspect of this invention address issue.

In crystalline solids, such as monocrystalline silicon, the atoms which make up the solid are spatially arranged in a periodic fashion. This periodic arrangement of atoms in a crystal is called a lattice. The crystal lattice always contains a volume which is representative of the entire lattice and it is regularly repeated throughout the crystal. The directions in a lattice are expressed as a set of three integers with the same relationship as the components of a vector in that direction. The three vector components are given in multiples of the basic vectors. For example, in cubic lattices, such as silicon which has a diamond crystal lattice, the body diagonal has the components of 1a, 1b, and 1c and this diagonal exist along the [111] direction with the [] brackets being used to denote a specific direction. However, many directions in a crystal are equivalent, depending on the arbitrary choice of orientation of the axes. Such equivalent directions are denoted with < > brackets and, for example, crystal directions in the cubic lattice [100], [010], and [001] are all crystallographically equivalent and are <100> directions. Since these directions will also be on the negative side of the origin, as arbitrarily defined, they also are identified with a (-) over the specific negative integer, such as $[\bar{1}00]$, $[0\bar{1}0]$, and $[00\bar{1}]$ for <100> directions. Unless specifically stated or shown in the following description in this application, a crystal direction includes both positive and negative integers.

Planes in a crystal also can be determined with a set of three integers h, k, and l. They are used to define a set of parallel planes and each set of three integers in ( ) parentheses identify a specific plane. As in the case of directions, many planes in a lattice

are equivalent and the indices of such equivalent planes are denoted by { } parentheses. For cubic lattices, direction [k,l,m] is perpendicular to a plane with the identical three integers (k,l,m). Thus, if either a direction or a plane of a cubic lattice is known, its perpendicular counterpart can be quickly determined without calculation. For example, for planes of equivalent symmetry such as {100} plane, the equivalent planes are (100), (010), (001), (100), (010), and (001). Like the crystal direction, the crystal plane in the following description in this application includes both positive and negative integers unless specifically stated otherwise.

General terminology is: ( ) for a certain plane; { } for a group of planes; [ ] for a certain direction; < > for a group of directions.

Ion implant processes are important to forming doped regions in substrates. The depth to which an ion becomes implanted is proportional to its kinetic energy. The implanted distribution in an amorphous target is roughly a Gaussian distribution characterized by a mean, known as the range, and a standard deviation, known as the straggle. In a single crystal target, the range and straggle for a given implant may be different than that in amorphous material, due to a phenomena known as ***channeling***. Higher ion energy, higher silicon temperature, and the growth of silicon dioxide layers on the silicon all tend to dechannel implants. In any event, range and straggle data for various materials including silicon, silicon dioxide, and photoresist have been determined.

The more relevant technical art in the patent literature is as follows:

US 5,970,300(Buynoski) shows an alignment of a FET on a wafer.

US 6,566,204(Wang, et al.) teaches the use of mask shadowing and angled implantation in fabricating asymmetrical field-effect transistors.

US 6,599,804(Bulucea, et al.)shows a fabrication of field-effect transistor for alleviating short-channel effects.

US 4,728,617(Woo, et al.) shows a method of fabricating a MOSFET with graded source and drain regions using a high tilt I/I.

However, there is a need for an improved process and device.

Summary of the Invention

It is an object of an embodiment the present invention to provide a device and method for fabricating a transistor with a graded doped region.

It is an object of an embodiment the present invention to provide a high voltage MOS device that has a higher breakdown voltage.

Some embodiments of the invention comprise implanting ions into said silicon substrate to form doped regions adjacent to said gate. The orientation of the channel region in the Si crystal structure (channel direction < 100>) in combination with the large angle tilt and twist implant process that increases channeling (described below) produces doped regions that have a more graded (gradual) junction.

With the embodiment's (a) transistor with a channel direction at < 100> and (b) the 45 tilt and 45 twist implant, the implanted ions enter the substrate at the <1 1 0> direction. This direction increases the channeling of the ion to create a graded junction.

An embodiment is a method of fabrication of doped regions in a semiconductor device; comprising the steps of :

a) providing a {001} silicon substrate;

b) forming a gate over said silicon substrate; said gate having a width and a length; a channel under the gate; said channel having a channel direction parallel with the direction of said gate width; said channel direction is [100] or [010] direction;

c) implanting ions into said silicon substrate to form a doped region adjacent to said gate; the implantation of ions comprises a large angle tilt implant with a twist of between about 40 and 50 degrees and a tilt angle of 40 and 50 degrees.

Another aspect of the embodiment is where said doped region is a N-LDD in an offset LDMOS FET.

Another aspect of the embodiment is where said ions being implanted about along the [110] directions of the silicon substrate.

Another aspect of the embodiment is where the implanting of said ions is performed in one implant step at an about 45 degree twist implant and a tilt angle of about 45 degrees.

Another aspect of the embodiment is where said silicon substrate has a notch/flat at a [110] direction.

Another aspect of the embodiment is where the implanting of ion further comprises: said silicon substrate has a notch/flat at a <110> direction, the implantation comprises an implant with a 45 tilt and 45 twist and the ions enter the substrate aligned at a <0 -1 -1> direction whereby the direction increases the channeling.

Another aspect of the embodiment is where said channel has an annular shape with a doped region on the inside of said channel and a second doped region surrounding the outside of said channel.

Another aspect of the embodiment is where said channel has an annular shape with a doped region on the inside of said channel region and a second doped region surrounding the outside of said channel; and the implanting of said ions further comprises a quadra implant at the twist angles of about 45, 135, 225 and 315 degrees with a range of +/- 5 degrees; and a tilt angle between 40 and 50 degrees.

Another aspect of the embodiment is where said channel has an annular shape with a doped region on the inside of said channel and a second doped region surrounding the outside of said channel region; and the implanting of said ions further comprises a quadra implant with the ion beams aligned with the <110> direction within plus/minus 2 degrees.

The orientation and implant process creates more channeling of ions. The channeling of ions creates a more graded junction.

When implemented on a HV MOS Tx, the graded junction of the LDD increases the drain breakdown voltage.

The above and below advantages and features are of representative embodiments only, and are not exhaustive and/or exclusive. They are presented only to assist in understanding the invention. It should be understood that they are not representative of all the inventions defined by the claims, to be considered limitations on

the invention as defined by the claims, or limitations on equivalents to the claims. For instance, some of these advantages may be mutually contradictory, in that they cannot be simultaneously present in a single embodiment. Similarly, some advantages are applicable to one aspect of the invention, and inapplicable to others. Furthermore, certain aspects of the claimed invention have not been discussed herein. However, no inference should be drawn regarding those discussed herein relative to those not discussed herein other than for purposes of space and reducing repetition. Thus, this summary of features and advantages should not be considered dispositive in determining equivalence. Additional features and advantages of the invention will become apparent in the following description, from the drawings, and from the claims.

Brief Description of the Drawings

The features and advantages of a semiconductor device according to the present invention and further details of a process of fabricating such a semiconductor device in accordance with the present invention will be more clearly understood from the following description taken in conjunction with the accompanying drawings in which like reference numerals designate similar or corresponding elements, regions and portions and in which:

Figure 1A is a top down view of a wafer having a transistor according to a process known to the inventor.

Figure 1B shows a schematic view of a twist and tilted ion implant according to the prior art for use in understand the terms "twist" and "tilt".

Figure 2A shows a FET with a channel direction 202 in a <100> direction according to an embodiment of the invention.

Figure 2B shows a FET with a channel direction 204 in a <110> direction according to an embodiment of the invention.

Figure 3A is a top down view of a wafer showing the channel orientation in a 45 degree twist and 45 degree tilt implant according to an embodiment of the invention.

Figure 3B is a top down view of a wafer showing the channel orientation <010> in a 45 degree twist and 45 degree tilt implant according to an embodiment of the invention.

Figure 4A shows a top down view of a embodiment of a closed shaped transistor according to an embodiment of the invention.

Figure 4B shows a cross sectional view of the closed FET shown in figure 4A along the axis 4B according to an embodiment of the invention.

Figure 5 shows a plot of the phosphorus concentration of the graded junction N- LDD of the embodiment in a normal V MOS TX compared to a conventional Ph profile.

Figure 6 shows both a standard 0 degree channel 102 104 FET and the embodiments' 45 degree angled channel 202 204 FETs formed on a wafer.

Figure 7 shows an example of an offset LDMOS TX according to an embodiment of the invention. The channel for the LDNMOS TX is preferably a p-well.

Figure 8 shows an example of a non-offset LDMOS TX formed using the embodiment's channel maximizing implant process for the source and drain.

Detailed Description of the Preferred Embodiments

II. INTRODUCTION - CURRENT INDUSTRY CHANNEL DIRECTION WITH RESPECT TO THE CRYSTAL DIRECTION

Referring now to the drawing and more particularly to Fig 1A, there is shown a structure over which the present invention is an improvement.

Figure 1A is a top down view of a wafer having a transistor. The wafer is {001}. The channel direction 102 is <110>. The channel direction is the direction between source and drain or drain and source. The channel direction is the direction current flows between the source and drain or drain and source. In current 8 inch P-type wafer technology, the notch is along the <110> direction as shown in figure 1A.

In manufacturing the FET with the source (S) and drain (D) separated by the gate (G) and having a channel (C) thereunder, the notch permits alignment of the wafer relative to the exposure masks so that the gate width and the channel length thereunder will be parallel or perpendicular with [110] crystal direction.

Problem of voltage limitation on Hi Vt NMOS

As the transistor scaling to smaller dimension, our high Vt NMOS transistor is facing a problem with voltage limitation. Thermal cycle was limited because of the consideration of logic device in the wafer.

Currently for high voltage transistor, we need to use high tilt implantation and long time diffusion in order to make the lateral junction of the LDD more graded. For example a lateral diffusion metal oxide semiconductor {LDMOS} was used for high voltage usage. However the LDD regions of the LDMOS need long time (several hours) diffusion to get a graded junction which can sustain high voltage. For sub-micron technology, because of the thermal cycle become more critical. Lower thermal cycle was needed because of the transistor dimension. In this case, LDMOS is not popular for small dimension high voltage transistor. There are mainly two high voltage transistors in the foundry for sub-micron transistors, offset transistor and non-offset transistor. Offset transistor use asymmetrical structure to get higher breakdown voltage. Non-offset structure use higher tilt angle for lateral doped drain (LDD) implantation to increase the breakdown voltage.

Overview of embodiments of the invention

In this example embodiment, a special layout for a high voltage transistor is introduced. A set of specific implantation method is given accordingly. A main advantage of this embodiment is to use the silicon crystalogy to get higher channeling effect through special implantation angle and rotation. Accordingly the layout for this implantation was optimized in order to get a more graded junction.

We implant ions into the {0 0 1} silicon substrate to form doped regions adjacent to the gate. The orientation of the channel region in the Si crystal structure (channel direction < 100>) in combination with the large angle tilt and twist implant process (describe below) produces doped regions that have a more graded (gradual) junction. The orientation and implant process creates more channeling of ions. The channeling of ions creates a more graded (less abrupt) junction.

Embodiments of the invention include open and closed shaped transistors and doped regions. An example of a closed shaped Tx is shown in figure 4A. Other embodiments include 45 degree twist / 45 degree tilt implants. Other embodiment include quadra twist and tilt implants.

With the embodiments of the invention, we can improve breakdown voltage of HV transistor. More graded junction LDD can be obtained without using long diffusion time.

In accordance with the present invention, a standard {001} silicon wafer with a primary notch of <110> direction is used and, before exposure to an image by a lithographic exposure apparatus, the relative relationship between the mask and the {001} silicon wafer is changed so that the relationship, in the same plane, is approximately forty-five degrees (45 degree) from the normal relationship in the same plane. Thus, the [110] crystal direction is aligned approximately 45 degrees to the gate width and will be aligned parallel with channel length direction when voltage is applied to the gate.

This 45 degree change is preferably accomplished by either modifying the mask holder or the wafer holder of an optical lithographic system so the mask holder and the wafer holder are in a relationship of approximately forty-five degrees (45°) from their normal relationship using the <001> crystal direction. The target of the relationship change is exactly 45 degree, because the mobility of the carriers in channel will be optimum when the channel and [110] crystal direction are parallel. However, due to slight imperfection of the lithographic apparatus wafer and mask holders, the change may vary by +- 2% of the 45 degree change. The remaining fabrication steps, such as plasma or anisotropic etching, oxidation, chemical vapor deposition, sputtering and planization, are performed without any modification of the wafer holders, because the exposed surface of the silicon wafer to these processes remains in the <001> direction.

Referring to figure 6, on the same wafer, both standard 0 degree and the embodiments' 45 degree angled channel FETs can be formed. For example, Figure 6 shows both standard 0 degree channel 102 104 FET and the embodiments' 45 degree angled channel 202 204 FETs formed on a wafer (source/drain regions not shown).

Another aspect of the present invention is a novel FET with its gate formed perpendicular to the <100> crystal direction so that the channel will be parallel with this direction with a voltage applied to the gate.

In another aspect of the present invention, annular shaped FETs are formed. Figure 6 shows annual FETs 602 and 612. FET 612 is has the embodiments channel <100> direction. FET 602 has the <110> channel directions. Any combination of

annular and linear FETs with different channel directions can be formed on the same wafer.

The embodiment's <100> channel direction is useful for MOS TX's and can reduce punchthrough.

III. Method of LATID with channel orientated in the <100> or <010>direction

A preferred embodiment of the invention is a method to form a doped region in a semiconductor device. The doped region preferably is a source or drain region in a FET and is more preferably a S or D region in a high voltage transistor such as a LDMOS transistor.

A feature of the process is that a more graded junction is formed by the large angled implant process.

{001} silicon substrate having [110] reference direction

Referring to figure 2A and 2b, an orientation of the channel (C) of an FET is shown. We provide a {001} silicon substrate having [110] reference direction (direction from substrate center to primary notch/flat).

Figure 2A shows a FET with a channel direction 202 in a <100> direction.

Figure 2B shows a FET with a channel direction 204 in a <110> direction.

Devices with both channel directions can be formed on the same wafer.

Gate, Source/ Drain and Channel

Next, a gate (G) is formed over the silicon substrate; the gate having a width and a length; a channel under the gate.

The channel (C) has a channel direction (202 204) parallel with the direction of the gate width. The channel direction is the direction of current flow direction. The channel direction is preferably about [100] or [010] crystal direction.

Large Angle implant with Twist to form Source and Drain

We implant ions into the silicon substrate to form doped regions adjacent to the gate. The orientation of the channel region in the Si crystal structure (channel direction < 100>) in combination with the large angle tilt and twist implant process (describe below) produces doped regions that have a more graded (gradual) junction. The orientation and implant process creates more channeling of ions. The ions are preferably implanted along the <110> direction to maximize channeling. The channeling of ions creates a more graded junction. Channeling is when implanted ions are not slowed by collisions with silicon atoms. It is controlled by three different techniques: wafer tilt, screen oxide layer or preamorphization. This embodiment preferably does not use these techniques to reduce channeling.

When implemented on a HV MOS Tx, the graded junction of the LDD increases the drain breakdown voltage.

Figure 1B shows a schematic view of a twist and tilted ion implant according to the prior art for use in understand the terms "twist" and "tilt".

Tilt is the angle between the wafer surface and the ion beam.

Twist is the angle between the vertical plane containing the ion beam and the vertical plane perpendicular to the reference direction (primary notch direction).

Single Implant at 45 tilt and 45 twist

As shown in figure 3A, the implantation of ions preferably comprises a tilt/twist implant with a twist of about 45 degree from the <110> reference direction (notch) of the crystal substrate and a tilt angle between 40 and 50 degrees (from the normal plane of the substrate surface) and more preferably a tilt angle of 45 degrees with a preferred tolerance of +/- 5 degrees.

For a (001) wafer (e.g., with a notch of <110>) direction, a implant with a 45 tilt and 45 twist, the ions enter the substrate at a <0 -1 -1> (or $<0\bar{1}\bar{1}>$) direction (or [110] group direction). This direction increases the channeling.

The 45 tilt and 45 twist single implant is preferably performed by implanting Ph ions at an energy between 40 and 400 and a dose between 1E12 and 1E15 at tilt angle between 40 and 50 degrees and more preferably about 45 degrees and a twist angle of between 40 and 50 degrees and more preferably 45 degrees.

This 45 degree twist and 45 degree tilt implant preferably forms a (symmetric) LDD.

FET with a Source (S) and Drain (D) and gate (G) with a channel direction of <100>

Figure 3B shows a top down view of a FET with a Source (S) and Drain (D) and gate (G) with a channel direction of <100> and a reference direction < 110> (also for the primary notch).

For a 45 degree twist implant and a 45 degree tilt, the ions are implanted into the S/D region along direction B. Direction B is parallel to the $<0\bar{1}1>$ (or <0 -1 -1>) .

"quadra" implant for open shaped tx

In a preferred embodiment the implanting of ions into further comprises an quadra implant. The quadra implant is performed by 4 implants of Ph ions at an energy between 40 and 400 Kev and a dose between 1E12 and 1E15 ions/sq-cm at tilt angle between 40 and 50 degrees and a twist angles of between 40 and 50 degrees

Figure 3C illustrates the embodiment's quad implant. The 4 implants at 45, 135, 225, and 315 degrees.

In the quadra implant, the implanted ions are aligned in the [0,-1,-1] , [1,0,-1], [0,1,-1] , [-1,0,-1] or <110> directions. (the negative signs represent bars over the 1's, e.g.-1 is equivalent to $\bar{1}$) This maximizes channeling.

Closed shaped (or annual shaped) channel region

Referring to figure 4A and figure 4B, an embodiment is shown where the transistor has a channel region with a "closed shape" so that S/D region on the inside of the channel region and a second doped region surrounding the outside of the channel region.

Figure 4A shows a top down view of a embodiment of a closed shaped transistor (e.g., with annular shaped channel region). Figure 4 shows field oxide regions 402, LDD regions 406 414, source /drain regions 407 415 (see fig 4B) and gate 410. The LLD regions are preferably formed by the embodiment's implant process. The "closed shape" means that the active region has no beginning or end. The channel under the gate 410 is surrounded by the LDD 406. The channel is preferably annular shaped and is more preferably rectangular or square shaped.

Figure 4B shows a cross sectional view of the closed FET shown in figure 4A along the axis 4B according to an embodiment of the invention. Figure 4B show a gate dielectric layer 412 under the gate 410.

The embodiments of the annular channel Tx can be a normal voltage Tx or a offset LDMOS or a Non-offset LDMOS.

Quadra Implant method for closed (e.g., annular) channel region

For the closed shaped doped region, for example as shown in figure 4A, preferably a quadra implant is performed.

HV LDMOS TX with offset transistor and non-offset transistors

The channel orientations and implant embodiments of the invention on can be used to form HV LDMOS TX with offset transistor and non-offset transistors.

Figure 7 shows an example of an offset LDMOS TX. The channel is a diffused p-well for the LDNMOS TX.

In the offset LDMOS TX (figure 7), only the N-LDD is formed using the embodiment's ion implant at [110] to maximize the ion channeling.

In the non- offset LDMOS TX (figure 8), preferably the N+ source and the N+ drain are simultaneously formed in the same implant step using the embodiment's ion implant at [110] to maximize the ion channeling.

Process for offset LDMOS TX (figure 7)

The process to form the OFFset LDMOS TX is as follows:

- form p-epi on substrate
- form p-well
- form (poly) gate
- form N-LDD (using embodiments' channeling maximizing ion implant)
- form spacers on gate
- form source (S) and drain (D) using a standard I/I .

Currently, the offset LDMOS Tx operates at a voltage between about 18V and 60 V. In comparison a normal voltage Tx operates between about 1V to 18V.

non-offset LDMOS TX

Figure 8 shows an example of a non-offset LDMOS TX. Usually we use a lot of diffusion to get a smooth and graded junction between the N+ and p- well. With the embodiment's wafer alignment and drain implant process, a good graded junction can be obtained. The breakdown voltage decreases with the embodiment because of the graded junction.

Process for non-offset LDMOS TX

The process to form the figure 8, non-offset LDMOS TX is as follows:

- form p-epi on substrate
- form p-well
- form poly gate
- form N-LDD (using embodiments' channeling max ion implant)
- form spacers

form N+ source and drain using invention's maximizing channeling ion implant.

Currently, the non-offset LDMOS Tx operates at a voltage between about 12V and 25 V. In comparison a normal voltage Tx operates between about 1V to 18V.

IV. EXAMPLES

The following non-limiting examples represent preferred forms and best modes contemplated by the inventor for practice of his invention, as well as illustrating the results obtained through its use.

High Voltage LDMOS transistor were fabricated using the standard transistor orientation shown in figure 1 and an embodiments orientation shown in figure 2A (e.g., channel in <100> direction). Ph ions were implanted at the conditions shown in the table below to form the N-LDD.

TABLE: comparison of embodiment and standard LDD implants

parameter	**45° tilt and 45°twist implant**	**30° tilt and 0° twist implant**
dose	1E12 atoms/sq-cm	1E12 atoms/sq-cm
energy	80 Kev	80 Kev
Junction depth	0.75μm	0.5 μm
Breakdown voltage	16.2 V	14.0 V

As shown in the table above, the embodiment's 45° tilt and 45°twist LDD implant had a deeper junction depth and a higher breakdown voltage.

The LDD implant on the embodiment's transistor orientation has increased channeling of ion that creates a deeper and more graded junction. The reduces the breakdown voltage. This is important especially on the HV transistor.

Figure 5 shows a plot of the phosphorus concentration of the graded junction N- LDD of the embodiment in a normal V MOS TX compared to a conventional Ph profile. The boron concentration of about 1E18 is the concentration of the p-well. (See e.g., figure 7 and 8.)

V. Ending

In summary, a new set of layout and implantation methods was given in the embodiments of this invention. A purpose is to use crystal structure of silicon to improve the junction or the LDD or S/D to obtain high breakdown voltage. It can be used for DMOS and HVNMOS and other high voltage transistor and normal MOS Transistors.

The embodiments' implant process can be performed on any wafer so that the ions enter the wafer in the [110] direction. The embodiments are not dependents on any configuration of wafer notches and/or flats. The orientation of notches and flat change with wafer technology.

Given the variety of embodiments of the present invention just described, the above description and illustrations show not be taken as limiting the scope of the present invention defined by the claims.

While the invention has been particularly shown and described with reference to the preferred embodiments thereof, it will be understood by those skilled in the art that various changes in form and details may be made without departing from the spirit and scope of the invention. It is intended to cover various modifications and similar arrangements and procedures, and the scope of the appended claims therefore should be accorded the broadest interpretation so as to encompass all such modifications and similar arrangements and procedures.

What is claimed is:

1. A method of fabrication of doped regions in a semiconductor device; comprising the steps of :

a) providing a {001} silicon substrate;

b) forming a gate over said silicon substrate; said gate having a width and a length; a channel under the gate; said channel having a channel direction parallel with the direction of said gate width; said channel direction is [100] or [010] direction;

c) implanting ions into said silicon substrate to form a doped region adjacent to said gate; the implantation of ions comprises a large angle tilt implant with a twist of between about 40 and 50 degrees and a tilt angle of 40 and 50 degrees.

2. The method of claim 1 wherein said doped region is a N- LDD in an offset LDMOS FET.

3. The method claim 1 wherein said ions being implanted about along the [110] directions of the silicon substrate.

4. The method claim 1 wherein the implanting of said ions is performed in one implant step at an about 45 degree twist implant and a tilt angle of about 45 degrees.

5. The method claim 1 wherein said silicon substrate has a notch/flat at a [110] direction.

6. The method claim 1 wherein the implanting of ion further comprises: said silicon substrate has a notch/flat at a <110> direction,

the implantation comprises an implant with a 45 tilt and 45 twist and the ions enter the substrate aligned at a <0 -1 -1> direction whereby the direction increases the channeling.

7. The method claim 1 wherein said channel has an annular shape with a doped region on the inside of said channel and a second doped region surrounding the outside of said channel.

8. The method claim 1 wherein said channel has an annular shape with a doped region on the inside of said channel region and a second doped region surrounding the outside of said channel;

and the implanting of said ions further comprises a quadra implant at the twist angles of about 45, 135, 225 and 315 degrees with a range of +/- 5 degrees; and a tilt angle between 40 and 50 degrees.

9. The method claim 1 wherein said channel has an annular shape with a doped region on the inside of said channel and a second doped region surrounding the outside of said channel region;

and the implanting of said ions further comprises a quadra implant with the ion beams aligned with the <110> direction within plus/minus 2 degrees.

10. The method claim 1 which further includes forming a High Vt NMOS FET from said gate and doped regions.

11. The semiconductor device of claim 1 wherein a LDMOS device is formed.

12. The semiconductor device of claim 1 which further comprises forming a second gate over said silicon substrate; said second gate having a width and a length; a second channel under the second gate; said second channel having a second channel direction parallel with the direction of width of said second gate; said second channel direction is parallel or perpendicular with the <110> direction.

13. A semiconductor device at least one field effect transistor (FET) having a source, drain and gate with the source and drain separated by a channel under the gate, comprising:

a {001} silicon substrate having ;

a gate having a length and a width; said gate having the gate width in the [100] or [010] crystal directions;

a source on one side of said patterned gate width and a drain on the other side of the patterned gate width, with impurities of the source and drain being disposed in the silicon substrate;

a channel under the gate between the source and drain when voltage is applied and being aligned in a direction parallel with the direction of the gate width, whereby the performance of the FET is enhanced.

14. The semiconductor device of claim 13 which further comprises said channel has an annular shape.

15. The semiconductor device of claim 13 which further comprises forming a second gate over said silicon substrate; said second gate having a width and a length; a second channel under the second gate; said second channel having a second channel direction parallel with the direction of width of said second gate; said second channel direction is parallel or perpendicular with the <110> direction.

16. The semiconductor device of claim 13 wherein a LDMOS device is formed.

17. In an integrated circuit with at least one field effect transistor (FET) having a source, drain and gate with the source and drain separated by a channel under the gate, comprising:

a {100} monocrystalline silicon substrate having (100) and (110) crystal planes and [100] and [110] crystal directions;

a FET gate having a length and a width and being insulated from the substrate by a gate dielectric layer, said gate being patterned with the gate width in the [100] crystal direction so that the gate width aligned approximately orthogonal to the (100) crystal plane and parallel with the [100] crystal direction;

a source on one side of said patterned gate width and a drain on the other side of the patterned gate width, and

a channel region being formed under the gate between the source and

drain when voltage is applied and being aligned in a direction parallel with the direction of the gate width.

18. The integrated circuit of claim 17 wherein the said channel has an annular shape with either said source or said drain surrounding the outside of said channel region.

19. The integrated circuit of claim 17 which further comprises forming a second FET over said silicon substrate, said second FET comprised of a second gate over said silicon substrate; said second gate having a width and a length; a second channel under the second gate; said second channel having a second channel direction parallel with the direction of width of said second gate; said second channel direction is parallel or perpendicular with the <110> direction.

20. The integrated circuit of claim 17 wherein said silicon substrate has a notch/flat at a [110] direction.

21. The integrated circuit of claim 17 wherein a LDMOS device is formed.

22. A semiconductor device comprising at least one field effect transistor (FET) having a source, drain and gate with the source and drain separated by an annular channel under the gate, comprising:

a first S/D doped region in a substrate;

a second annular S/D doped region spaced from said first S/D doped region by a channel region in said substrate;

a gate over said annular channel region; said gate has an annular shape;

23. The semiconductor device of claim 24 wherein annular channel and said second annular S/D doped region have a rectangular shape.

24. The semiconductor device of claim 24 wherein said substrate comprises a {001} monocrystalline silicon substrate;

said channel region aligned with or perpendicular with the [110] crystal direction.

25. The semiconductor device of claim 24 wherein said substrate comprises a {001} monocrystalline silicon substrate having [110] reference direction from substrate center to primary notch/flat;

said annular channel region aligned with or perpendicular with the [110] crystal direction.

26. The semiconductor device of claim 24 which further includes a first LLD region adjacent to said gate and said first S/D region; and a second LDD region having an annular shape adjacent to said second annular S/D region.

27. A method for a semiconductor device comprising at least one field effect transistor (FET) having a source, drain and gate with the source and drain separated by an annular channel under the gate, comprising:

a) forming a gate over a substrate; said gate has an annular shape; a annular channel region in said substrate under said gate;

b) forming a first S/D doped region and a second annular S/D doped region in said substrate; said second annular S/D doped region spaced from said first S/D doped region by a channel region in said substrate.

28. The method of claim 27 wherein said annular channel region and said second annular S/D doped region have a rectangular shape.

29. The method of claim 27 wherein said substrate comprises a {001} monocrystalline silicon substrate ;

said channel region aligned with or perpendicular with the [110] crystal direction.

30. The method of claim 27 wherein said substrate comprises a {001} monocrystalline silicon substrate having [110] reference direction from substrate center to primary notch/flat;

said annular channel region aligned with or perpendicular with the [110] crystal direction.

31. The method of claim 27 wherein which further includes a first LLD region adjacent to said gate and said first S/D doped region; and a second LDD region having an annular shape adjacent to said second annular S/D doped region.

32. The method claim 27 wherein said first S/D doped region and said second annualar S/D doped region form by ions being implanted about along the [110] directions of the silicon substrate.

33. The method claim 27 wherein said first S/D doped region and said second annular S/D doped region form by implanting ions in one implant step at an about 45 degree twist implant and a tilt angle of about 45 degrees.

34. The method claim 27 wherein said first S/D doped region and said second annular S/D doped region form by ions being implanted comprising a quadra implant at the twist angles of about 45, 135, 225 and 315 degrees with a range of +/- 5 degrees; and a tilt angle between 40 and 50 degrees.

35. A semiconductor device comprising at least one field effect transistor (FET) having a source, drain and gate with the source and drain separated by a channel under the gate, comprising:

a first annular S/D doped region in a substrate;

a second annular S/D doped region spaced from said first annular first annular S/D doped region by a channel region in said substrate;

said first and said second annular diffusion have a rectangular shape;

a gate over said channel region.

36. The semiconductor device of claim 35 wherein said substrate comprises a {001} monocrystalline silicon substrate;

said channel region aligned with or perpendicular with the [110] crystal direction.

37. The semiconductor device of claim 35 wherein said substrate comprises a {001} monocrystalline silicon substrate having [110] reference direction from substrate center to primary notch/flat;

said channel region aligned with or perpendicular with the [110] crystal direction.

38. A method to form a Offset LDMOS Tx by implanting the N-LDD to increase channeling comprising the steps of:

forming p-epi layer over substrate;

forming a p-well in said p- epi layer;

forming a gate dielectric and a gate over said p- epi layer; said gate having a width and a length; a channel under the gate; said channel having a channel direction parallel with the direction of said gate width; said channel direction is [100] or [010] direction;

forming a drain N-LDD region on one said of said gate; said N- LDD region form by implanting ions into said p-epi layer; the implantation of ions comprises a large angle tilt implant with a twist of between about 40 and 50 degrees and a tilt angle of 40 and 50 degrees.

forming spacers on gate; said spacers extending over said p-epi layer longer in the direction of a subsequently formed source;

forming source and drain region adjacent to said gate.

39. The method claim 38 wherein said channel has an annular shape with a source or drain region on the inside of said channel and said source or drain region surrounding the outside of said channel region.