INTEGRATED CIRCUIT POWER SWITCH CIRCUIT SIZING AND PLACEMENT TECHNIQUE

The present invention generally relates to integrated circuits and more particularly to an improved integrated circuit design and method which utilizes voltage islands in application specific integrated circuit (ASIC) designs that make increasing use of power supply switching techniques to control chip power consumption.

As technology scales for increased circuit density and performance, the need to reduce power consumption increases in significance as designers strive to utilize the advancing silicon capabilities. The consumer product market further drives the need to minimize chip power consumption.

The total power consumed by conventional CMOS circuitry includes active power consumed by circuits as they switch states and either charge or discharge the capacitance associated with the switching nodes. Active power represents the power consumed by the intended work of the circuit to switch signal states and thus execute logic function. This power is not present if the circuit in question is not actively switching. Active power is proportional to the capacitance that is switched, the frequency of operation and to the square of the power supply voltage. Due to technology scaling, the capacitance per unit area increases with each process generation. The power increase represented by this capacitance increase is offset by the scaling of the power supply voltage, Vdd.

The frequency of operation, however, increases with each generation, leading to an overall increase in active power density from technology generation to technology generation. This increasing power density in turn drives the need for more expensive packaging, complex cooling solutions and decreased reliability due to increased temperatures.

Therefore, there is a need for a method and structure that increases performance, while at the same time decreases power consumption. The invention described below satisfies these by providing a solution to the problem of optimum placement of power supply switch circuits.

The invention provides an integrated circuit structure as claimed in claim 1 and corresponding method of claim 6.

The invention will be better understood from the following detailed description of preferred embodiments of the invention with reference to the drawings, in which:

Fig. 1 is an integrated circuit which includes an number of isolated blocks;

Fig. 2 is a power switch circuit incorporated into the integrated circuit wiring;

Fig. 3 shows a series of curves that depicts the relationship between voltage drop and maximum drive distance for various width metal lines;

Fig. 4 shows the translation from drive distance to effective area;

Fig. 5 shows a Voltage Island with Uniform Random Logic Placement;

Figs. 6 and 7 shows the structure which can include a number of logic core areas within the voltage island; and

Fig. 8 is a flowchart showing how the invention matches the size of the power switches to the width of one or more power buses.

The power challenges posed by advanced technologies force system designers to make choices concerning devices, structures and voltage levels for the functions they are designing. In previous generations, large functional blocks were not integrated on the same chip, so these choices could be made independently for each block. High levels of integration supported by system-on-a-chip (SoC) enabling technology drive single chip implementations, where traditional approaches to power distribution and performance optimization fail to provide the flexibility of voltage and technology optimization of the previously disintegrated solution.

Newer technologies divide each semiconductor chip into individual functional blocks (voltage islands) as explained in copending U.S. Patent Application Number 10/065,201 and 10/065,202. These voltage islands of the SoC design can have power characteristics unique from the rest of the design and, with the invention, can be optimized accordingly.

An SoC architecture based on Voltage Islands uses additional design components such as power switches to distribute and manage power. ASIC designs are making increasing use of power supply switching techniques to

control chip power consumption. Thus, power can be conserved by switching off certain voltage islands when they are idle. This invention provides a solution to the problem of optimum placement of such power supply switch circuits.

More specifically, Figure 1 shows an integrated circuit which may include a number of isolated blocks, one of which is labeled "Voltage Island" 10. The power supply of the circuitry within the boundary of the box 10 is isolated from the remainder of the chip and controlled by the power switch circuit 11. For ease of description, this particular example describes the island power coming from a single peripheral I/O cell 12, through the power switch 11, then distributed to all cells within the island. However, a single I/O cell 12, connecting wire 13, and power switch cell 11 has limited current capacity. Thus, to fully exploit the advantages of power supply switching, it is better to use multiple power switch circuits in each voltage island. The following describes a technique for determining the quantity of power switch cells required and their placement for varied voltage island content.

Figure 2 shows a power switch circuit 11 incorporated into integrated circuit wiring. In this example, the highest level of metal shown (Mx) provides unswitched current to the power switch circuit. The power switch 11 supplies switched current to the voltage island via the underlying metal layers, MX-1 and MX-2 in this example. The current capacity of the power switch cell is limited by wire width or the circuit providing the switching function. In either case, each power switch cell has limited current capacity, a portion of which is available on MX-1 and the remainder on MX-2. If the current capacity of the orthogonal metal lines driven by the power switch cell is equivalent, equal current is available on each metal level. If properly designed, current density does not exceed the capacity of the metal wire and voltage drop (voltage drop increases with distance driven) is the limiting factor to how far from the power switch cell a circuit can be driven.

Figure 3 shows a series of curves depicting the relationship between voltage drop and maximum drive distance for a given load of various width metal lines on a single periodicity (illustrated as Wa, Wb and Wc). Wa is the narrowest line and Wc is the widest line in Figure 3. The curves represent a particular power pattern and load, but generally voltage drop increases with distance driven. The invention matches the size of the power switch to provide just the current supported by the power bus width available. Thus, by knowing the wiring length, width and load, the

current and voltage that will be present on the power buses can be calculated. The size of the power switch within the voltage island is selected to match this current and voltage. Matching the power switch circuit size with the power bus width assures that the minimum area overhead is devoted to power switching circuits.

The efficient placement of the power switch cells within a voltage island is dependent on the circuitry within the island. The effective support area of a power switch cell is tightly coupled to the design of the power bus it drives. For regular orthogonal power distribution, the effective support area of a power switch can be approximated as a circle of radius equal to the maximum drive distance shown in Figure 3. Figure 4 shows the translation from maximum drive distance to effective area. One half the dimension of a side of the effective support area is the effective device distance. The relationship is design dependent related to the number of metal levels available for power distribution and their geometric relationship. The invention is applicable to any design style in which the placement of a power switch circuit can be related to a serviceable area.

Figure 5 shows a Voltage Island with Uniform Random Logic Placement and power consumption. First, the embodiment determines the current and voltage drop that will occur on the power buses. From this, the embodiment selects the appropriate size power switch. Next, the embodiment determines the maximum power switch drive distance for the power bus width and distribution as shown above. The embodiment then divides the voltage island area by the power switch serviceable area to determine the number of power switch cells needed. The embodiment evenly distributes the power switch circuits across the voltage island making sure the drive distance does not exceed x or y in Figure 5 (x and y are the maximum power switch serviceable area for the given power bus width and distribution).

In other words, as shown in Figure 8, the embodiment matches the size of the power switches to the width of one or more power buses supplying power to the voltage island 800. The matching process 800 matches the size of the power switches to the current and voltage that will be provided by the power buses. The embodiment then determines the size of the serviceable area to which each of the power switches can provide power 802. The serviceable area is dependent upon power bus current, voltage drop, and distribution. Next, the embodiment places the power switches within the voltage island according to the size of the serviceable area of each of

the power switches 804. More specifically, the embodiment divides the voltage island area by the size of serviceable area to calculate the number of power switches needed.

However, uniform power switch placement is not always possible, such as the case of a large core within an island. For example, Figure 6 shows a voltage island with non- uniform placement having a logic core 60 having dimensions P by Q. First, the embodiment again determines the voltage drop and the switch size 800. Next, the embodiment determines the maximum power switch drive distance (e.g. serviceable area) for the voltage island power bus distribution for the non-core portion 61 of the island 802. The area of the logic core(s) 60 is subtracted from the entire voltage island area to calculate the non-core 61 area. The embodiment then evenly distributes the power switch cells across the non-core area (labeled U in Fig. 6) 804. Again, the embodiment calculates the serviceable area and the number of power switches needed relative to the logic core 60 area (by dividing the logic core area by the power switch serviceable area) 806. The embodiment then allocates (positions, distributes, etc.) this number of power switch circuits evenly along the sides of the core 60, as shown in item 808. More specifically, the power switch circuits for the core area C are positioned along the longer sides of the core 60. This minimizes the distance between the power switches to ensure adequate power supply to all areas of the logic core 60.

If the shorter core dimension P exceeds twice the effective drive distance or if the distance between the power switches is greater than twice the effective drive distance (2x or 2y), additional power switch cells are added to the extent additional power buses are available. An example of such extra power switches Ca are shown in Figure 7. The supported drive distance increases by the proportion of additional power switch cells Ca added. Placement of the additional cells is again along the periphery of the longer side of the logic core, as explained above. This technique can be further supplemented by increasing the power bus width within the core area thereby increasing the size of the power switches and the power switch serviceable area.

The embodiment produces structures shown in Figures 5-7 that include at least one voltage island 10 and a pattern of power switches 11 within the voltage island. The pattern 11 balances the power switches according to the size of the serviceable area to which each of the power switches can provide power. Power buses MX-1, MX-2 are connected to the power switches 11. As explained above, the size of the power switches 11 are matched to

the current and voltage that will be provided by the power buses MX. The size of the serviceable area to which each of the power switches can provide power is dependent upon the size of the power switches and the power bus width. Thus, larger power switches have a larger serviceable area than smaller power switches. As shown above, the number of power switches is equal to the area of the voltage island divided by the size of serviceable area.

As shown in Figures 6 and 7, the structure can include a number of logic core areas (although only one (60) is shown for clarity) within the voltage island. A sub-group of the power switches (C,Ca) is positioned along the periphery of logic core areas. The logic core areas generally comprise rectangles having a longer pair of sides and a shorter pair of sides. The power switches are positioned along the longer sides of the logic core areas to minimize the distance between switches, as explained above.

Thus, as shown above, the embodiment determines the quantity of power switch cells required and provides a technique for analysis and placement to minimize the number of power switch cells. Placement is driven by power bus design and circuit power consumption.

Further, the power switch cells can be distributed unevenly so that different areas (having different power needs) within a given voltage island could be treated separately. Higher densities of power switch cells could be placed in areas of higher power density. This would create an uneven distribution of power switch cells across the voltage island. In the vicinity of cores, placement is along two opposite sides only. In the overall picture, several schemes can be used to evenly distribute power switch cells in localized regions of the voltage island to result in an uneven distribution across the voltage island. Therefore, this allows each area of the voltage island to be treated according to its specific needs, thereby only utilizing power switch cells where needed. This minimizes the number of power switch cells that are used in the design and also reduces power consumption.

CLAIMS

1. An integrated circuit structure comprising:

at least one voltage island; and

a pattern of power switches within said voltage island, wherein said pattern balances said power switches according to the size of the serviceable area to which each of said power switches can provide power, further comprising power buses connected to said power switches, wherein the size of said power switches are matched to the current and voltage that will be provided by said power buses.

2. The structure in claim 1, wherein the size of the serviceable area to which each of said power switches can provide power is dependent upon said size of said power switches.

3. The structure in any preceding claim, wherein the number of power switches is equal to the area of the voltage island divided by said size of serviceable area.

4. The structure in any preceding claim, further comprising logic core areas within said voltage island, wherein a group of said power switches is positioned along the periphery of logic core areas.

5. The structure in claim 4, wherein said logic core areas comprise rectangles having a longer pair of sides and a shorter pair of sides, and wherein said group of power switches is positioned along the longer sides of said logic core areas.

6. A method of positioning power switches in a voltage island of an integrated circuit structure, said method comprising:

matching the size of said power switches to the width of one or more power buses supplying power to said voltage island; and

placing said power switches within said voltage island according to the size of the serviceable area of each of said power switches.

7. The method of claim 6, wherein said matching step matches said size of said power switches to the current and voltage that will be provided by said power buses.

8. The method in claim 6 or 7, wherein said placing process includes allocating a group of said power switches along the periphery of logic core areas within said voltage island.

9. The method in claim 6, 7 or 8, wherein said logic core areas comprise rectangles having a longer pair of sides and a shorter pair of sides, and wherein said allocating of said group of power switches positions said group of power switches along the longer sides of said logic core areas.