ABSTRACT

STACKABLE SEMICONDUCTOR PACKAGE AND WAFER LEVEL FABRICATION METHOD

A stackable semiconductor package includes a semiconductor die, and has a chip sized peripheral outline matching that of the die. In addition to the die, the package includes stacking pads and stacking contacts on opposing sides of the die, and conductive grooves on the edges of the die in electrical communication with the stacking pads and the stacking contacts. The conductive grooves function as interlevel conductors for the package and can also function as edge contacts for the package. The configuration of the stacking pads, of the stacking contacts and of the conductive grooves permit multiple packages to be stacked and electrically interconnected to form stacked assemblies. A method for fabricating the package is performed at the wafer level on a substrate, such as a semiconductor wafer, containing multiple dice. In addition, multiple substrates can be stacked, bonded and singulated to form stacked assemblies that include multiple stacked packages.

FIGURE 1