CLAIMS

1. A field effect transistor, comprising:

a first source/drain on a substrate;

a second source/drain on the substrate;

a channel region between the first source/drain and the second source/drain;

a metal liner on at least three sides of the first source/drain and/or the second source/drain, wherein the metal liner covers less than the full length of a sidewall of the first source/drain and/or the second source/drain, and wherein the metal liner has a width, W_L, on a top surface of the first source/drain and/or the second source/drain that is greater than a width of the underlying source/drain;

a metal-silicide between the metal liner and the first source/drain and/or the second source/drain; and

a conductive contact on the metal liner on the first source/drain and/or the second source/drain, wherein the conductive contact is a conductive material different from a conductive material of the metal liner.

2. The field effect transistor of claim 1, further comprising a gate structure on the channel region, and wherein the metal liner has a thickness in a range of 2 nm to 15 nm.

3. The field effect transistor of claim 2, wherein the metal liner is a conductive silicide forming metal selected from the group consisting of titanium (Ti), nickel (Ni), nickel-platinum (NiPt), and combinations thereof.

4. The field effect transistor of claim 3, wherein the conductive contact is a conductive metal selected from the group consisting of tungsten (W), ruthenium (Ru), Cobalt (Co), copper (Cu), and aluminum (Al), and wherein the conductive contact has a width, W_C, at an interface with a top surface of the metal liner that is less than the width of the metal liner, W_L.

5. The field effect transistor of claim 2, wherein the gate structure includes a gate dielectric layer on the channel region and a conductive gate fill on the gate dielectric layer.

6. The field effect transistor of claim 5, wherein the gate dielectric layer is hafnium oxide (HfO), and the conductive gate fill is a conductive material selected from the group consisting of copper (Cu), Cobalt (Co), tungsten (W), molybdenum (Mo), titanium-aluminum (TiAl), titanium nitride (TiN), tantalum nitride (TaN), tungsten nitride (WN), hafnium nitride (HfN), titanium carbide (TiC), tantalum carbide (TaC), tungsten carbide (WC), hafnium carbide (HfC), titanium aluminum carbide (TiAlC), and combinations thereof.

7. The field effect transistor of claim 5, further comprising one or more nanosheet channel layer(s) between the first source/drain and the second source/drain, wherein the one or more nanosheet channel layer(s) form the channel region.

8. The field effect transistor of claim 7, further comprising an insulating bottom spacer layer between the first source/drain and/or the second source/drain and a portion of the substrate.

9. The field effect transistor of claim 8, further comprising protective blocks between an edge portion of the first source/drain and/or the second source/drain and an isolation region on each of opposite sides of the portion of the substrate below the insulating bottom spacer layer.

10. A field effect transistor, comprising:

a first source/drain on a substrate;

a second source/drain on the substrate;

a channel region between the first source/drain and the second source/drain;

a first metal liner on at least three sides of the first source/drain, wherein the first metal liner covers half (1/2) to nine-tenths (9/10) the length of a sidewall of the first source/drain;

a second metal liner on at least three sides of the second source/drain, wherein the second metal liner covers half (1/2) to nine-tenths (9/10) the length of a sidewall of the second source/drain;

a first metal-silicide layer between the first metal liner and the first source/drain, and a second metal-silicide layer between the second metal liner and the second source/drain, wherein the first source/drain and the second source/drain each have amorphized surfaces adjoining the first metal-silicide layer and second metal-silicide layer;

a first conductive contact on the first metal liner on the first source/drain, wherein the first conductive contact is a conductive material different from the conductive material of the first metal liner;

a second conductive contact on the second metal liner on the second source/drain, wherein the second conductive contact is a conductive material different from the conductive material of the second metal liner; and

a first cover layer on the first metal liner and first conductive contact, wherein a portion of the first cover layer separates the first metal liner and an isolation region on the substrate.

11. The field effect transistor of claim 10, wherein each of the first and second metal-silicide layers have a thickness in a range of 2 nm to 6 nm, and each of the first and second metal liners have a thickness in a range of 3 nm to 12 nm.

12. The field effect transistor of claim 10, further comprising a second cover layer on the second metal liner and second conductive contact, wherein a portion of the second cover layer separates the second metal liner from the isolation region on the substrate.

13. The field effect transistor of claim 10, further comprising an insulating bottom spacer layer between the first source/drain and the second source/drain and a portion of the substrate.

14. The field effect transistor of claim 13, further comprising a protective block adjacent to the insulating

bottom spacer layer and between an edge portion of the first source/drain and the isolation region in the substrate.

15. The field effect transistor of claim 14, further comprising a second cover layer on the second metal liner and second conductive contact, wherein a portion of the second cover layer is between the second metal liner and the isolation region.

16. The field effect transistor of claim 15, wherein a gate structure on the channel region includes a gate dielectric layer on the channel region and a conductive gate fill on the gate dielectric layer.

17. A method of forming a field effect transistor, comprising:

forming a channel region on a substrate;

forming a first source/drain and a second source/drain on opposite sides of the channel region;

amorphizing the surfaces on at least three sides of the first source/drain and the second source/drain by an ion bombardment;

forming a first metal liner on at least three sides of the first source/drain and a second metal liner on at least three sides of the second source/drain;

forming a first metal-silicide layer between the first metal liner and the first source/drain, and a second metal-silicide layer between the second metal liner and the second source/drain;

forming a first cover layer on the first metal liner, wherein a portion of the first cover layer is between the first metal liner and an isolation region on the substrate;

forming a second cover layer on the second metal liner, wherein a portion of the second cover layer is between the second metal liner and the isolation region on the substrate; and

forming a first conductive contact on the first metal liner on the first source/drain and a second conductive contact on the second metal liner on the second source/drain.

18. The method of claim 17, further comprising forming an insulating bottom spacer layer on the substrate, wherein the first source/drain, the channel region, and the second source/drain, are on the insulating bottom spacer layer.

19. The method of claim 18, wherein each of the first and second metal-silicide layers have a thickness in a range of 2 nm to 6 nm, and each of the first and second metal liners have a thickness in a range of 3 nm to 12 nm.

20. The method of claim 19, wherein the first metal liner covers half (1/2) to nine-tenths (9/10) the length of each of the sidewalls of the first source/drain.