

The invention relates to an electrical circuit including a plurality of current-voltage converters whose parameters are dependent in an approximately similar manner on external factors.

An arrangement, whose task is to regulate the current emitted by a plurality of parallel connected current sources which feed a common load, is known from US-PS 4 074 146.

A plurality of current sources are connected in parallel in order to supply a markedly varying load resistance, e.g. a data processing system, with current. The voltage dropped across the load resistance is tapped off and added to a reference voltage in a summing circuit. The output voltage of the summing circuit is amplified in an amplifier whose output is connected to the control inputs of each of the current sources; the output voltage of the amplifier thus serves for regulating each of the current sources. Because the voltage dropped across the load is added to a reference voltage, the load simultaneously acts as a test resistance.

The transfer resistance of a current-voltage converter, referred to hereinafter as an IU converter for brevity, depends on the temperature and other effects. On the one hand, the temperature dependence is particularly pronounced in integrated circuits, because of the large changes in the diffused or implanted resistances. On the other hand, it is frequently necessary to ensure a high stability of the transfer resistance of an IU converter. This applies for example to the integrated circuits of a CD player for motor vehicles which have to be able to function over a temperature range of -20° to $+70^{\circ}$ Celsius and which have to be very stable.

Thus, the object of the invention is to suppress any drift of the transfer resistance in an electrical circuit including a plurality of IU converters.

The invention achieves this object in that, for regulating the transfer resistance of the current-voltage converters at a constant value, one of the current-voltage converters is provided as a reference current-voltage converter whose transfer resistance is compared with a reference resistance in a comparator, that a reference voltage is applied to the comparator and to the reference resistance which is proportional to the transfer resistance of the current-voltage converters and that the output signal of the comparator is supplied to each of the current-voltage converters in such a way that the transfer resistance of the current-voltage converters is regulated at the constant value.

The invention will now be explained with the help of embodiments. In the appertaining drawings,

Figure 1 shows a first embodiment of the invention;

Figure 2 a simple manner of producing the reference current;

Figure 3 the production of the reference current by means of synchronous current sources;

Figure 4 the manner of making the reference voltage symmetrical;

Figure 5a the generation of the current for achieving symmetry;

Figure 5b the generation of the current for achieving symmetry in the reverse direction;

Figure 6 the break-down of the IU converter into an input stage, a control stage and an output stage;

Figure 7 an IU converter using a discretely controlled transfer resistance.

In accordance with Figure 1, an integrated circuit comprises a plurality, but at least two, of IU converters $W_r, W_1, \dots, W_n$. Each IU converter has a current sensitive, preferably low impedance input, an output carrying a voltage and a control input. One of the IU converters is provided as a reference IU converter W_r . A reference current I_{ref} , which is supplied to the input of the reference IU converter W_r , is produced in a reference current source I_q by means of a reference voltage source U_{ref} and a reference resistance R_{ref} . The first input of a comparator V_1 is connected to the output of the reference IU converter W_r and the second input is connected to the reference voltage source U_{ref} . The control inputs of each of the IU converters $W_r, W_1, \dots, W_n$ are connected to the output of the comparator V_1 .

The reference current $I_{ref} = K_1 * U_{ref} / R_{ref}$, where K_1 is a constant factor, is produced in the reference current source I_q . The reference IU converter W_r forms the output voltage $U_r = I_{ref} * R_r$, where R_r is the transfer resistance of the reference IU converter W_r , from the inflowing reference current I_{ref} . The comparator V_1 forms, at least approximately, the output signal $S_a = V * (U_r - K_2 * U_{ref})$, where K_2 is a constant factor and V is the amplification factor. With a sufficiently high amplification factor, $U_r - K_2 * U_{ref} = 0$ in a stable system. Using the above mentioned relationships, there thereby results $R_r = R_{ref} * K_2 / K_1$. As the reference IU converter W_r adopts the transfer resistance $R_r = R_{ref} * K_2 / K_1$ by virtue of the control signal S_a , each of the other IU converters W_1 to W_n are set to

the same transfer resistance $R_1 = R_2 = \dots R_n = R_r$, insofar as they have the same properties as the reference IU converter W_r . The prerequisite for the similarity of all of the IU converters as regards the dependence of individual parameters on external factors can be commensurately easily achieved within an integrated circuit by using a similar type of construction, locating them close together and having low thermal gradients. The stability of the reference voltage U_{ref} is of no consequence since it does not enter into the balancing conditions.

It is illustrated in Figure 2 how the reference current I_{ref} can be produced in a simple manner. The reference resistance R_{ref} is located between the reference voltage source U_{ref} and the input of the reference IU converter W_r . In this arrangement, the potential at the input of the reference IU converter W_r has to be equal to the potential on the earth terminal. If the reference resistance R_{ref} is connected externally, two connections to the integrated circuit are required.

The arrangement illustrated in Figure 3 is more advantageous. A differential amplifier V_d controls two current sources I_{q1} and I_{q2} which are illustrated here in the form of two transistors T_1 and T_2 having emitter resistors R_1 and R_2 . The output of the differential amplifier V_d is connected to the bases of the transistors T_1 and T_2 . The emitter resistors R_1 and R_2 extend to a common supply voltage source U_{b1} . The collector of the first transistor T_1 , which corresponds to the output of the first current source I_{q1} , is connected to the reference resistance R_{ref} and the first input terminal of the differential amplifier V_d . The collector of the second transistor T_2 , which corresponds to the output of the second current source I_{q2} , is connected to the input of the reference IU converter W_r .

The voltage drop across the reference resistance R_{ref} must be equal to the reference voltage U_{ref} with a sufficiently high amplification factor of the differential amplifier V_d . The current necessary for this is delivered by the first current source I_{q1} . The current I_{ref} to the input of the reference IU converter W_r is delivered by the second current source I_{q2} . The current sources I_{q1} , I_{q2} may be dimensioned such that their currents are mutually equal or, something that is advantageous for sensitive IU converters, such that the current I_{ref} amounts to a fraction K_1 of the current through the reference resistance R_{ref} .

A substantially better stability can be achieved by the use of an external reference resistance rather than by using a resistance which is internal to the chip. Moreover, one is then able to balance out individual variations of the signal sources feeding the IU converters by appropriately matching the reference resistance.

In a bipolar integrated circuit, one prefers symmetrical signals. The reference IU converter W_r delivers the output signal U_r to two connection terminals of opposed polarity whereby the in-phase voltages on the two output terminals may be dependent on the temperature or other external factors. Consequently, a comparison of the symmetrical output signal U_r of the reference IU converter W_r with the unsymmetrical reference voltage U_{ref} has to be carried out. In accordance with Figure 4, this can be effected by a differencing stage consisting of two transistors T_3 and T_4 which is fed from a current source I_v whereby the current source I_v is dependent on the reference voltage U_{ref} . An emitter resistor R_3 is connected prior to one of the two transistors. The bases of the transistors T_3 and T_4 are connected to the output terminals of the reference IU converter W_r . The collectors of the transistors T_3 and T_4 are connected to a current mirror S_{sp} . A signal U_v , which is converted into a control signal S_r by an output amplifier for example, is extracted from the output A of the current mirror S_{sp} . The functioning of this part of the comparator V_1 results from the fact that, with a reflection factor of one for the current mirror S_{sp} and, in the balanced state of the control loop, equal currents $I_v/2$ flow through the respective two branches including the transistors T_1 and T_2 and that the voltage U_r therefore has to be equal to the voltage drop U_{r3} across the resistor R_3 .

In accordance with Figure 5, the current I_v is formed by means of the reference voltage U_{ref} . In Figure 5a, there is provided a differential amplifier V_2 whose first input is connected to the one pole of the reference voltage source U_{ref} , whose second input is connected to the one terminal of a reference resistance R_{ref2} and whose output is connected to the base of a current source transistor T_5 . The emitter of the current source transistor T_5 is connected to the second input of the differential amplifier V_2 . The other pole of the reference voltage source U_{ref2} and the other terminal of the reference resistance R_{ref2} are connected to earth or to a reference point.

The voltage drop across the reference resistance R_{ref2} is equal to the reference voltage U_{ref} if the amplification of the differential amplifier V_2 is sufficiently high. Apart from the very low base current, the current extractable at the collector of the current source transistor T_5 then corresponds to the current through the reference resistance R_{ref2} . If greater demands are made, the current source transistor T_5 can be replaced by a Darlington circuit consisting of two transistors. If for example, $R_3 = 2 * R_{ref2}$, then, due to the halving of the current I_v , the voltage drop across R_3 will be equal to the reference voltage U_{ref} . The auxiliary voltage $U_{r3} = U_r$ can be selected arbitrarily in dependence on the ratio of the

resistances. An alteration of the resistances R_{ref2} and R_3 in the same sense would leave the voltage U_r unchanged because only the resistance ratio R_3 / R_{ref2} is relevant. A very low temperature dependency of the integrated circuit is thereby achieved.

The circuit of Figure 5b differs from the circuit of Figure 5a as regards the arrangement of the current source transistor T5 whose collector is connected here to the second input of the differential amplifier V2 whilst its emitter represents the output A_i of the current source. Whereas in Figure 5a, the second input of the differential amplifier V2 is of the inverting type, it has to be non-inverting in Figure 5b. Furthermore, it is illustrated in Figure 5b how one current source can be formed in the reverse direction. To this end, a resistor R_5 is connected between the output A_i and a supply voltage source U_{b2} . The base of a further transistor T6 is connected to the output of the differential amplifier V2. A resistor R_6 is located between the supply voltage source U_{b2} and the emitter of the transistor T6. The output current I_v in the reverse direction is extracted from the collector of the transistor T6 which is referenced as the output A_j .

The object of stabilising a plurality of IU converters but preserving thereby the different transfer resistances, can likewise be fulfilled by the means in accordance with the invention. For this, it is foreseen in accordance with Figure 6, to use a differencing stage having bipolar transistors T7 and T8 acting as a controllable arrangement within the IU converter. The i th IU converter is built-up from an input stage W_{ai} , a differencing stage W_{bi} and an output stage W_{ci} . The input stage W_{ai} converts the input current I_i into a voltage U_{ai} . The differencing stage W_{bi} located between the input stage W_{ai} and the output stage W_{ci} is constructed from two transistors T7 and T8 whose bases are connected to the output of the input stage W_{ai} , whose emitters are connected to a current source I_{bi} and whose collectors are connected to the inputs of the output stage W_{ci} . The output stage W_{ci} forms the output voltage U_i from the collector currents of the differencing stage W_{bi} .

The way in which it works is based on the transconductance of the differencing stage and thus its amplification being proportional to the current of the current source I_{bi} . In order to achieve the result that the i th converter W_i has a transfer resistance which is K times that relating to the reference IU converter W_r , the current I_{bi} must adopt a value which is K times the value of the current I_{br} of the reference IU converter W_r . The circuit means for achieving this are known and thus do not need to be expounded here. The possibility of making the factor K variable and thus controllable is included hereby.

One way of making the transfer resistance discretely controllable and thus programmable is illustrated in Figure 7. A plurality of differencing stages consisting of bipolar transistors T71, T81; T72, T82; T73, T83; ... are connected on their input sides to the input part Wai and to the output part Wci on their output sides. They are fed from the current sources Ib1, Ib2, Ib3, ... which can be switched on and off by the controllable switches S1, S2, S3 ... If the emitter resistors R71, R81; R72, R82; R73, R83; ... are provided for the transistors T71, T81; T72, T82; T73, T83; ... of the differencing stages, the linearity and other properties are improved.

The transconductance of the central part Wbi arises from the sum of the transconductances of the connected differencing stages. As a consequence, the transconductance may be altered in steps by the controllable switches K1, K2, K3, ... It is particularly advantageous to select the currents Ib1, Ib2, Ib3, ... in accordance with a series of powers to the base 2. In the event that emitter resistors are provided, their values have to be assigned inversely. Moreover, it is to be recommended to likewise grade the surface areas of the transistors T71, T81; T72, T82; ... in the ratio of the currents because the greatest accuracy and stability can thereby be achieved.



Claims

1. Electrical circuit including a plurality of current-voltage converters (W_r , W_1 , ..., W_n) whose parameters are dependent in an approximately similar manner on external factors, characterised in that, for regulating the transfer resistance of the current-voltage converters (W_r , W_1 , ..., W_n) at a constant value, one of the current-voltage converters is provided as a reference current-voltage converter (W_r) whose transfer resistance is compared with a reference resistance (R_{ref}) in a comparator (V_1), that a reference voltage (U_{ref}) is applied to the comparator (V_1) and to the reference resistance (R_{ref}) which is proportional to the transfer resistance of the current-voltage converters (W_r , W_1 , ..., W_n) and that the output signal of the comparator (V_1) is supplied to each of the current-voltage converters (W_r , W_1 , ..., W_n) in such a way that the transfer resistance of the current-voltage converters (W_r , W_1 , ..., W_n) is regulated at the constant value.

2. Electrical circuit in accordance with Claim 1, characterised in that, the first input of a first current source (I_q) is connected via the reference resistor (R_{ref}) to earth, that the reference voltage (U_{ref}) is connected to the second input of the first current source (I_q) and to the first input of the comparator (V_1), that the output of the first current source (I_q) is connected to the input of the reference current-voltage converter (W_r), that the output of the reference current-voltage converter (W_r) is connected to the second input of the comparator (V_1) and that the output of the comparator (V_1) is connected to the control inputs of each of the current-voltage converters (W_r , W_1 , ..., W_n).

3. Electrical circuit in accordance with Claim 1, characterised in that, the one pole of the reference voltage source (U_{ref}) is connected to the first input of the comparator (V_1) and via the reference resistance (R_{ref}) to the input of the reference current-voltage converter (W_r), that the output of the reference current-voltage converter (W_r) is connected to the second input of the comparator (V_1) and that the output of the comparator (V_1) is connected to the control inputs of each of the current-voltage converters (W_r , W_1 , ..., W_n).

4. Electrical circuit in accordance with Claim 2, characterised in that, the first input of a first differential amplifier (V_d) is connected via the reference resistance (R_{ref}) to earth, that the reference voltage (U_{ref}) is connected to the second input of the first differential amplifier (V_d), that the output of the first differential amplifier (V_d) controls a second and a third current source (I_{q1} , I_{q2}) and that one of the two current sources delivers the current for the reference current-voltage converter (W_r).



5. Electrical circuit in accordance with Claim 4, characterised in that, the first input of the first differential amplifier (Vd) is connected via the reference resistance (Rref) to earth, that the reference voltage (Uref) is connected to the second input of the first differential amplifier (Vd), that the output of the first differential amplifier (Vd) is connected to the base of a first and second transistor (T1, T2), that the emitter of the first and second transistor (T1, T2) is connected via a respective resistor (R1, R2) to a first supply voltage (Ub1), that the collector of the first transistor (T1) is connected to the first input of the first differential amplifier (Vd) and that the collector of the second transistor (T2) is connected to the input of the reference current-voltage converter (Wr).

6. Electrical circuit in accordance with Claim 4 or 5, characterised in that, the currents of the current sources (Iq1, Iq2) or of the first and second transistor (T1, T2) are selected to be equally great.

7. Electrical circuit in accordance with Claim 4 or 5, characterised in that, the current (Iref) at the input of the reference current-voltage converter (Wr) is selected to be smaller than the current flowing through the reference resistance (Rref).

8. Electrical circuit in accordance with Claim 1, 2, 3, 4, 5, 6 or 7, characterised in that, the comparator (V1) comprises a third current source (Iv) which is controlled by the supplied reference voltage (Uref).

9. Electrical circuit in accordance with Claim 8, characterised in that, the comparator (V1) comprises an asymmetrical differencing stage including a third and fourth transistor (T3, T4), that the bases of the third and fourth transistor (T3, T4) form the second input of the comparator (1), that the emitters of the third and fourth transistor (T3, T4) are connected to the third current source (Iv), whereby a resistor (R3) is connected prior to the emitter of the third or fourth transistor (T3, T4) and that the collectors of the third and fourth transistor (T3, T4) are connected to the input (E) and to the output (A) of a current mirror (Ssp).

10. Electrical circuit in accordance with Claim 8, characterised in that, the third current source (Iv) is constructed in such a way that the one pole of the reference voltage source (Uref) is connected to the non-inverting input of a second differential amplifier (V2), that the inverting input of the second differential amplifier (V2) is connected to the emitter of a fifth transistor (T5) and via a fourth resistor (Rref2) to the other pole of the reference voltage source (Uref) which is



connected to earth, that the base of the fifth transistor (T5) is connected to the output of the second differential amplifier (V2) and that the collector of the fifth transistor (T5) represents the output of the third current source (Iv).

11. Electrical circuit in accordance with Claim 8, characterised in that, the third current source (Iv) is constructed in such a way that the reference voltage source (Uref) is connected to the inverting input of a second differential amplifier (V2), that the non-inverting input of the second differential amplifier (V2) is connected to the collector of a fifth transistor (T5) and via a fourth resistor (Rref2) to the other pole of the reference voltage source (Uref), that the base of the fifth transistor (T5) is connected to the output of the second differential amplifier (V2) and that the emitter of the fifth transistor (T5) represents the output (Ai) of the third current source (Iv).

12. Electrical circuit in accordance with Claim 8, characterised in that, the third current source (Iv) is constructed in such a way that the one pole of the reference voltage source (Uref) is connected to the inverting input of a second differential amplifier (V2) whose non-inverting input is connected to the collector of a fifth transistor (T5) and via a fourth resistor (Rref2) to the other pole of the reference voltage source (Uref), that the output of the second differential amplifier (V2) is connected to the base of the fifth transistor (T5) and of a sixth transistor (T6), that the emitter of the fifth transistor (T5) is connected via a fifth resistor (R5) and the emitter of the sixth transistor (T6) via a sixth resistor (R6) to a second supply voltage source (Ub2) and that the collector of the sixth transistor (T6) represents the output (Aj) of the third current source (Iv).

13. Electrical circuit in accordance with one or more of the preceding Claims, characterised in that, each current-voltage converter (Wr, W1, ..., Wn) is built-up by an input stage (Wai), an output stage (Wci) and a control stage (Wbi) which is located between the input stage (Wai) and the output stage (Wci).

14. Electrical circuit in accordance with Claim 13, characterised in that, the first output of the input stage (Wai) is connected to the base of a seventh transistor (T7) whose collector is connected to the first input of the output stage (Wci), that the second output of the input stage (Wai) is connected to the base of an eighth transistor (T8) whose collector is connected to the second input of the output stage (Wci), that the interconnected emitters of the seventh and eighth transistor (T7, T8) are connected to the one pole of a controllable current source (Ibi) and that the seventh and



eighth transistors (T7, T8) together with the controllable current source (Ib1) form the control stage (Wbi).

15. Electrical circuit in accordance with Claim 14, characterised in that, a plurality of control stages (Wbi) are connected together in parallel, that an emitter resistor (R71, R72, ..., R81, R82, ...) is provided for each transistor (T71, T72, ... T81, T82, ...) and that each controllable current source (Ib1, Ib2, ...) can be connected to the emitter resistors (R71, R72, ..., R81, R82, ...) by means of a controllable switch (S1, S2, ...).

16. Electrical circuit in accordance with Claim 15, characterised in that, the currents of the controllable current sources (Ib1, Ib2, ...) are selected in accordance with a power series to the base 2.

17. Electrical circuit in accordance with Claim 15 or 16, characterised in that, the surface areas of the transistors (T71, T72, ... T81, T82, ...) are graded in the ratio of the currents of the current sources (Ib1, Ib2, ...).