CLAIMS

1. A memory cell (100), comprising:

a first transistor (110), located in a first dielectric layer (120);

a second transistor (130), located in a second dielectric layer (140), wherein the second dielectric layer (140) is located above the first dielectric layer (120), wherein the first transistor (110) and the second transistor (130) each comprise: an active layer (111), wherein a material of the active layer (111) comprises an indium gallium zinc oxide, and the active layer (111) comprises a channel region, and a source and a drain that are respectively located at two sides of the channel region; a gate oxide layer (112), disposed on the active layer (111); and a gate (113), disposed on the gate oxide layer (112), wherein projection of the gate (113) on the active layer (111) covers the channel region; and

a connecting wire (150), located in the first dielectric layer (120) and the second dielectric layer (140), wherein one end of the connecting wire (150) is connected to the gate (113) of the first transistor (110), and the other end is connected to the source or drain of the second transistor (130); and

the first transistor (110) and the second transistor (130) are metal-oxide thin-film transistors, the connecting wire (150) comprises a first contact part (151) and a second contact part (153) that are disposed vertically and a metal wire (152) disposed horizontally; and the first contact part (151) is connected to the gate (113) of the first transistor (110), the second contact part (153) is connected to the source or drain of the second transistor (130), and the metal wire (152) connects the first contact part (151) to the second contact part (153); one end of the metal wire (152) is connected to the end of the first contact part (151) away from the gate (113) of the first transistor (110), and the other end of the metal wire (152) is connected to the end of the second contact part (153) away from the second transistor (130), the first contact part (151) and the second contact part (153) are not aligned vertically.

2. The memory cell (100) according to claim 1, wherein the first transistor (110)

and the second transistor (130) each further comprise a protective layer (114), wherein the protective layer (114) is located at sides of the gate (113) and of the gate oxide layer (112).

3. The memory cell (100) according to claim 1, wherein the first contact part (151) and the metal wire (152) are located in the first dielectric layer (120), and the second contact part (153) is located in the second dielectric layer (140).

4. The memory cell (100) according to claim 1 or 3, wherein a barrier layer (160) is disposed between the first dielectric layer (120) and the second dielectric layer (140), the barrier layer (160) is located on the metal wire (152), and the second contact part (153) is in contact with the metal wire (152) and runs through the barrier layer (160).

5. A memory, comprising:

a base (210), wherein a peripheral circuit (211) is disposed on a surface of the base (210);

a plurality of the memory cells (100) according to any one of claims 1 to 4, located above the peripheral circuit (211); and

a data line (220), configured to connect the peripheral circuit (211) to the plurality of the memory cells (100).

6. The memory according to claim 5, wherein the plurality of the memory cells (100) are arranged in a direction parallel to the base (210) to form a horizontal array; and/or

the plurality of the memory cells (100) are stacked in a direction perpendicular to the base (210) to form a vertical array.

7. The memory according to claim 5, wherein the data line (220) comprises a write word line (223), a write bit line (224), a read word line (221) and a read bit line (222); and

the write word line (223) extends in a first direction and is connected to the gate (113) of the second transistor (130) in each of the plurality of memory cells (100), the write bit line (224) extends in a second direction and is connected to the source or drain of the second transistor (130) in each of the plurality of memory cells (100), and

a joint between the write bit line (224) and the source or drain of the second transistor (130) is different from a joint between the connecting wire (150) and the source or drain of the second transistor (130), the read word line (221) extends in a third direction and is connected to the source or drain of the first transistor (110) in each of the plurality of memory cells (100), the read bit line (222) extends in a fourth direction and is connected to the source or drain of the first transistor (110) in each of the plurality of memory cells (100), and a joint between the read bit line (222) and the source or drain of the first transistor (110) is different from a joint between the read word line (221) and the source or drain of the first transistor (110).

8. The memory according to claim 7, wherein projection of the first direction and projection of the second direction on a surface parallel or perpendicular to the base (210) form a first angle, projection of the third direction and projection of the fourth direction on a surface parallel or perpendicular to the base (210) form a second angle, and neither the first angle nor the second angle is zero.

9. The memory according to claim 5, wherein a peripheral dielectric layer (230) is disposed on the base (210), and the peripheral dielectric layer (230) covers the peripheral circuit (211); and

a peripheral barrier layer (240) is further disposed between the peripheral dielectric layer (230) and the first dielectric layer (120) of the memory cell (100).

10. The memory according to claim 9, wherein the data line (220) runs through the peripheral barrier layer (240) and the peripheral dielectric layer (230), and is connected to the peripheral circuit (211).

11. A method of manufacturing the memory cell (100) according to claim 1, comprising:

forming a first transistor (110) in a first dielectric layer (120), wherein the first transistor (110) is a metal-oxide thin-film transistor;

forming a part of a connecting wire (150) in the first dielectric layer (120), wherein one end of the connecting wire (150) is connected to the first transistor (110);

forming a second dielectric layer (140) on the first dielectric layer (120);

forming another part of the connecting wire (150) in the second dielectric layer

(140), wherein one end of the connecting wire (150) close to the first dielectric layer (120) is connected to the connecting wire (150) formed in the first dielectric layer (120); and

forming a second transistor (130) in the second dielectric layer (140), wherein the second transistor (130) is connected to one end of the connecting wire (150) away from the first dielectric layer (120), and the second transistor (130) is a metal-oxide thin-film transistor.

12. The method of manufacturing a memory cell (100) according to claim 11, wherein the forming a first transistor (110) in a first dielectric layer (120) comprises:

step a: providing a first insulating layer (121);

step b: forming an active layer (111) on the first insulating layer (121), wherein a material of the active layer (111) comprises an indium gallium zinc oxide;

step c: forming a channel region in the active layer (111), and a source and a drain respectively located at two sides of the channel region;

step d: forming a gate oxide layer (112) on the active layer (111), wherein a length of the gate oxide layer (112) is smaller than a length of the active layer (111);

step e: forming a gate (113) on the gate oxide layer (112), wherein projection of the gate (113) on the active layer (111) covers the channel region;

step f: forming a protective layer (114) on the active layer (111), wherein the protective layer (114) wraps sides of the gate (113) and of the gate oxide layer (112); and

step g: forming a second insulating layer covering the active layer (111), the gate oxide layer (112), the gate (113), and the protective layer (114) on the first insulating layer (121), wherein the second insulating layer and the first insulating layer (121) form the first dielectric layer (120).

13. The method of manufacturing a memory cell (100) according to claim 12, wherein the forming a part of a connecting wire (150) in the first dielectric layer (120), wherein one end of the connecting wire (150) is connected to the first transistor (110) comprises:

forming a first contact part (151) and a metal wire (152) connected to the first

contact part (151) in the second insulating layer, wherein the first contact part (151) extends in a vertical direction and is connected to the gate (113) of the first transistor (110), and the metal wire (152) extends in a horizontal direction.

14. The method of manufacturing a memory cell (100) according to claim 13, wherein the forming a second transistor (130) in the second dielectric layer (140) comprises:

forming a third insulating layer (141) on the first dielectric layer (120);

forming an active layer (111) on the third insulating layer (141), wherein a material of the active layer (111) comprises an indium gallium zinc oxide;

repeating steps c to f, to form the second transistor (130) on the third insulating layer (141); and

forming a fourth insulating layer covering the active layer (111), the gate oxide layer (112), the gate (113), and the protective layer (114) on the third insulating layer (141), wherein the fourth insulating layer and the third insulating layer (141) form the second dielectric layer (140).

15. The method of manufacturing a memory cell (100) according to any one of claims 12 to 14, wherein after the first contact part (151) is formed in the second insulating layer and before the second contact part (153) is formed in the second dielectric layer (140), the method further comprises:

forming a barrier layer (160) on the second insulating layer.

16. A method of manufacturing a memory, comprising:

providing a base (210), wherein a peripheral circuit (211) is disposed on a surface of the base (210);

forming a plurality of memory cells (100) sequentially on the base (210), wherein the plurality of the memory cells (100) are arranged in a direction parallel to the base (210) to form a horizontal array; and/or the plurality of the memory cells (100) are stacked in a direction perpendicular to the base (210) to form a vertical array; and the memory cell (100) is obtained by using the method of manufacturing a memory cell (100) according to any one of claims 11 to 15; and

forming a data line (220), wherein the data line (220) is configured to connect the

peripheral circuit (211) to the memory cells (100).

17. The method of manufacturing a memory according to claim 16, wherein the forming a data line (220) comprises:

forming a read word line (221) and a read bit line (222) that are insulated from each other in the first dielectric layer (120), wherein the read word line (221) is configured to be connected to the source or drain of the first transistor (110) in each of the plurality of the memory cells (100), the read bit line (222) is configured to be connected to the source or drain of the first transistor (110) in each of the plurality of the memory cells (100), and a joint between the read bit line (222) and the source or drain of the first transistor (110) is different from a joint between the read word line (221) and the source or drain of the first transistor (110); and

forming a write word line (223) and a write bit line (224) in the second dielectric layer (140), wherein the write word line (223) is configured to be connected to the gate (113) of the second transistor (130) in each of the plurality of the memory cells (100), the write bit line (224) is configured to be connected to the source or drain of the second transistor (130) in each of the plurality of memory cells (100), and a joint between the write bit line (224) and the source or drain of the second transistor (130) is different from a joint between the connecting wire (150) and the source or drain of the second transistor (130).