DESCRIPTION

METHOD OF MANUFACTURING SEMICONDUCTOR DEVICE

TECHNICAL FIELD

The present invention is directed to a semiconductor device manufacturing method, and in particular to a semiconductor device manufacturing method for disposing plural semiconductor substrates having semiconductor chips one above the other, connecting semiconductor chips, each of which constitutes a different semiconductor substrate, in such a manner as to enable signal transmission, and subsequently singularizing the semiconductor chips into individual pieces.

BACKGROUND ART

A reduction in size, thickness and weight of semiconductor application products for use in various mobile apparatuses, such as digital cameras and portable telephones, has progressed at a rapid pace in recent years. In accordance with the trend, there are continuing demands for size reduction and density increase of semiconductor devices installed in the semiconductor application products. To meet such demands, for example, methods of manufacturing semiconductor devices having a wafer-on-wafer (hereinafter, referred to as "WOW") configuration have been proposed. In the WOW configuration, plural semiconductor substrates (wafers) having semiconductor chips are disposed one above the other and bonded in this wafer state.

The following gives a brief description of a conventionally proposed method of manufacturing a semiconductor device having the WOW configuration with

reference to drawings. FIGs. 1A to 1G illustrate a conventional process flow for manufacturing a WOW configuration semiconductor device.

First, in a process shown in FIG. 1A, a semiconductor substrate 110 is prepared. The semiconductor substrate 110 includes a substrate body 120, a semiconductor integrated circuit 130 and via holes 140 which are filled with metal. The semiconductor integrated circuit 130 is formed on the substrate body 120, and the via holes 140 filled with metal are formed in the substrate body 120 and the semiconductor integrated circuit 130. When the semiconductor substrate 110 is prepared, the via holes 140 may be formed in the substrate body 120 prior to the formation of the semiconductor integrated circuit 130, or the semiconductor integrated circuit 130 may be formed on the substrate body 120 prior to the formation of the via holes 140. Note that since the substrate body 120 is reduced in thickness in a process to be described below, the via holes 140 do not have to penetrate the substrate body 120 at this point.

Next in a process shown in FIG. 1B, a support 300 is bonded to the semiconductor substrate 110 on the semiconductor integrated circuit 130 side. A glass substrate, for example, may be used for the support 300. Subsequently, in a process shown in FIG. 1C, the substrate body 120 is reduced in thickness. The thickness reduction is achieved by, for example, polishing a surface of the substrate body 120, on which surface the semiconductor integrated circuit 130 is not formed. The semiconductor substrate 110 and the substrate body 120 after the thickness reduction are referred to as the semiconductor substrate 110a and the substrate body 120a, respectively. The support 300 has a function of supporting the

semiconductor substrate 110a having reduced rigidity after the thickness reduction. Then, bumps (not shown) are formed on the via holes 140 exposed from the surface on which the thickness reduction has been performed. Note that the bumps (not shown) may be formed via electrode pads (not shown).

Next in a process shown in FIG. 1D, a semiconductor substrate 210 is prepared. The semiconductor substrate 210 includes a substrate body 220, a semiconductor integrated circuit 230 and via holes 240 which are filled with metal. The semiconductor integrated circuit 230 is formed on the substrate body 220, and the via holes 240 filled with metal are formed in the substrate body 220 and the semiconductor integrated circuit 230. Bumps (not shown) are formed on the via holes 240 exposed from the surface of the semiconductor substrate 210 on the semiconductor integrated circuit 230 side. Note that the bumps (not shown) may be formed via electrode pads (not shown). Then, the semiconductor substrate 210 is bonded to the semiconductor substrate 110a in such a manner that the semiconductor integrated circuit 230 of the semiconductor substrate 210 opposes the substrate body 120a of the semiconductor substrate 110a. Note that the via holes 240 are formed in advance at positions corresponding to the via holes 140, and each set of the corresponding via holes 240 and 140 are electrically connected via a bump.

Next in a process shown in FIG. 1E, the substrate body 220 is reduced in thickness, in the same manner as in the process of FIG. 1C. The semiconductor substrate 210 and the substrate body 220 after the thickness reduction are referred to as the semiconductor substrate 210a and the substrate body 220a, respectively.

Then, bumps (not shown) are formed on the via holes 240 exposed from the surface on which the thickness reduction has been performed. Note that the bumps (not shown) may be formed via electrode pads (not shown).

Next in a process shown in FIG. 1F, by repeating the same processes of FIGs. 1D and 1E, semiconductor substrates 310a and 410a are disposed one above the other at the bottom of the substrate body 220a of the semiconductor substrate 210a. Then in a process shown in FIG. 1G, the support 300 of FIG. 1F is removed. Herewith, a semiconductor device 100 is completed. In this manner, the WOW-configuration semiconductor device 100 is manufactured in which the semiconductor substrates 110a, 210a, 310a and 410a with reduced thicknesses are bonded to one another in the semiconductor substrate (wafer) state.

FIGs. 2A to 2C illustrate another conventional process flow for manufacturing a WOW configuration semiconductor device. In FIGs. 2A to 2C, the same reference numerals are given to the components which are common in FIGs. 1A to 1G, and their explanations may be omitted. First, in a process shown in FIG. 2A, semiconductor substrates 510 and 610 are prepared. The semiconductor substrate 510 includes a substrate body 520 and a semiconductor integrated circuit 530. The semiconductor integrated circuit 530 is formed on the substrate body 520. The semiconductor substrate 610 includes a substrate body 620 and a semiconductor integrated circuit 630. The semiconductor integrated circuit 630 is formed on the substrate body 620. Then, the semiconductor substrate 610 is bonded to the semiconductor substrate 510 in such a manner that the semiconductor integrated circuit 630 of the semiconductor substrate 610 opposes the semiconductor integrated circuit

530 of the semiconductor substrate 510.

Next in a process shown in FIG. 2B, the substrate body 620 is reduced in thickness. The thickness reduction is achieved by, for example, polishing a surface of the substrate body 620, on which surface the semiconductor integrated circuit 630 is not formed. The semiconductor substrate 610 and the substrate body 620 after the thickness reduction are referred to as the semiconductor substrate 610a and the substrate body 620a, respectively. Subsequently, in a process shown in FIG. 2C, via holes 640 filled with metal are formed in such a manner to penetrate the substrate body 620a and connect the semiconductor integrated circuit 530 and the semiconductor integrated circuit 630. In this manner, a WOW-configuration semiconductor device 500 is manufactured in which the semiconductor substrate 510 and the semiconductor substrate 610a with a reduced thickness are bonded to one another in the semiconductor substrate (wafer) state.

[Prior Art Document]

[Patent Document]

[Patent Document 1] Japanese Laid-open Patent Application Publication No. 2008-153499

DISCLOSURE OF THE INVENTION

PROBLEMS TO BE SOLVED BY THE INVENTION

However, the semiconductor device manufacturing method shown in FIGs. 1A to 1G requires, when two semiconductor substrates are connected, a process of forming bumps on the via holes exposed from both semiconductor substrates, thus leaving the problems of low productivity and an increase in the cost of manufacturing

the semiconductor device.

According to the semiconductor device manufacturing method shown in FIGs. 2A to 2C, since the semiconductor substrates are bonded in such a manner that the surfaces on which the semiconductor integrated circuits have been formed oppose each other, three or more semiconductor substrates cannot be disposed one above the other by simply repeating the same processes. That is, a special process is required to dispose three or more semiconductor substrates one above the other, which results in low productivity and an increase in the cost of manufacturing the semiconductor device.

Also, according to either of the semiconductor device manufacturing methods shown in FIGs. 1A to 1G and FIGs. 2A to 2C, in the case of forming deep via holes, it takes a long time to perform the hole-formation of the via holes and the metal filling process and also the number of materials required for the processes increases, which leads to an increase in the cost of manufacturing the semiconductor device.

Furthermore, according to either of the semiconductor device manufacturing methods shown in FIGs. 1A to 1G and FIGs. 2A to 2C, in the case of forming the via holes by dry etching or the like, the depths of the via holes change according to the size and density of the via holes, which leads to the variation in the diameter of the end portions of the via holes. As a result, the diameter of the via holes exposed when the semiconductor substrate is reduced to a desired thickness varies, which in turn results in the variation in the resistance of the electrical connections, leaving the problem of decreased reliability of the semiconductor device.

In view of the above problems, the present

invention aims at providing a reliable semiconductor device manufacturing method with high productivity, capable of reducing the manufacturing costs.

MEANS FOR SOLVING THE PROBLEMS

In order to achieve the above-described object, the present invention is a semiconductor device manufacturing method for disposing one above another plural semiconductor substrates each having, on the main surface, semiconductor chips each of which has a semiconductor integrated circuit, connecting the semiconductor chips, each of which constitutes a different one of the semiconductor substrates, in such a manner as to enable signal transmission, and subsequently singularizing the semiconductor chips into individual pieces. The semiconductor device manufacturing method includes a first step of preparing a first semiconductor substrate and a second semiconductor substrate; a second step of reducing thickness of the second semiconductor substrate; a third step of firmly fixing an opposite surface of the second semiconductor substrate with a reduced thickness to the main surface of the first semiconductor substrate via an insulating layer, the opposite surface being opposite to the main surface of the second semiconductor substrate; a fourth step of forming, in the second semiconductor substrate with the reduced thickness, a via hole which penetrates from the main surface to the opposite surface of the second semiconductor substrate; and a fifth step of forming a connection part which enables the signal transmission, via the via hole, between the semiconductor chip of the first semiconductor substrate and the semiconductor chip of the second semiconductor substrate.

EFFECTS OF THE INVENTION

According to the present invention, it is possible to provide a reliable semiconductor device manufacturing method with high productivity, capable of reducing the manufacturing costs.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1A illustrates a first process of a manufacturing process flow of a conventional WOW-configuration semiconductor device;

FIG. 1B illustrates a second process of the manufacturing process flow of the conventional WOW-configuration semiconductor device;

FIG. 1C illustrates a third process of the manufacturing process flow of the conventional WOW-configuration semiconductor device;

FIG. 1D illustrates a fourth process of the manufacturing process flow of the conventional WOW-configuration semiconductor device;

FIG. 1E illustrates a fifth process of the manufacturing process flow of the conventional WOW-configuration semiconductor device;

FIG. 1F illustrates a sixth process of the manufacturing process flow of the conventional WOW-configuration semiconductor device;

FIG. 1G illustrates a seventh process of the manufacturing process flow of the conventional WOW-configuration semiconductor device;

FIG. 2A illustrates a first process of another manufacturing process of a conventional WOW-configuration semiconductor device;

FIG. 2B illustrates a second process of the

other manufacturing process of the conventional WOW-configuration semiconductor device;

FIG. 2C illustrates a third process of the other manufacturing process of the conventional WOW-configuration semiconductor device;

FIG. 3 is a cross-sectional view illustrating a semiconductor device according to a first embodiment of the present invention;

FIG. 4A illustrates a first process of a manufacturing process flow of the semiconductor device according to the first embodiment of the present invention;

FIG. 4B illustrates a second process of the manufacturing process flow of the semiconductor device according to the first embodiment of the present invention;

FIG. 4C illustrates a third process of the manufacturing process flow of the semiconductor device according to the first embodiment of the present invention;

FIG. 4D illustrates a fourth process of the manufacturing process flow of the semiconductor device according to the first embodiment of the present invention;

FIG. 4E illustrates a fifth process of the manufacturing process flow of the semiconductor device according to the first embodiment of the present invention;

FIG. 4F illustrates a sixth process of the manufacturing process flow of the semiconductor device according to the first embodiment of the present invention;

FIG. 4G illustrates a seventh process of the

manufacturing process flow of the semiconductor device according to the first embodiment of the present invention;

FIG. 4H illustrates an eighth process of the manufacturing process flow of the semiconductor device according to the first embodiment of the present invention;

FIG. 4I illustrates a ninth process of the manufacturing process flow of the semiconductor device according to the first embodiment of the present invention;

FIG. 4J illustrates a tenth process of the manufacturing process flow of the semiconductor device according to the first embodiment of the present invention;

FIG. 4K illustrates an eleventh process of the manufacturing process flow of the semiconductor device according to the first embodiment of the present invention;

FIG. 4L illustrates a twelfth process of the manufacturing process flow of the semiconductor device according to the first embodiment of the present invention;

FIG. 4M illustrates a thirteenth process of the manufacturing process flow of the semiconductor device according to the first embodiment of the present invention;

FIG. 4N illustrates a fourteenth process of the manufacturing process flow of the semiconductor device according to the first embodiment of the present invention;

FIG. 4O illustrates a fifteenth process of the manufacturing process flow of the semiconductor device

according to the first embodiment of the present invention;

FIG. 4P illustrates a sixteenth process of the manufacturing process flow of the semiconductor device according to the first embodiment of the present invention;

FIG. 4Q illustrates a seventeenth process of the manufacturing process flow of the semiconductor device according to the first embodiment of the present invention;

FIG. 4R illustrates an eighteenth process of the manufacturing process flow of the semiconductor device according to the first embodiment of the present invention;

FIG. 4S illustrates a nineteenth process of the manufacturing process flow of the semiconductor device according to the first embodiment of the present invention;

FIG. 4T illustrates a twentieth process of the manufacturing process flow of the semiconductor device according to the first embodiment of the present invention;

FIG. 5A illustrates a first process of a manufacturing process flow of a semiconductor device according to a modification of the first embodiment of the present invention;

FIG. 5B illustrates a second process of the manufacturing process flow of the semiconductor device according to the modification of the first embodiment of the present invention;

FIG. 5C illustrates a third process of the manufacturing process flow of the semiconductor device according to the modification of the first embodiment of

the present invention;

FIG. 5D illustrates a fourth process of the manufacturing process flow of the semiconductor device according to the modification of the first embodiment of the present invention;

FIG. 6 is a cross-sectional view illustrating a semiconductor device according to a second embodiment of the present invention;

FIG. 7A illustrates a first process of a manufacturing process flow of the semiconductor device according to the second embodiment of the present invention;

FIG. 7B illustrates a second process of the manufacturing process flow of the semiconductor device according to the second embodiment of the present invention;

FIG. 7C illustrates a third process of the manufacturing process flow of the semiconductor device according to the second embodiment of the present invention;

FIG. 7D illustrates a fourth process of the manufacturing process flow of the semiconductor device according to the second embodiment of the present invention;

FIG. 7E illustrates a fifth process of the manufacturing process flow of the semiconductor device according to the second embodiment of the present invention;

FIG. 7F illustrates a sixth process of the manufacturing process flow of the semiconductor device according to the second embodiment of the present invention;

FIG. 8 is a cross-sectional view illustrating a

semiconductor device according to a third embodiment of the present invention;

FIG. 9A illustrates a first process of a manufacturing process flow of the semiconductor device according to the third embodiment of the present invention;

FIG. 9B illustrates a second process of the manufacturing process flow of the semiconductor device according to the third embodiment of the present invention;

FIG. 9C illustrates a third process of the manufacturing process flow of the semiconductor device according to the third embodiment of the present invention;

FIG. 9D illustrates a fourth process of the manufacturing process flow of the semiconductor device according to the third embodiment of the present invention;

FIG. 9E illustrates a fifth process of the manufacturing process flow of the semiconductor device according to the third embodiment of the present invention;

FIG. 9F illustrates a sixth process of the manufacturing process flow of the semiconductor device according to the third embodiment of the present invention;

FIG. 10 is a cross-sectional view illustrating a semiconductor device according to a fourth embodiment of the present invention;

FIG. 11A illustrates a first process of a manufacturing process flow of the semiconductor device according to the fourth embodiment of the present invention;

FIG. 11B illustrates a second process of the manufacturing process flow of the semiconductor device according to the fourth embodiment of the present invention;

FIG. 11C illustrates a third process of the manufacturing process flow of the semiconductor device according to the fourth embodiment of the present invention;

FIG. 11D illustrates a fourth process of the manufacturing process flow of the semiconductor device according to the fourth embodiment of the present invention;

FIG. 11E illustrates a fifth process of the manufacturing process flow of the semiconductor device according to the fourth embodiment of the present invention;

FIG. 11F illustrates a sixth process of the manufacturing process flow of the semiconductor device according to the fourth embodiment of the present invention;

FIG. 11G illustrates a seventh process of the manufacturing process flow of the semiconductor device according to the fourth embodiment of the present invention;

FIG. 11H illustrates an eighth process of the manufacturing process flow of the semiconductor device according to the fourth embodiment of the present invention;

FIG. 12 is a cross-sectional view illustrating a semiconductor device according to a fifth embodiment of the present invention; and

FIG. 13 is a flowchart showing an example of an entire manufacturing process flow of a semiconductor

device, including WOW processes and widely-recognized semiconductor device manufacturing processes.

DESCRIPTION OF EMBODIMENT

Embodiments that describe the best mode for carrying out the present invention are explained next with reference to the drawings.

[First Embodiment]

[Configuration Of Semiconductor Device According To First Embodiment Of The Present Invention]

First is described the configuration of a semiconductor device according to a first embodiment of the present invention. FIG. 3 is a cross-sectional view illustrating a semiconductor device according to the first embodiment of the present invention. With reference to FIG. 3, a semiconductor device 10 according to the first embodiment of the present invention has a configuration in which semiconductor substrates 11c, 21c, 31c, 41c, 51c, 61c and 71c are disposed one above the other. The semiconductor device 10 is, for example, a CMOS LSI, a memory device, a sensor device or a MEMS.

The semiconductor substrates 11c-71c constituting the semiconductor device 10 are, for example, silicon wafers. In the case where the semiconductor substrate 11c-71c are silicon wafers, the semiconductor device 10 is a so-called WOW-configuration semiconductor device in which plural semiconductor substrates (wafers) are bonded to one another in the semiconductor substrate (wafer) state.

The semiconductor substrates 11c-71c include plural regions A in which semiconductor chips are formed (hereinafter, referred to as the "semiconductor chip formation regions A") and a scribing region B for

separating the plural semiconductor chip formation regions A. The reference symbol C indicates a position at which, on the semiconductor device 10, cutting is performed using a dicing blade or the like (hereinafter, the "cutting position C"). The semiconductor device 10 is cut into individual pieces at the cutting positions C using a dicing blade or the like to thereby form final products.

Each semiconductor chip formation region A of the semiconductor substrates 11c-71c includes, respectively, a substrate body 12-72 (not shown), a semiconductor integrated circuit 13-73 (not shown) and electrode pads 15-75. The substrate bodies 12-72 (not shown) are made, for example, of silicon. Each of the semiconductor integrated circuits 13-73 (not shown) has a configuration in which a diffusion layer (not shown), an insulating layer (not shown), via holes (not shown), a wiring layer (not shown) and the like are formed in silicon, for example, and is formed on one surface of the corresponding substrate body 12-72 (not shown). In the following description, the surface of each of the semiconductor substrates 11c-71c, on which surface the semiconductor integrated circuit 13-73 (not shown) is provided may be referred to as the "main surface".

The electrode pads 15-75 are disposed on the corresponding semiconductor integrated circuits 13-73 (not shown), respectively, via the insulating layer (not shown). The electrode pads 15-75 are electrically connected to the corresponding wiring layer (not shown) provided in the semiconductor integrated circuit 13-73 (not shown). As each of the electrode pads 15-75, a laminated body or the like may be used, in which an Au layer is disposed on a Ti layer, for example. Or, the following may also be used as the electrode pad 15-75: a laminated body in which an Au

layer is disposed on a Ni layer; a laminated body in which a Pd layer and an Au layer are sequentially disposed on a Ni layer; a laminated body in which a Cu layer or an Al layer is disposed on a layer of a high melting point metal, such as Co, Ta, Ti and TiN, in place of Ni; or a damascene interconnect structure.

The semiconductor substrates 11c and 21c are bonded to one another via a resin layer 16, and the electrode pads 15 of the semiconductor substrate 11c and the electrode pads 25 of the semiconductor substrate 21c are electrically connected to each other via metal layers 38 formed in via holes 21y. The semiconductor substrates 21c and 31c are bonded to one another via a resin layer 26, and the electrode pads 25 of the semiconductor substrate 21c and the electrode pads 35 of the semiconductor substrate 31c are electrically connected to each other via metal layers 48 formed in via holes 31y. Note that each via hole is a connecting hole provided to connect semiconductor substrates (not limited to adjacent semiconductor substrates), and connects the semiconductor substrates to enable signal transmission between them when a metal layer, an optical waveguide or the like is formed inside the via hole. The metal layer, the optical waveguide or the like formed inside the via hole may be referred to as the "connection part".

The semiconductor substrates 31c and 41c are bonded to one another via a resin layer 36, and the electrode pads 35 of the semiconductor substrate 31c and the electrode pads 45 of the semiconductor substrate 41c are electrically connected to each other via metal layers 58 formed in via holes 41y. The semiconductor substrates 41c and 51c are bonded to one another via a resin layer 46, and the electrode pads 45 of the semiconductor substrate

41c and the electrode pads 55 of the semiconductor substrate 51c are electrically connected to each other via metal layers 68 formed in via holes 51y.

The semiconductor substrates 51c and 61c are bonded to one another via a resin layer 56, and the electrode pads 55 of the semiconductor substrate 51c and the electrode pads 65 of the semiconductor substrate 61c are electrically connected to each other via metal layers 78 formed in via holes 61y. The semiconductor substrates 61c and 71c are bonded to one another via a resin layer 66, and the electrode pads 65 of the semiconductor substrate 61c and the electrode pads 75 of the semiconductor substrate 71c are electrically connected to each other via metal layers 88 formed in via holes 71y.

In the semiconductor substrate 71c, a solder mask layer 76 having openings 76x is formed, and external connection terminals 91 are formed inside the openings 76x. The external connection terminals 91 are provided to electrically connect the semiconductor device 10 and a wiring substrate or the like provided outside the semiconductor device 10, and are connected to the electrode pads 75. As the external connection terminals 91, solder balls, Au bumps, a conductive paste or the like may be used. In the case when solder balls are used as the external connection terminals 91, an alloy containing Pb, an alloy of Sn and Cu, an alloy of Sn and Ag, an alloy of Sn, Ag and Cu or the like may be used as a material of the external connection terminals 91.

[Processes For Manufacturing Semiconductor Device According To First Embodiment Of The Present Invention]

Next is described a manufacturing process flow of the semiconductor device according to the first embodiment of the present invention. FIGs. 4A to 4T

illustrate the manufacturing process flow of the semiconductor device according to the first embodiment of the present invention. In FIGs. 4A to 4T, the same reference numerals are given to the components which are common to the semiconductor device 10 shown in FIG. 3, and their explanations may be omitted.

First, a semiconductor substrate 11 shown in FIGs. 4A and 4B is prepared. FIG. 4A is a plan view and FIG. 4B is a cross-sectional view. With reference to FIGs. 4A and 4B, the semiconductor substrate 11 includes the substrate body 12, the semiconductor integrated circuit 13 and the electrode pads 15. Note that, in FIG. 4A, the electrode pads 15 are not shown. In FIG. 4B, the reference numeral 11a denotes one surface of the semiconductor substrate 11 (the surface on which the electrode pads 15 are formed, i.e., the main surface), and the reference numeral 11b denotes the other surface of the semiconductor substrate 11 (i.e., the surface opposite to the main surface).

The substrate body 12 is made, for example, of silicon. The semiconductor integrated circuit 13 has, for example, a configuration in which a diffusion layer (not shown), an insulating layer (not shown), via holes (not shown), a wiring layer (not shown) and the like are formed in silicon. The electrode pads 15 are formed on the semiconductor integrated circuit 13 via the insulating layer (not shown). As each of the electrode pads 15, a laminated body or the like may be used, in which an Au layer is disposed on a Ti layer, for example. Or, the following may also be used as the electrode pad 15: a laminated body in which an Au layer is disposed on a Ni layer; a laminated body in which a Pd layer and an Au layer are sequentially disposed on a Ni layer; a laminated

body in which a Cu layer or an Al layer is disposed on a layer of a high melting point metal, such as Co, Ta, Ti and TiN, in place of Ni; or a damascene interconnect structure.

The semiconductor substrate 11 includes plural semiconductor chip formation regions A and a scribing region B for separating the plural semiconductor chip formation regions A. The reference symbol C indicates a position at which, on the semiconductor substrate 11, cutting is performed using a dicing blade or the like (hereinafter, referred to as the "cutting position C"). A diameter φ1 of the semiconductor substrate 11 is, for example, 6 inches (about 150 mm), 8 inches (about 200 mm) or 12 inches (about 300 mm). A thickness T1 of the semiconductor substrate 11 is, for example, 0.625 mm (when φ1 = 6 inches), 0.725 mm (when φ1 = 8 inches) and 0.775 mm (when φ1 = 12 inches). In the present embodiment, the following description is given with an example in which an 8-inch-diameter (about 200 mm in diameter) silicon wafer is used as the semiconductor substrate 11.

Subsequently, in a process shown in FIG. 4C, a fringe portion 11x of the semiconductor substrate 11 shown in FIGs. 4A and 4B is removed. The semiconductor substrate 11 after the fringe portion 11x is removed is referred to as the semiconductor substrate 11c. The removal of the fringe portion 11x is performed by grinding with a grinder or the like in such a manner that the semiconductor substrate 11c after the removal of the fringe portion 11x has, for example, a circular shape in a planar view. In this operation, dry polishing, wet etching or the like may also be used in combination.

The dry polishing here is a processing method in which a surface is ground down (polished) using abrasive

cloth formed by hardening fibers containing silica, for example. The wet etching is a processing method in which etching is performed by supplying fluoro-nitric acid or the like while the semiconductor substrate 11 is rotated using a spinner, for example. In the case where the semiconductor substrate 11c after the removal of the fringe portion 11x has a circular shape in a planar view, a diameter φ2 of the semiconductor substrate 11c having a circular shape in a planar view is, for example, 193.0 ± 0.1 mm. That is, the semiconductor substrate 11 whose diameter φ1 is 8 inches (about 200 mm) is reduced in diameter to form the semiconductor substrate 11c with the diameter φ2 of 193.0 ± 0.1 mm.

Next in a process shown in FIG. 4D, the resin layer 16 is formed on the surface 11a of the semiconductor substrate 11c. A resin mainly composed of, for example, benzocyclobutene (BCB) may be used as a material of the resin layer 16. Alternatively, an epoxide-based resin, an acrylic-based resin, a polyimide-based resin or the like may be used as a material of the resin layer 16. A thickness T2 of the resin layer 16 is, for example, about 5 μm. The resin layer 16 may be formed by applying a resin mainly composed of, for example, benzocyclobutene (BCB) to the surface 11a of the semiconductor substrate 11c using, for example, spin-coating technique. Subsequently, the resin layer 16 is prebaked at 140 °C, for example, to be semi-hardened. The semi-hardened resin layer 16 has adhesiveness. Note that the resin layer 16 may be formed by a vapor-phase growth method or by attaching a film resin, instead of using spin-coating technique.

In the process shown in FIG. 4D, it is preferable that, when the surface 11b of the semiconductor

substrate 11c is used as a reference plane, a surface 16a of the resin layer 16 be parallel to the reference plane. If the surface 16a of the resin layer 16 is not parallel to the reference plane, for example, the via holes 21y are formed at an angle in a process shown in FIG. 4I to be described below, and the metal layers 38 or the like are formed in the slanted via holes 21y. This may result in the problem of decreased reliability of the connection between adjacent semiconductor substrates. Note that being parallel in this case means that the variation in a height H1 of the surface 16a of the resin layer 16 with respect to the reference plane is 1 μm or less. Accordingly, it is preferable to have a process of checking the variation in the height H1 after the formation of the resin layer 16. In the case where the variation in the height H1 is more than 1 μm, it is preferable to have a process of adjusting the surface 16a of the resin layer 16 to make the variation in the height H1 within 1 μm. The surface 16a of the resin layer 16 may be processed (ground) by, for example, a CMP method.

When n semiconductor substrates have already been disposed one above the other and a resin layer is then formed on the topmost (the n^{th} layer) semiconductor substrate, the back surface of the lowermost semiconductor substrate (the surface on which no devices are formed) is used as a reference plane. In this case, it is preferable that the top surface of the resin layer be parallel to the reference plane. Note that being parallel in this case means that the variation in the height of the top surface of the resin layer with respect to the reference plane is $(1 \times n)$ μm or less. That is, as described above, in the case when a resin layer is formed on a single semiconductor substrate, the variation in the height of

the top surface of the resin layer with respect to the reference plane is preferably 1 × 1 = 1 μm or less, and in the case when a resin layer is formed on semiconductor substrates of, for example, ten layers, the variation in the height of the top surface of the resin layer with respect to the reference plane (the back surface of the lowermost semiconductor substrate) is preferably 1 × 10 = 10 μm or less.

Next in a process shown in FIG. 4E, a semiconductor substrate 21, which has a configuration the same as that of the semiconductor substrate 11 of FIGs. 4A and 4B, is prepared. In FIG. 4E, the reference numeral 21a denotes one surface of the semiconductor substrate 21 (the surface on which the electrode pads 25 are formed, i.e., the main surface), and the reference numeral 21b denotes the other surface of the semiconductor substrate 21 (i.e., the surface opposite to the main surface). The semiconductor substrate 21 includes a substrate body 22, a semiconductor integrated circuit 23 and the electrode pads 25. Details about the semiconductor substrate 21 are the same as those of the semiconductor substrate 11, and the explanation is therefore omitted.

Subsequently, a depression 21x is formed on the surface 21b side of the prepared semiconductor substrate 21. The semiconductor substrate 21 after the formation of the depression 21x is referred to as the semiconductor substrate 21c. The depression 21x is formed, for example, in such a manner as to reduce the thickness of the central portion and its vicinity (an area including the plural semiconductor chip formation regions A) while leaving the fringe portion of the semiconductor substrate 21 (an area excluding the plural semiconductor chip formation regions A). The depression 21x is formed, for example, by

grinding the surface 21b of the semiconductor substrate 21 using a grinder or the like. In this operation, dry polishing, wet etching or the like may also be used in combination.

The depression 21x has, for example, a circular shape in a planar view; however, it may have a shape other than circular. In the case where the depression 21x has a circular shape in a planar view, a diameter φ3 of the depression 21x having a circular shape in a planar view is, for example, 195.2 ± 0.1 mm. A thickness T3 of the area with a reduced thickness in the semiconductor substrate 21c is in the range of about 1 μm to about 100 μm, for example; however, in terms of strength, the thickness T3 is preferably in the range of about 10 μm to about 50 μm. This is because setting the thickness T3 of the area with a reduced thickness to about 10 μm to about 50 μm reduces breakage due to mechanical vibrations or the like and stress exerted on the semiconductor chips. Note that the lateral side of the depression 21x does not necessarily have to be perpendicular to the bottom surface of the depression 21x.

The reason for the thickness T3 of the area with a reduced thickness in the semiconductor substrate 21c being 1 μm or more is as follows. It is considered that, in order to prevent a defect or contamination having occurred on the back surface of the semiconductor substrate 21c (the surface on which no devices are formed) from spreading to devices, such as transistors, in the semiconductor integrated circuit 23, the thickness T3 of the area with a reduced thickness in the semiconductor substrate 21c needs to be at least five times or more the depth of element isolation (not shown) in the devices. Here, the depth of element isolation (not shown) in the

devices in the semiconductor integrated circuit 23 is in the range of about 200 nm to about 500 nm. Accordingly, the thickness T3 of the area with a reduced thickness in the semiconductor substrate 21c needs to be at least 1 μm, which is five times the minimum value of the depth of element isolation, 200 nm.

Thus, by forming the depression 21x in such a manner as to reduce the thickness of the central portion and its vicinity (the area including the plural semiconductor chip formation regions A) while leaving the fringe portion of the semiconductor substrate 21 (the area excluding the plural semiconductor chip formation regions A), the semiconductor substrate 21c after the formation of the depression 21x maintains sufficient rigidity. Accordingly, the method for manufacturing the semiconductor device according to the first embodiment of the present invention does not need to employ a support having a function of supporting the semiconductor substrate 21c, as described in the section of Background Art, and the semiconductor substrate 21c with a reduced thickness can be treated in the same manner as the semiconductor substrate 21 before the thickness reduction. This eliminates the need for the processes of bonding and removing the support to/from the semiconductor substrate, which processes are not usual wafer processes of a semiconductor device. As a result, it is possible to improve the productivity.

Next in a process shown in FIG. 4F, the semiconductor substrate 11c is bonded to the depression 21x of the semiconductor substrate 21c. First, the semiconductor substrate 11c is disposed in such a manner that the resin layer 16 formed on the surface 11a of the semiconductor substrate 11c comes in contact with the

bottom surface of the depression 21x of the semiconductor substrate 21c. Alignment marks for enabling highly accurate positioning are provided in advance in, for example, the scribing regions B of the semiconductor substrates 11c and 21c. The positioning of the semiconductor substrate 11c may be achieved by a well-recognized method using the alignment marks as a reference. The alignment accuracy is, for example, 2 μm or less.

Note that a certain amount of gap is formed between the lateral side of the depression 21x of the semiconductor substrate 21c and the lateral side of the semiconductor substrate 11c. In the case where both the depression 21x of the semiconductor substrate 21c and the semiconductor substrate 11c have, for example, a circular shape in a planar view, the gap in the shape of a circular ring is formed. Subsequently, while the structure shown in FIG. 4F is being heated at, for example, 250 °C, the semiconductor substrate 11c is pressed from the surface 11b side to thereby cause the resin layer 16 formed on the surface 11a of the semiconductor substrate 11c to be press-bonded to the bottom surface of the depression 21x of the semiconductor substrate 21c. Herewith, the resin layer 16 becomes hardened, and the semiconductor substrate 11c is bonded in the depression 21x to the semiconductor substrate 21c. The heating operation may be performed at 300 °C; however, the temperature is preferably 200 °C or less. If the operation is performed at the temperature as high as 300 °C, stress occurs due to a difference in the thermal expansion, which can cause separation and/or breakage of the semiconductor substrates. Such separation and breakage becomes more likely as the number of laminated layers increases.

Next in a process shown in FIG. 4G, a

photosensitive resist film 27 is formed in such a manner as to cover the surface 21a of the semiconductor substrate 21c. The resist film 27 is formed, for example, by applying a liquid resist to the surface 21a of the semiconductor substrate 21c. The thickness of the resist film 27 is 10 μm, for example.

Next in a process shown in FIG. 4H, the resist film 27 of FIG. 4G is exposed via a predetermined mask, and the exposed resist film 27 is subsequently developed, thereby forming an opening 27x in the resist film 27. Note that for convenience of explanation, FIGs. 4H to 4S show enlarged views of a part of the structure shown in FIG. 4G (i.e., the electrode pads 15 and 25 and their vicinity). The reference numerals 14 and 24 of FIG. 4H denote insulating layers provided on the semiconductor integrated circuits 13 and 23, respectively, which insulating layers are not shown in FIGs. 4A to 4G. The insulating layers 14 and 24 are made of, for example, Si_3N_4 or SiO_2. The thickness of each of the insulating layers 14 and 24 is in the range of, for example, 0.1 μm to 2.0 μm so as to achieve electrical insulation between the semiconductor integrated circuits 13 and 23.

Next in a process shown in FIG. 4I, the via hole 21y is formed in the semiconductor substrate 21c. The via hole 21y is formed in such a manner to penetrate the resin layer 16 and a part of the semiconductor substrate 21c (the substrate body 22, the semiconductor integrated circuit 23, the insulating layer 24 and the electrode pad 25) corresponding to the opening 27x so that the electrode pad 15 of the semiconductor substrate 11c is exposed. The via hole 21y is formed by, for example, dry etching. The via hole 21y has, for example, a circular shape in a planar view, and has a diameter φ4 of, for example, 1 μm

to 30 μm. Note however that the diameter φ4 of the via hole 21y is preferably set to a value which allows the via hole 21y to have an aspect ratio (= depth D1/diameter φ4) between 0.5 and 5 inclusive. This is because by setting the diameter φ4 of the via hole 21y to a value which allows the via hole 21y to have an aspect ratio (= depth D1/diameter φ4) between 0.5 and 5 inclusive, it is possible to achieve, for example, an improvement in the etching speed (throughput) for forming the via hole 21y and an improvement of the ease of forming the metal layer 38 in the via hole 21y.

Next in a process shown in FIG. 4J, the resist film 27 of FIG. 4I is removed. Then, in a process shown in FIG. 4K, an insulating layer 28 is formed in such a manner as to cover the top surface of the insulting layer 24, the top surface and lateral side of the electrode pad 25, the wall surface of the via hole 21y and the top surface of the electrode pad 15 exposed at the bottom of the via hole 21y. The insulating layer 28 is formed by, for example, plasma CVD. The insulating layer 28 is made of, for example, Si_3N_4 or SiO_2. The thickness of the insulating layer 28 is in the range of 0.1 μm to 2.0 μm, for example.

Next in a process shown in FIG. 4L, the insulating layer 28 is removed, except for that formed on the wall surface of the via hole 21y. The removal of the insulating layer 28 is performed by, for example, RIE (Reactive Ion Etching). In this process, only predetermined parts of the insulating layer 28 are removed without using a photomask, and the process is referred to as a self-alignment process. By the self-alignment process, the positions of the via hole 21y and the electrode pad 25 are determined with accuracy. In

addition, by using a design in which no electrode pad is present in some part, etching is performed in the section with no electrode pad and is continued to the electrode pad of a different semiconductor substrate in the underlying section, to thereby form a via hole having a different depth.

Next in a process shown in FIG. 4M, a metal layer 29 is formed in such a manner as to cover the top surface of the insulating layer 24, the top surface and lateral side of the electrode pad 25, the top surface of the insulating layer 28 and the top surface of the electrode pad 15 exposed at the bottom of the via hole 21y. The metal layer 29 is formed by, for example, electroless plating, or may be formed by sputtering, CVD or the like. As the metal layer 29, a laminated body in which a Cu layer is disposed on a Ti layer, or a laminated body in which a Cu layer is disposed on a Ta layer, for example, may be used. In addition, a conductor which satisfies the design criteria can be used as the buried material, and W, Al, doped polysilicon, a carbon material such as a carbon nanotube, or a conductive polymer may be used in place of Cu. In the case where the electrical insulation of the insulating layer is sufficient, a combination with a buried wiring using no barrier metal layer may be chosen.

Next in a process shown in FIG. 4N, a photosensitive resist film 37 is formed in such a manner as to cover the top surface of the metal layer 29 except for the inside of the via hole 21y. The resist film 37 is formed, for example, by applying a dry film resist to the top surface of the metal layer 29. The thickness of the resist film 37 is 10 μm, for example. Then, in a process shown in FIG. 4O, the resist film 37 of FIG. 4N is exposed via a predetermined mask, and the exposed resist film 37

is subsequently developed, thereby forming an opening 37x in the resist film 37. The opening 37x has, for example, a circular shape in a planer view, and has a diameter φ5 of, for example, 1 μm to 30 μm.

Next in a process shown in FIG. 4P, the metal layer 38 is formed inside the via hole 21y and on a part of the opening 37x shown in FIG. 4O. With use of electrolytic plating, in which the metal layer 29 is used as a feeder layer, the metal layer 38 is formed, for example, by growing a plating film by precipitation in such a manner as to fill the inside of the via hole 21y and the part of the opening 37x shown in FIG. 4O. The plating film forming the metal layer 38 is, for example, a Cu plating film. Next in a process shown in FIG. 4Q, the resist film 37 of FIG. 4P is removed.

Next in a process shown in FIG. 4R, a part of the metal layer 29 which is not covered by the metal layer 38 is removed. The metal layer 29 may be removed by, for example, wet etching. Next in a process shown in FIG. 4S, a metal layer 39 is formed in such a manner as to cover the electrode pad 25 and the metal layer 38. The metal layer 39 is formed, for example, by forming, on the insulating layer 24, a resist film having an opening for the electrode pad 25 and the metal layer 38. Subsequently, with use of electrolytic plating, in which the electrode pad 25 and the metal layer 38 are used as feeder layers, a plating film is grown by precipitation in such a manner as to fill the opening, and the resist film is then removed to thereby form the metal layer 39. As the metal layer 39, the following may be used: a laminated body in which an Au layer is disposed on a Ti layer, for example; a laminated body in which a Pd layer and an Au layer are sequentially disposed on a Ni layer; a laminated body in

which a Cu layer or an Al layer is disposed on a layer of a high melting point metal, such as Co, Ta, Ti and TiN, in place of Ni; or a damascene interconnect structure.

Next in a process shown in FIG. 4T, a fringe portion of the semiconductor substrate 21c is removed. The semiconductor substrate 21c after the removal of the fringe portion is referred to as a semiconductor substrate 21d. The removal of the fringe portion of the semiconductor substrate 21c is performed by grinding with a grinder or the like in such a manner that the semiconductor substrate 21d after the removal of the fringe portion has, for example, a circular shape in a planar view. In this operation, dry polishing, wet etching or the like may also be used in combination. In the case where the semiconductor substrate 21d after the removal of the fringe portion has a circular shape in a planar view, a diameter φ6 of the semiconductor substrate 21d having a circular shape in a planar view is, for example, 193.0 ± 0.1 mm, as in the case of the diameter φ2 of the semiconductor substrate 11c having a circular shape in a planar view.

Next, after a resin layer 26 is formed on the surface 21a of the semiconductor substrate 21d, the semiconductor substrate 31 is prepared, which has a configuration the same as that of the semiconductor substrate 11 of FIGs. 4A and 4B. Then, the processes of FIGs. 4E to 4T are repeated. The same processes are repeated for semiconductor substrates 41 to 71. Lastly, the external connection terminals 91 are formed by a well-recognized method. When the external connection terminals 91 are formed, a Ni layer, for example, is formed as the metal layer 39. Then, the solder mask layer 76 having the openings 76x which expose the Ni layer is formed, and the

external connection terminals 91 are formed on the Ni layer exposed inside the openings 76x.

The external connection terminals 91 are provided to electrically connect the semiconductor device 10 and a wiring substrate or the like provided outside the semiconductor device 10. As the external connection terminals 91, solder balls, Au bumps, a conductive paste or the like may be used. In the case when solder balls are used as the external connection terminals 91, an alloy containing Pb, an alloy of Sn and Cu, an alloy of Sn and Ag, an alloy of Sn, Ag and Cu or the like may be used as a material of the external connection terminals 91.

In this manner, the semiconductor device 10 of FIG. 3 is manufactured. The semiconductor device 10 is cut into individual pieces at the cutting positions C using a dicing blade or the like to thereby form final products.

According to the first embodiment of the present invention, a first semiconductor substrate is prepared, in which only the fringe portion is removed (reduction in the diameter) without thickness reduction. Also, a second semiconductor substrate is prepared, in which a depression is formed in such a manner as to reduce the thickness of the central portion and its vicinity while leaving the fringe portion. Then, the depression of the second substrate is bonded to the first semiconductor substrate, and via holes are formed in such a manner as to penetrate the second semiconductor substrate with a reduced thickness, and electrode pads of each semiconductor chip of the first and second semiconductor substrates are electrically connected to each other via metal layers formed in the via holes. Then, the fringe portion of the second semiconductor substrate is removed. Furthermore,

in the same manner with the second semiconductor, a third semiconductor substrate is prepared, in which a depression is formed to reduce the thickness of the central portion and its vicinity while leaving the fringe portion. Then, the depression of the third substrate is bonded to the second semiconductor substrate, and via holes are formed in such a manner as to penetrate the third semiconductor substrate with a reduced thickness, and electrode pads of each semiconductor chip of the second and third semiconductor substrates are electrically connected to each other via metal layers formed in the via holes. Then, the fringe portion of the third semiconductor substrate is removed.

By repeating such processes, it is possible to dispose plural semiconductor substrates one above the other and connect semiconductor chips, each of which constitutes a different semiconductor substrate, in such a manner as to enable signal transmission. This process flow eliminates the need for the processes of bonding and removing a support to/from the semiconductor substrate, which processes are not usual wafer process of a semiconductor device, and it is therefore possible to provide a semiconductor device manufacturing method with high productivity, capable of reducing the manufacturing costs. Note that in the case when the diameter of the prepared first semiconductor substrate is smaller than the diameter of the bottom surface of the depression in the second semiconductor, the vertical wiring system according to the present invention is applicable without the removal of the fringe portion of the first semiconductor substrate.

In addition, according to the first embodiment of the present invention, a process of forming a bump on each via hole when the semiconductor substrates are bonded

to one another is not necessary, and it is therefore possible to provide a semiconductor device manufacturing method with high productivity, capable of reducing the manufacturing costs.

In addition, according to the first embodiment of the present invention, semiconductor substrates are bonded to one another in such a manner that a surface of one of the semiconductor substrates, on which surface a semiconductor integrated circuit is formed, opposes a surface of the other semiconductor substrate, on which surface a semiconductor integrated circuit is not formed. Accordingly, by simply repeating the same processes, three or more semiconductor substrates can be disposed one above the other, and it is therefore possible to provide a semiconductor device manufacturing method with high productivity, capable of reducing the manufacturing costs.

In addition, according to the first embodiment of the present invention, the via holes are formed, within the semiconductor substrate, only in a part having a reduced thickness. This eliminates the need for creating deep via holes, and therefore causes neither an increase in the time required for the hole-formation of the via holes and the metal layer forming process nor an increase in the number of materials required for these processes, which results in preventing an increase in the cost of manufacturing the semiconductor device.

In addition, according to the first embodiment of the present invention, since the via holes are formed after the thickness of the semiconductor substrate is reduced to a great extent, it is possible to reduce the variation in the diameter of the end portions of the via holes even when the size or density of the via holes are changed. As a result, the variation in the resistance of

the electrical connections is reduced, and thus, the reliability of the semiconductor device is improved.

[Modification of First Embodiment]

The first embodiment describes an example in which, by forming the depression 21x in such a manner as to reduce the thickness of the central portion and its vicinity (the area including the plural semiconductor chip formation regions A) while leaving the fringe portion of the semiconductor substrate 21 (the area excluding the plural semiconductor chip formation regions A), the semiconductor substrate 21c after the formation of the depression 21x maintains sufficient rigidity. However, the thickness reduction may be performed on the entire surface 21b of the semiconductor substrate 21 without the formation of the depression 21x. In this case, the following manufacturing processes can be adopted.

FIGs. 5A to 5D illustrate a manufacturing process flow of a semiconductor device according to a modification of the first embodiment of the present invention. In FIGs. 5A to 5D, the same reference numerals are given to the components which are common to the semiconductor device 10 shown in FIG. 3, and their explanations may be omitted.

First, the semiconductor substrate 11 shown in FIGs. 4A and 4B is prepared. Next in a process shown in FIG. 5A, the resin layer 16 is formed on the surface 11a of the semiconductor substrate 11 without removing the fringe portion 11x of the semiconductor substrate 11. At this point, in the same manner as in the process of FIG. 4D, it is preferable that, when the surface 11b of the semiconductor substrate 11c is used as a reference plane, the variation in the height H1 of the surface 16a of the resin layer 16 with respect to the reference plane is

preferably 1 μm or less. Accordingly, it is preferable to have a process of checking the variation in the height H1 after the formation of the resin layer 16. In the case where the variation in the height H1 is more than 1 μm, it is preferable to have a process of adjusting the surface 16a of the resin layer 16 to make the variation in the height H1 within 1 μm. The surface 16a of the resin layer 16 may be processed by, for example, a CMP method.

When n semiconductor substrates have already been disposed one above the other and a resin layer is then formed on the topmost (the n^{th} layer) semiconductor substrate, the back surface of the bottom semiconductor substrate (the surface on which no devices are formed) is used as a reference plane. In this case, it is preferable that the top surface of the resin layer be parallel to the reference plane. Note that being parallel in this case means that the variation in the height of the top surface of the resin layer with respect to the reference plane is $(1 \times n)$ μm or less. That is, as described above, in the case when a resin layer is formed on a single semiconductor substrate, the variation in the height of the top surface of the resin layer with respect to the reference plane is preferably $1 \times 1 = 1$ μm or less, and in the case when a resin layer is formed on semiconductor substrates of, for example, ten layers, the variation in the height of the top surface of the resin layer with respect to the reference plane is preferably $1 \times 10 = 10$ μm or less.

Next in a process shown in FIG. 5B, the semiconductor substrate 21 is prepared, which has a configuration the same as that of the semiconductor substrate 11 of FIGs. 4A and 4B. Then, an adhesion layer 96 is formed on the surface 21a of the semiconductor

substrate 21, and a support 97 is bonded (temporarily bonded) to the adhesion layer 96. As the support 97, it is preferable to use a substrate which transmits light when alignment is performed, and a silica glass substrate, for example, may be used. As the adhesion layer 96, an adhesive agent may be used which turns soft at a heating temperature used in a process of FIG. 5D (i.e., an adhesive agent which becomes soft at about 200 °C or less) to be described below. The adhesion layer 96 is formed on the surface 21a of the semiconductor substrate 21 by spin-coating, for example. The adhesion layer 96 may be formed on the surface 21a of the semiconductor substrate 21 by attaching a film-type adhesive instead of by spin-coating.

Next in a process shown in FIG. 5C, thickness reduction is performed on the entire surface 21b of the semiconductor substrate 21. The semiconductor substrate 21 after the thickness reduction is referred to as the semiconductor substrate 21c. The thickness reduction is achieved, for example, by grinding the surface 21b of the semiconductor substrate 21 using a grinder or the like. In this operation, dry polishing, wet etching or the like may also be used in combination. The thickness T3 of the semiconductor substrate 21c with a reduced thickness is in the range of about 1 μm to about 100 μm, for example; however, in terms of strength, the thickness T3 is preferably in the range of about 10 μm to about 50 μm. This is because setting the thickness T3 of the area with a reduced thickness to about 10 μm to about 50 μm reduces breakage due to mechanical vibrations or the like and stress exerted on the semiconductor chips. The support 97 has a function of supporting the semiconductor substrate 21c having reduced rigidity after the thickness reduction. The reason why the thickness T3 of the semiconductor

substrate 21c with a reduced thickness has to be 1 μm or more is as described above.

Next in a process shown in FIG. 5D, the semiconductor substrate 21c having the support 97 is disposed on the semiconductor substrate 11 in such a manner that the surface 16a of the resin layer 16 which has been formed on the surface 11a of the semiconductor substrate 11 comes in contact with the surface 21b of the semiconductor substrate 21c. Alignment marks for enabling highly accurate positioning are provided in advance in, for example, the scribing regions B of the semiconductor substrates 11 and 21c. The positioning of the semiconductor substrate 21c having the support 97 onto the semiconductor substrate 11 may be achieved by a well-recognized method using the alignment marks as a reference. The alignment accuracy is, for example, 2 μm or less. Subsequently, while being heated at, for example, 250 °C, the structure shown in FIG. 5D is pressed from the support 97 side to thereby cause the surface 16a of the resin layer 16 formed on the surface 11a of the semiconductor substrate 11 to be press-bonded to the surface 21b of the semiconductor substrate 21c. Herewith, the resin layer 16 becomes hardened, and the semiconductor substrate 11 is bonded to the surface 21b of the semiconductor substrate 21c. The heating operation may be performed at 300 °C; however, the temperature is preferably 200 °C or less. If the operation is performed at the temperature as high as 300 °C, stress occurs due to a difference in the thermal expansion, which can cause separation and/or breakage of the semiconductor substrates. Such separation and breakage becomes more likely as the number of laminated layers increases. Note that since the adhesion layer 96 is made of an adhesive agent which turns soft at a heating

temperature used in the process of FIG. 5D (i.e., an adhesive agent which becomes soft at about 200 °C or less), the support 97 is readily removed after the semiconductor substrates 11 and 21c are bonded to each other.

Next, the photosensitive resist film 27 is formed in such a manner as to cover the surface 21a of the semiconductor substrate 21c in the same manner as in the process of FIG. 4G of the first embodiment. The resist film 27 is formed, for example, by applying a liquid resist to the surface 21a of the semiconductor substrate 21c. The thickness of the resist film 27 is 10 μm, for example. Subsequently, processes the same as those of FIGs. 4H to 4T according to the first embodiment are performed.

Next, after the resin layer 26 is formed on the surface 21a of the semiconductor substrate 21d, the semiconductor substrate 31 is prepared, which has a configuration the same as that of the semiconductor substrate 11 of FIGs. 4A and 4B. Then, the above-described processes and the processes of FIGs. 4H to 4T are repeated. The same processes are repeated for the semiconductor substrates 41 to 71. Lastly, the external connection terminals 91 are formed by a well-recognized method. When the external connection terminals 91 are formed, a Ni layer, for example, is formed as the metal layer 39. Then, the solder mask layer 76 having the openings 76x which expose the Ni layer is formed, and the external connection terminals 91 are formed in the openings 76x where the Ni layer is exposed, to thereby manufacture a semiconductor device equivalent to the semiconductor device 10 of FIG. 3. Note however that in the manufactured semiconductor device, the fringe portion of each of the semiconductor substrates disposed one above

the other is not removed. The manufactured semiconductor device is cut into individual pieces at the cutting positions C using a dicing blade or the like to thereby form final products.

According to the modification of the first embodiment of the present invention, a first semiconductor substrate, on which thickness reduction is not performed, is prepared. Also, a second semiconductor, on which thickness reduction has been performed, is prepared. Then, the second substrate is bonded to the first semiconductor substrate, and via holes are formed in such a manner as to penetrate the second semiconductor substrate with a reduced thickness, and electrode pads of each semiconductor chip of the first and second semiconductor substrates are electrically connected to each other via metal layers formed in the via holes. Furthermore, a third semiconductor substrate with a reduced thickness is prepared. Then, the third substrate is bonded to the second semiconductor substrate, and via holes are formed in such a manner as to penetrate the third semiconductor substrate with a reduced thickness, and electrode pads of each semiconductor chip of the second and third semiconductor substrates are electrically connected to each other via metal layers formed in the via holes.

By repeating such processes, it is possible to dispose plural semiconductor substrates one above the other and connect semiconductor chips, each of which constitutes a different semiconductor substrate, in such a manner as to enable signal transmission. This process flow eliminates the need for the process of forming a bump on each via hole when the semiconductor substrates are bonded to one another, and it is therefore possible to provide a semiconductor device manufacturing method with

high productivity, capable of reducing the manufacturing costs.

In addition, according to the modification of the first embodiment of the present invention, semiconductor substrates are bonded to one another in such a manner that a surface of one of the semiconductor substrates, on which surface a semiconductor integrated circuit is formed, opposes a surface of the other semiconductor substrate, on which surface a semiconductor integrated circuit is not formed. Accordingly, by simply repeating the same processes, three or more semiconductor substrates can be disposed one above the other, and it is therefore possible to provide a semiconductor device manufacturing method with high productivity, capable of reducing the manufacturing costs.

In addition, according to the modification of the first embodiment of the present invention, the via holes are formed, within the semiconductor substrate, only in a part having a reduced thickness. This eliminates the need for creating deep via holes, and therefore causes neither an increase in the time required for the hole-formation of the via holes and the metal layer forming process nor an increase in the number of materials required for these processes, which results in preventing an increase in the cost of manufacturing the semiconductor device.

In addition, according to the modification of the first embodiment of the present invention, since the via holes are formed after the thickness of the semiconductor substrate is reduced to a great extent, it is possible to reduce the variation in the diameter of the end portions of the via holes even when the size or density of the via holes are changed. As a result, the

variation in the resistance of the electrical connections is reduced, and thus, the reliability of the semiconductor device is improved.

[Second Embodiment]

[Configuration Of Semiconductor Device According To Second Embodiment Of The Present Invention]

First is described the configuration of a semiconductor device according to a second embodiment of the present invention. FIG. 6 is a cross-sectional view illustrating a semiconductor device according to the second embodiment of the present invention. In FIG. 6, the same reference numerals are given to the components which are common to those in FIG. 3, and their explanations may be omitted. A semiconductor device 10A according to the second embodiment of the present invention has the same configuration as that of the semiconductor device 10 according to the first embodiment of the present invention, except that the number of via holes and metal layers connecting metal pads of adjacent semiconductor substrates is four, instead of one in the first embodiment.

In FIG. 6, the reference numerals 21z to 71z denote via holes, and the reference numerals 38a to 88a denote metal layers formed in the via holes 21z to 71z. Four via holes and four metal layers are provided for each metal pad in each semiconductor substrate.

Thus, by providing plural via holes and metal layers for each metal pad, it is possible to improve the reliability of the connection between metal pads. In addition, if a metal pad is not provided for a semiconductor substrate disposed immediately below, via holes and metal layers can be provided for a semiconductor substrate at one or more layers below. In this system,

the same electrical signal or a different electrical signal can be connected to a desired semiconductor substrate. In addition, since each via hole has a smaller diameter, it is possible to reduce the time required for the process of providing the via holes and metal layers. Note that the number of via holes and metal layers provided for each metal pad may be two, three, five or more.

[Processes For Manufacturing Semiconductor Device According To Second Embodiment Of The Present Invention]

Next is described a manufacturing process flow of the semiconductor device according to the second embodiment of the present invention. FIGs. 7A to 7F illustrate the manufacturing process flow of the semiconductor device according to the second embodiment of the present invention. In FIGs. 7A to 7F, the same reference numerals are given to the components which are common to the semiconductor device 10A shown in FIG. 6, and their explanations may be omitted. Also, manufacturing processes similar to those of the semiconductor device according to the first embodiment of the present invention may be omitted.

First, processes the same as those of FIGs. 4A to 4G are performed. Next in a process shown in FIGs. 7A and 7B, the resist film 27 of FIG. 4G is exposed via a predetermined mask, and the exposed resist film 27 is subsequently developed, thereby forming openings 27y in the resist film 27. FIG. 7A is a cross-sectional view, and FIG. 7B is a plan view. Note that for convenience of explanation, FIGs. 7A to 7F show enlarged views of a part of the structure shown in FIG. 4G (i.e., the electrode pads 15 and 25 and their vicinity).

Next in a process shown in FIG. 7C, the via

holes 21z are formed in the semiconductor substrate 21c. The via holes 21z are formed in such a manner to penetrate the resin layer 16 and parts of the semiconductor substrate 21c (the substrate body 22, the semiconductor integrated circuit 23, the insulating layer 24 and the electrode pad 25) corresponding to the openings 27y so that the electrode pad 15 of the semiconductor substrate 11c is exposed. The via holes 21z are formed by, for example, dry etching. Each of the via holes 21z has, for example, a circular shape in a planar view, and has a diameter φ7 of, for example, 1 μm to 10 μm. Note however that the diameter φ7 of each of the via holes 21z is preferably set to a value which allows the via hole 21z to have an aspect ratio (= depth D2/diameter φ7) between 0.5 and 5 inclusive. This is because by setting the diameter φ7 of the via hole 21z to a value which allows the via hole 21z to have an aspect ratio (= depth D2/diameter φ7) between 0.5 and 5 inclusive, it is possible to achieve, for example, an improvement in the etching speed (throughput) for forming the via hole 21z and an improvement of the ease of forming the metal layer 38a in the via hole 21z.

Next in a process shown in FIG. 7D, the resist film 27 of FIG. 7C is removed. Then, processes the same as those of FIGs. 4K to 4Q are performed, to thereby form the metal layers 38a in the via holes 21z as shown in FIG. 7E. Next, a part of the metal layer 29 which is not covered by the metal layers 38a is removed by, for example, wet etching, and then the metal layer 39 is formed in such a manner as to cover the electrode pad 25 and the metal layers 38a, as shown in FIG. 7F. The metal layer 39 is formed, for example, by forming, on the insulating layer 24, a resist film having an opening for the electrode pad

25 and the metal layers 38a. Subsequently, with use of electrolytic plating, in which the electrode pad 25 and the metal layers 38a are used as feeder layers, a plating film is grown by precipitation in such a manner as to fill the opening, and the resist film is then removed to thereby form the metal layer 39.

Subsequently, by repeating processes the same as those of the first embodiment, the semiconductor device 10A of FIG. 6 is manufactured. The semiconductor device 10A is cut into individual pieces at the cutting positions C using a dicing blade or the like to thereby form final products.

According to the second embodiment of the present invention, the same effect as in the first embodiment can be achieved. In addition, since each via hole has a smaller diameter, it is possible to reduce the time required for the process of providing the via holes and metal layers. Also, by providing plural via holes and metal layers for each metal pad, it is possible to improve the reliability of the connection between metal pads.

[Third Embodiment]

[Configuration Of Semiconductor Device According To Third Embodiment Of The Present Invention]

First is described the configuration of a semiconductor device according to a third embodiment of the present invention. FIG. 8 is a cross-sectional view illustrating a semiconductor device according to the third embodiment of the present invention. In FIG. 8, the same reference numerals are given to the components which are common to those in FIG. 6, and their explanations may be omitted. A semiconductor device 10B according to the third embodiment of the present invention has the same configuration as that of the semiconductor device 10A

according to the second embodiment of the present invention, except that one metal pad is provided for each via hole and metal layer, instead of providing one metal pad for four via holes and four metal layers in the semiconductor device 10A according to the second embodiment of the present invention.

In FIG. 8, the reference numerals 15a, 15b-75a and 75b denote metal pads. One metal pad is provided for each set of a via hole and metal layer.

Thus, by providing one metal pad for each set of a via hole and metal layer, it is possible to improve the reliability of the connection between metal pads, as in the case of the second embodiment, when the same signal is assigned to adjacent metal pads. In addition, in the case where different signals are respectively assigned to adjacent metal pads, it is possible to improve the flexibility of the wiring design.

[Processes For Manufacturing Semiconductor Device According To Third Embodiment Of The Present Invention]

Next is described a manufacturing process flow of the semiconductor device according to the third embodiment of the present invention. FIGs. 9A to 9F illustrate the manufacturing process flow of the semiconductor device according to the third embodiment of the present invention. In FIGs. 9A to 9F, the same reference numerals are given to the components which are common to the semiconductor device 10B shown in FIG. 8, and their explanations may be omitted. Also, manufacturing processes similar to those of the semiconductor devices according to the first and second embodiments of the present invention may be omitted.

First, processes the same as those of FIGs. 4A to 4G are performed. Next in a process shown in FIGs. 9A

and 9B, the resist film 27 of FIG. 4G is exposed via a predetermined mask, and the exposed resist film 27 is subsequently developed, thereby forming openings 27y in the resist film 27. FIG. 9A is a cross-sectional view, and FIG. 9B is a plan view. Note that for convenience of explanation, FIGs. 9A to 9F show enlarged views of a part of the structure shown in FIG. 4G (i.e., the electrode pads 15 and 25 and their vicinity).

Next in a process shown in FIG. 9C, the via holes 21z are formed in the semiconductor substrate 21c. The via holes 21z are formed in such a manner to penetrate the resin layer 16 and parts of the semiconductor substrate 21c (the substrate body 22, the semiconductor integrated circuit 23, the insulating layer 24 and the electrode pad 25) corresponding to the openings 27y so that electrode pads 15a and 15b of the semiconductor substrate 11c are exposed. The via holes 21z are formed by, for example, dry etching. Each of the via holes 21z has, for example, a circular shape in a planar view, and has the diameter φ7 of, for example, 1 μm to 10 μm. Note however that the diameter φ7 of each of the via holes 21z is preferably set to a value which allows the via hole 21z to have an aspect ratio (= depth D2/diameter φ7) between 0.5 and 5 inclusive. This is because by setting the diameter φ7 of the via hole 21z to a value which allows the via hole 21z to have an aspect ratio (= depth D2/diameter φ7) between 0.5 and 5 inclusive, it is possible to achieve, for example, an improvement in the etching speed (throughput) for forming the via hole 21z and an improvement of the ease of filling the metal layer 38b in the via hole 21z.

Next in a process shown in FIG. 9D, the resist film 27 of FIG. 9C is removed. Then, processes the same

as those of FIGs. 4K to 4Q are performed, to thereby form the metal layers 38b in the via holes 21z as shown in FIG. 9E. Next, parts of the metal layer 29 which are not covered by the metal layers 38b are removed by, for example, wet etching, and then metal layers 39a are formed in such a manner as to cover the electrode pads 25 and the metal layers 38b, as shown in FIG. 9F. The metal layers 39a are formed, for example, by forming, on the insulating layer 24, a resist film having openings for the electrode pads 25 and the metal layers 38b. Subsequently, with use of electrolytic plating, in which the electrode pads 25 and the metal layers 38b are used as feeder layers, a plating film is grown by precipitation in such a manner as to fill the openings, the resist film is then removed to thereby form the metal layers 39a.

Subsequently, by repeating processes the same as those of the first embodiment, the semiconductor device 10B of FIG. 8 is manufactured. The semiconductor device 10B is cut into individual pieces at the cutting positions C using a dicing blade or the like to thereby form final products.

According to the third embodiment of the present invention, the same effect as in the first embodiment can be achieved. In addition, in the case when the same signal is assigned to adjacent metal pads, it is possible to improve the reliability of the connection between metal pads. On the other hand, in the case where different signals are respectively assigned to adjacent metal pads, it is possible to improve the flexibility of the wiring design.

[Fourth Embodiment]

[Configuration Of Semiconductor Device According To Fourth Embodiment Of The Present Invention]

First is described the configuration of a semiconductor device according to a fourth embodiment of the present invention. FIG. 10 is a cross-sectional view illustrating a semiconductor device according to the fourth embodiment of the present invention. In FIG. 10, the same reference numerals are given to the components which are common to those in FIG. 8, and their explanations may be omitted. A semiconductor device 10C according to the fourth embodiment of the present invention has the same configuration as that of the semiconductor device 10B according to the third embodiment of the present invention, except that some of the via holes are not provided with a metal pad, and that semiconductor substrates on which metal pads are provided are directly connected to each other by via holes and metal layers, whereas all positions corresponding to via holes in every semiconductor substrate are provided with a metal pad in the semiconductor device 10B according to the third embodiment of the present invention.

Thus, by providing metal pads for only some of the semiconductor substrates, semiconductor substrates not adjacent to each other can be directly connected by via holes and metal layers, which results in an increase in the flexibility of the wiring design.

[Processes For Manufacturing Semiconductor Device According To Fourth Embodiment Of The Present Invention]

Next is described a manufacturing process flow of the semiconductor device according to the fourth embodiment of the present invention. FIGs. 11A to 11H illustrate the manufacturing process flow of the semiconductor device according to the fourth embodiment of the present invention. In FIGs. 11A to 11H, the same reference numerals are given to the components which are

common to the semiconductor device 10C shown in FIG. 10, and their explanations may be omitted. Also, manufacturing processes similar to those of the semiconductor devices according to the first to third embodiments of the present invention may be omitted.

First, processes the same as those of FIGs. 4A to 4G are performed. Next in a process shown in FIGs. 11A and 11B, the resist film 27 of FIG. 4G is exposed via a predetermined mask, and the exposed resist film 27 is subsequently developed, thereby forming openings 27z in the resist film 27. FIG. 11A is a cross-sectional view, and FIG. 11B is a plan view. Note that for convenience of explanation, FIGs. 11A to 11H show enlarged views of a part of the structure shown in FIG. 4G (i.e., the electrode pads 15 and 25 and their vicinity).

Next in a process shown in FIG. 11C, the via holes 21z are formed in the semiconductor substrate 21c. The via holes 21z are formed in such a manner to penetrate the resin layer 16 and parts of the semiconductor substrate 21c (the substrate body 22, the semiconductor integrated circuit 23, the insulating layer 24 and the electrode pad 25) corresponding to the openings 27z so that electrode pads 15a and 15b of the semiconductor substrate 11c are exposed. The via holes 21z are formed by, for example, dry etching. Each of the via holes 21z has, for example, a circular shape in a planar view, and has the diameter $\varphi 7$ of, for example, 1 μm to 10 μm. Note however that the diameter $\varphi 7$ of each of the via holes 21z is preferably set to a value which allows the via hole 21z to have an aspect ratio (= depth D2/diameter $\varphi 7$) between 0.5 and 5 inclusive. This is because by setting the diameter $\varphi 7$ of the via hole 21z to a value which allows the via hole 21z to have an aspect ratio (= depth

D2/diameter φ7) between 0.5 and 5 inclusive, it is possible to achieve, for example, an improvement in the etching speed (throughput) for forming the via hole 21z and an improvement of the ease of forming the metal layer 38b in the via hole 21z.

Next in a process shown in FIG. 11D, the resist film 27 of FIG. 11C is removed. Then, after processes the same as those of FIGs. 4K to 4L are performed, the metal layer 29 is formed in such a manner as to cover the top surface of the insulating layer 24, the top surface and lateral side of the electrode pad 25, the top surface of the insulating layer 28 and the top surfaces of the electrode pads 15a and 15b exposed at the bottom of the via holes 21z. The metal layer 29 is formed by, for example, electroless plating, or may be formed by sputtering, CVD or the like. As the metal layer 29, a laminated body in which a Cu layer is disposed on a Ti layer, or a laminated body in which a Cu layer is disposed on a Ta layer, for example, may be used. In addition, a conductor which satisfies the design criteria can be used as the buried material, and W, Al, doped polysilicon, a carbon material such as a carbon nanotube, or a conductive polymer may be used in place of Cu. In the case where the electrical insulation of the insulating layer is sufficient, a combination with a buried wiring using no barrier metal layer may be chosen.

Next in a process shown in FIG. 11F, the photosensitive resist film 37 is formed in such a manner as to cover the top surface of the metal layer 29 except for the inside of the via holes 21z. The resist film 37 is formed, for example, by applying a dry film resist to the top surface of the metal layer 29. The thickness of the resist film 37 is 10 μm, for example. Then, the

resist film 37 is exposed via a predetermined mask and subsequently developed, thereby forming an opening 37y in the resist film 37. The opening 37y is formed only on a via hole 21z corresponding to a section at which the electrode pad 25 has been formed.

Next, in the same manner as in the processes of FIGs. 4P to 4R, a part of the metal layer 29 which is not covered by the metal layer 38b is removed as shown in FIG. 11G. Next in a process shown in FIG. 11H, the metal layer 39a is formed in such a manner as to cover the electrode pad 25 and the metal layer 38b. The metal layer 39a is formed, for example, by forming, on the insulating layer 24, a resist film having an opening for the electrode pad 25 and the metal layer 38b. Subsequently, with use of electrolytic plating, in which the electrode pad 25 and the metal layer 38b are used as feeder layers, a plating film is grown by precipitation in such a manner as to fill the opening, and the resist film is then removed to thereby form the metal layer 39a.

Subsequently, by repeating processes the same as those of the first embodiment, the semiconductor device 10C of FIG. 10 is manufactured. Note that via holes with no metal-layer filling are filled with a metal layer in the same manner as in the first embodiment after a semiconductor substrate having electrode pads is disposed thereon. The semiconductor device 10C is cut into individual pieces at the cutting positions C using a dicing blade or the like to thereby form final products.

Note that positions to be and not to be provided with a metal pad can be decided arbitrarily, and it is not limited to the case illustrated in FIG. 10.

According to the fourth embodiment of the present invention, the same effect as in the first

embodiment can be achieved. In addition, by not providing metal pads for some of the via holes in all the semiconductor substrates, semiconductor substrates not adjacent to each other can be directly connected by via holes and metal layers, which results in the flexibility of the wiring design.

[Fifth Embodiment]

The first to fourth embodiments illustrate and describe methods of manufacturing a semiconductor device for disposing plural semiconductor substrates having semiconductor chips one above the other and connecting semiconductor chips, each of which constitutes a different semiconductor substrate, in such a manner as to enable signal transmission. However, not all the substrates to be disposed one above the other have to be a semiconductor substrate having semiconductor chips, and a structure layer having no semiconductor chips may also be included. Accordingly, a fifth embodiment of the present invention illustrates and describes a method of manufacturing a semiconductor device including a structure layer having no semiconductor chips. Here, the structure layer means a set of layers having no semiconductor chips, which set includes a silicon substrate, a metal layer, an insulating layer and the like.

[Configuration Of Semiconductor Device According To Fifth Embodiment Of The Present Invention]

First is described the configuration of a semiconductor device according to the fifth embodiment of the present invention. FIG. 12 is a cross-sectional view illustrating the semiconductor device according to the fifth embodiment of the present invention. In FIG. 12, the same reference numerals are given to the components which are common to those in FIG. 3, and their

explanations may be omitted. A semiconductor device 10D according to the fifth embodiment of the present invention has the same configuration as that of the semiconductor device 10 of FIG. 3 according to the first embodiment of the present invention, except that a structure layer 81 and a resin layer 86 are provided between the resin layer 66 and the semiconductor substrate 71c of the semiconductor device 10.

In the semiconductor device 10D of FIG. 12, the structure layer 81 is disposed on the semiconductor substrate 61c via the resin layer 66, and the semiconductor substrate 71c is disposed on the structure layer 81 via the resin layer 86. The structure layer 81 is provided with, for example, via holes (not shown) and metal layers (not shown) for electrically connecting the semiconductor substrates 61c and 71. The resin layer 86 may be made of the same material as that of the resin layer 16 or the like.

The structure layer 81 includes a silicon substrate 81c having no semiconductor chips, an insulating film 81d and grooves 81x. The grooves 81x are provided, in the silicon substrate 81c, on the semiconductor substrate 71c side, and the insulating film 81d made, for example, of Si_3N_4 or SiO_2 is formed on the surface of the silicon substrate 81c including the grooves 81x. The silicon substrate 81c is insulated from the adjacent semiconductor substrate 71c by the insulating film 81d. In the grooves 81x, a cooling medium, such as water and ethanol, is supplied, and the grooves 81x function as refrigerant flow paths. The shape and positions of the grooves 81x may be determined arbitrarily.

Thus, substrates to be disposed in the semiconductor device are not limited to semiconductor

substrates having semiconductor chips, and a structure layer with no semiconductor chips may also be included. By including, for example, a silicon substrate having refrigerant flow paths in the structure layer to be disposed in the semiconductor device, it is possible to cause the semiconductor device to have a cooling function for transferring heat generated by semiconductor substrates. It is especially effective if the structure layer having a cooling function is provided adjacent to a semiconductor substrate including a device generating a large amount of heat, such as a CPU. Note that the semiconductor device may include plural structure layers having no semiconductor chips.

[Processes For Manufacturing Semiconductor Device According To Fifth Embodiment Of The Present Invention]

Next is described a manufacturing process flow of the semiconductor device according to the fifth embodiment of the present invention.

First, the structure layer 81 is prepared. Specifically, the silicon substrate 81c is processed to have a predetermined outer diameter, and the grooves 81x are formed on one surface of the silicon substrate 81c. The grooves 81x are formed by, for example, DRIE (Deep Reactive Ion Etching). Then, the insulating film 81d is formed on the surface of the silicon substrate 81c, on which surface the grooves 81x have been formed. The insulating film 81d is formed by, for example, plasma CVD. According to these processes, the structure layer 81 is completed.

Next, in processes the same as those of FIGs. 4A to 4T, the semiconductor substrates 11c-61c, the resin layer 66, the structure layer 81, the resin layer 86 and the semiconductor substrate 71c are sequentially disposed

one above the other, and then via holes, metal layers and the like are formed, to thereby complete the semiconductor device 10D.

Thus, the above illustrates and describes the method of manufacturing the semiconductor device having a structure layer which includes a silicon substrate having no semiconductor chips; however, the structure layer may include, in addition to the silicon substrate having no semiconductor chips, a metal layer made of Cu or the like and an insulating layer made of an epoxy resin, or may have a structure having a MEMS device. Examples of such a MEMS device include pressure sensors and acceleration sensors.

According to the fifth embodiment of the present invention, the same effect as in the first embodiment can be achieved. In addition, by providing the structure layer having no semiconductor chips in the semiconductor device, it is possible to achieve, for example, a cooling function for transferring heat generated by semiconductor substrates.

[Sixth Embodiment]

The first to fourth embodiments illustrate and describe methods of manufacturing a semiconductor device (WOW) for disposing plural semiconductor substrates having semiconductor chips one above the other and connecting semiconductor chips, each of which constitutes a different semiconductor substrate, in such a manner as to enable signal transmission. The fifth embodiment illustrates and describes a method of manufacturing a semiconductor device including a structure layer having no semiconductor chips. Next, a sixth embodiment illustrates and describes the entire manufacturing process flow of a semiconductor device, including WOW processes and widely-recognized

semiconductor device manufacturing processes (so-called FEOL and BEOL).

FIG. 13 is a flowchart showing an example of the entire manufacturing process flow of a semiconductor device, including WOW processes and widely-recognized semiconductor device manufacturing processes. With reference to FIG. 13, first in a process of "oxidation" (S11), an oxide film is formed on the surface of a semiconductor substrate. Next in a process of "diffusion" (S12), a dopant (impurity) is introduced into the semiconductor substrate to form a semiconductor region. Next in a process of "FEOL (Front End Of Line)" (S13), devices, such as transistors or the like, are formed by repeating a lithography process (S13a), an etching process (S13b), a film formation process (S13c) and a CMP process (S13d) as many times as required.

Specifically, in the lithography process (S13a), a photoresist (photo-sensitive material) is applied to the semiconductor substrate, and a device/circuit pattern drawn on a photomask is transferred onto the semiconductor substrate by an exposure device. In the etching process (S13b), unnecessary parts of the oxide film, metal film and the like are removed by physical or chemical etching. In the film formation process (S13c), an oxide film, a metal film and the like constituting devices, such as transistors, are formed by sputtering, CVD or the like. In the CMP process (S13d), the surface of the semiconductor substrate is polished.

Next in a process of "BEOL (Back End Of Line)" (S14), the devices, such as transistors or the like, formed on the semiconductor substrate are wired using Cu or the like to complete a circuit by repeating a lithography process (S14a), an etching process (S14b), a

film formation process (S14c) and a CMP process (S14d) as many times as required. The lithography process (S14a), the etching process (S14b), the film formation process (S14c) and the CMP process (S14d) are as described above. Herewith, the semiconductor substrate having semiconductor chips is completed.

Next in a process of "WOW (wafer-on-wafer)" (S15), a thickness reduction process (S15a), a lamination process (S15b), a lithography process (S15c), a via hole etching process (S15d), a film formation process (S15e) and a planarization process (S15f) are repeated as many times as required. Herewith, plural semiconductor substrates having semiconductor chips are disposed one above the other and semiconductor chips, each of which constitutes a different semiconductor substrate, are connected in such a manner as to enable signal transmission.

Specifically, in the thickness reduction process (S15a), the semiconductor substrate is reduced in thickness, as shown in FIGs. 4E and 5C. In the lamination process (S15b), the semiconductor substrate having a reduced thickness and a semiconductor substrate on which no thickness reduction is performed are disposed one above the other, as shown in FIGs. 4F and 5D. In the lithography process (S15c), the via hole etching process (S15d), the film formation process (S15e) and the planarization process (S15f), semiconductor chips, each of which constitutes a different semiconductor substrate, are connected to each other in such a manner as to enable signal transmission, as shown in FIGs. 4H-4S, for example.

Next in a process of "electrical testing" (S16), electrical testing of the laminated semiconductor substrates is performed. Next in a process of "grinding"

(S17), the laminated semiconductor substrates are polished to adjust the thickness. Next in a process of "dicing" (S18), the laminated semiconductor substrates are cut to form plural laminated semiconductor chips. Next in a process of "bonding" (S19), the laminated semiconductor chip is fixed onto a lead frame, and the electrode pads of the semiconductor chip and the lead frame are electrically connected to each other by a bonding wire. Next in a process of "molding" (S20), the laminated semiconductor chip fixed onto the lead frame is sealed with a resin. Next in a process of "final inspection" (S21), a pre-shipment inspection (inspections on electrical properties, appearance and the like) of the laminated semiconductor chip which is made into a final product form in the process of S20. In this manner, all processes are completed.

In FIG. 13, the processes S11-S14 are well-recognized processes for handling semiconductor substrates before singularization (dicing). The WOW process of S15 according to the present invention, following S14, is also a process for handling the semiconductor substrates before singularization (dicing). That is, while maintaining the semiconductor substrates in the pre-dicing state, it is possible to form the semiconductor substrates into a three-dimensional structure (i.e., dispose plural semiconductor substrates having semiconductor chips one above the other) and connect semiconductor chips, each of which constitutes a different semiconductor substrate, in such a manner as to enable signal transmission. Compared to a conventional manufacturing process flow in which semiconductor substrates are cut into semiconductor chips (dicing) after the process of "BEOL (Back End Of Line)" and the diced semiconductor chips are then formed into a

three-dimensional structure, the WOW configuration allows immediate transition from the process of "BEOL (Back End Of Line)" to the process of the three-dimensional structure formation using the pre-dicing semiconductor substrates. This simplifies the manufacturing process flow of semiconductor devices and also reduces the investment in mass production facilities.

In addition, the WOW process does not have a theoretical limit for the number of semiconductor substrate layers to be stacked one over the other. That is, an integration degree according to the number of semiconductor substrate layers being stacked can be obtained. For example, if a semiconductor device is formed by stacking ten semiconductor substrates in the WOW configuration, a memory device formed of the semiconductor device with, for example, 32 GB per semiconductor chip has capacity of 320 GB, and about 1000 pieces of three-dimensional chips can be obtained. If, in a logic device, a CPU core unit and a cache unit are separately formed in different semiconductor substrates and disposed one above the other using the WOW process, multi-core architectures, such as 16-core, 32-core, 64-core..., can be achieved. If a massively multi-core architecture having 32 cores can be realized, the CPU core itself can be handled redundantly, which allows organization of a three-dimensional logic device having no effective defects.

Furthermore, in the WOW process, the wiring distance corresponds to the thickness of the semiconductor substrate, and devices can be therefore connected to each other in the range of about 20 μm even including the thickness of the device layers. This contributes to significant shortening of the wiring length, considering that the long wiring of usual circuits is in the range of

several hundred micrometers to several tens of millimeters. Accordingly, the application of the WOW process to signal wiring enables high-speed information transfer with a large bus bandwidth per unit via hole.

Thus, the preferred embodiments of the present invention have been described in detail; however, it should be understood that the present invention is not limited to the above-described particular embodiments and various changes and modification may be made to the particular embodiments without departing from the scope of the present invention.

For example, in each of the embodiments, the description is given with an example of using semiconductor substrates (silicon wafers) having a circular shape in a planar view; however, the shape of the semiconductor substrates is not limited to a circular shape, and may be a panel shape, such as a rectangular shape in a planar view.

In addition, the material of the substrates on which the semiconductor integrated circuits are formed is not limited to silicon, and may be germanium or sapphire, for example.

In addition, in each of the embodiments above, the description is given with an example of connecting semiconductor chips, which constitute layered semiconductor substrates, to each other by an electrical signal via metal layers formed in via holes; however, the connection between the semiconductor chips constituting the layered semiconductor substrates does not have to be made by an electrical signal, and may be made by a light signal. In this case, optical waveguides may be formed in the via holes in place of the metal layers.

In addition, in each of the embodiments above,

the description is given with an example of forming the via holes after the formation of the electrode pads on the semiconductor substrates; however, the electrode pads may be formed after the formation of the via holes. Furthermore, a process (damascene process) of grinding the top surfaces of the metal layers formed in the via holes by CMP (Chemical Mechanical Polishing) or the like may be provided.

In addition, in each of the embodiments above, the description is given with an example of forming the depression in the semiconductor substrate in such a manner as to reduce the thickness of the central portion and its vicinity while leaving the fringe portion. The formation of the depression is made so that the semiconductor substrate with a reduced thickness maintains sufficient rigidity. Accordingly, as long as the semiconductor substrate maintains sufficient rigidity, the depression is not limited to a particular shape. For example, parts excluding the lattice sections may be reduced in thickness (i.e., plural depressions are formed).

In addition, the different connection configurations of the electrode pads and the via holes described in the above embodiments may be provided together in a single semiconductor device.

In addition, modification the same as that of the first embodiment may be applied to the second to fifth embodiments above.

The present international application claims priority based on Japanese Patent Application No. 2008-240015, filed on September 18, 2008, the entire contents of which are incorporated herein by reference.

DESCRIPTION OF THE REFERENCE NUMERALS

10, 10A, 10B, 10C semiconductor device

11, 11c, 21c, 31c, 41c, 51c, 61c, 71c semiconductor substrate

11a, 11b, 16a, 21a, 21b surface

11x fringe portion

12, 22 substrate body

13, 23 semiconductor integrated circuit

14, 24, 28 insulating layer

15, 15a, 15b, 25, 25a, 25b, 35, 35a, 35b, 45, 45a, 45b, 55, 55a, 55b, 65, 65a, 65b, 75, 75a, 75b electrode pad

16, 26, 36, 46, 56, 66, 76, 86 resin layer

21x depression

21y, 21z, 31y, 31z, 41y, 41z, 51y, 51z, 61y, 61z, 71y, 71z via hole

27, 37 resist film

29, 38, 38a, 39, 39a, 38b, 48, 48a, 58, 58a, 68, 68a, 78, 78a, 88, 88a metal layer

27x, 27y, 27z, 37x, 37y, 76x opening

81 structure layer

81c silicon substrate

81d insulating film

81x groove

91 external connection terminal

96 adhesion layer

97 support

A semiconductor chip formation region

B scribing region

C cutting position

D1, D2 depth

H1 height

T1-T3 thickness

φ1- φ7 diameter

CLAIMS

1. A semiconductor device manufacturing method of disposing one above another a plurality of semiconductor substrates each substrate having, on a main surface thereof, semiconductor chips each of which has a semiconductor integrated circuit, connecting the semiconductor chips, each of which constitutes a different one of the semiconductor substrates, in such a manner as to enable signal transmission, and subsequently singularizing the semiconductor chips into individual pieces, the semiconductor device manufacturing method comprising:

a first step of preparing a first semiconductor substrate and a second semiconductor substrate;

a second step of reducing a thickness of the second semiconductor substrate;

a third step of firmly fixing an opposite surface of the second semiconductor substrate with the reduced thickness to the main surface of the first semiconductor substrate via an insulating layer, the opposite surface being opposite to the main surface of the second semiconductor substrate;

a fourth step of forming, in the second semiconductor substrate with the reduced thickness, a via hole which penetrates from the main surface to the opposite surface of the second semiconductor substrate; and

a fifth step of forming a connection part which enables the signal transmission, via the via hole, between the semiconductor chip of the first semiconductor substrate and the semiconductor chip of the second semiconductor substrate.

2. The semiconductor device manufacturing method as claimed in claim 1, further comprising:

a sixth step of preparing a semiconductor substrate different from the first semiconductor substrate and the second substrate, and disposing the different semiconductor substrate on the second semiconductor substrate by performing steps similar to the second, the third, the fourth and the fifth steps on the different semiconductor substrate.

3. The semiconductor device manufacturing method as claimed in claim 1, wherein in the second step, only a predetermined region of the second semiconductor substrate is reduced in thickness.

4. The semiconductor device manufacturing method as claimed in claim 3, wherein the predetermined region is a region, within the second semiconductor substrate, other than a fringe portion of the second semiconductor substrate.

5. The semiconductor device manufacturing method as claimed in claim 4, further comprising:

a first removing step of removing a fringe portion of the first semiconductor substrate, wherein the first removing step is performed prior to the third step.

6. The semiconductor device manufacturing method as claimed in claim 5, further comprising:

a second removing step of removing the fringe portion of the second semiconductor substrate, wherein the second removing step is performed prior to the third step.

7. The semiconductor device manufacturing method as claimed in claim 1, wherein each of the semiconductor substrates has a substantially circular shape in a planar view.

8. The semiconductor device manufacturing method as claimed in claim 1, wherein the connection part connects the semiconductor chip of the first semiconductor substrate and the semiconductor chip of the second semiconductor substrate by an electrical signal.

9. The semiconductor device manufacturing method as claimed in claim 1, wherein the connection part connects the semiconductor chip of the first semiconductor substrate and the semiconductor chip of the second semiconductor substrate by a light signal.

10. The semiconductor device manufacturing method as claimed in claim 1, wherein a structure layer having no semiconductor chip is included in the semiconductor substrates disposed one above the other, the structure layer being insulated from the semiconductor substrates.

11. The semiconductor device manufacturing method as claimed in claim 10, wherein the structure layer is one of a substrate, a metal layer and an insulating layer.

12. The semiconductor device manufacturing method as claimed in claim 10, wherein the structure layer has a function of cooling the semiconductor substrates.

13. The semiconductor device manufacturing method as claimed in claim 10, wherein the structure layer has a MEMS.

14. The semiconductor device manufacturing method as claimed in claim 1, wherein a reduced thickness of the second semiconductor substrate after the second process is five times or more a depth of element isolation in a device of the second semiconductor substrate.

15. The semiconductor device manufacturing method as claimed in claim 1, wherein a reduced thickness of the second semiconductor substrate after the second process is 1 μm or more.

16. The semiconductor device manufacturing method as claimed in claim 1, wherein the via hole formed in the fourth step has an aspect ratio of not less than 0.5 and not more than 5.