A Self-Aligned Vertical PNP Transistor for High Performance SiGe CBiCMOS Process

Abstract

A structure and a process for a self-aligned vertical PNP transistor for high performance SiGe CBiCMOS process. Embodiments include SiGe CBiCMOS with high-performance SiGe NPN transistors and PNP transistors. As the PNP transistors and NPN transistors contained different types of impurity profile, they need separate lithography and doping step for each transistor. The process is easy to integrate with existing CMOS process to save manufacturing time and cost. As plug-in module, fully integration with SiGe BiCMOS processes. High doping Polysilicon Emitter can increase hole injection efficiency from emitter to base, reduce emitter resistor, and form very shallow EB junction. Self-aligned N+ base implant can reduce base resistor and parasitical EB capacitor. Very low collector resistor benefits from BP layer. PNP transistor can be Isolated from other CMOS and NPN devices by BNwell, Nwell and BN+ junction.

Figure 14