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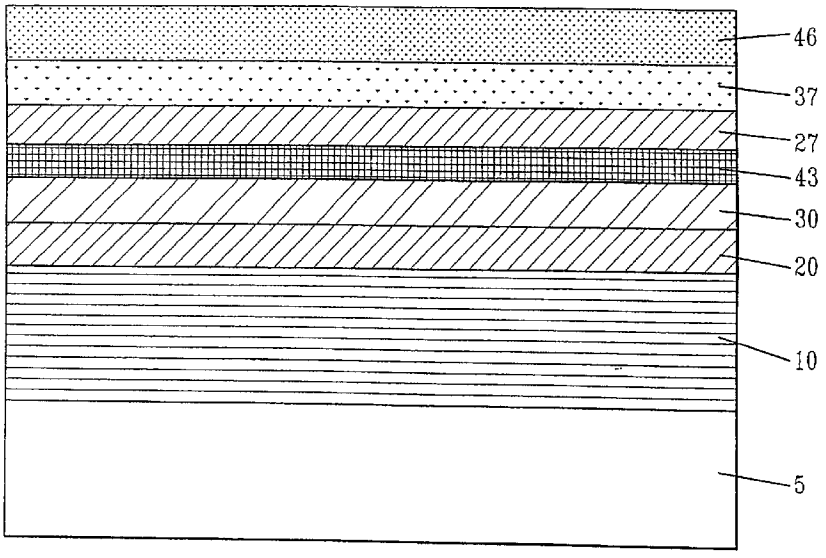
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(54) Title: RELAXED SiGe LAYERS ON Si OR SILICON-ON-INSULATOR SUBSTRATES BY ION IMPLANTATION AND THERMAL ANNEALING



(57) Abstract: A method to obtain thin (less than 300 nm) strain-relaxed $Si_{1-x}Ge_x$ buffer layers on Si or silicon-on-insulator (SOI) substrates. These buffer layers have a homogeneous distribution of misfit dislocations that relieve the strain, remarkably smooth surfaces, and a low threading dislocation (TD) density, i.e. less than $10^6 cm^2$. The approach begins with the growth of a pseudomorphic or nearlypseudomorphic $Si_{1-x}Ge_x$ layer, i.e., a layer that is free of misfit dislocations, which is then implanted with He or other light elements and subsequently annealed to achieve the substantial strain relaxation. The very effective strain relaxation mechanism operatiing with this method is dislocation nucleation at He-inducedplatelets (not bubbles) that lie below the $Si/Si_{1-x}Ge_x$ interface, parallel to the Si(001) surface.

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Declarations under Rule 4.17:

— *as to applicant's entitlement to apply for and be granted a patent (Rule 4.17(ii)) for the following designations AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BW, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NI, NO, NZ, OM, PG, PH, PL, PT, RO, RU, SC, SD, SE, SG, SK, SL, SY, TJ, TM, TN, TR, TT, TZ, UA, UG, UZ, VC, VN, YU, ZA, ZM, ZW, ARIPO patent (BW, GH, GM, KE, LS, MW, MZ, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HU, IE, IT, LU, MC, NL, PT, RO, SE, SI, SK, TR), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG)*

— *as to the applicant's entitlement to claim the priority of the earlier application (Rule 4.17(iii)) for all designations*

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