

RESERVE COPY. PATENT SPECIFICATION

DRAWINGS ATTACHED

107 L571

107 L571



Date of Application and filing Complete Specification: May 19, 1964.

No. 20655/64.

Application made in United States of America (No. 283805) on May 28, 1963.

Complete Specification Published: June 7, 1967.

© Crown Copyright 1967.

Index at acceptance: —H3 T(1C1, 2F, 2T3X, 2W2, 4EX); H1 K(1C1, 1CX, 2S20, 3E1D, 3E1M, 3J, 3P9, 3T1, 3X, 4C21, 4C23, 4F11G, 4F17, 4F20, 5C5); H4 L(14K, 14L)

Int. Cl.: —H 03 k 17/36//H 01 L, H 04 j

COMPLETE SPECIFICATION

Electronic Switching

We, RADIO CORPORATION OF AMERICA, a Corporation organized under the laws of the State of Delaware, United States of America, of 30, Rockefeller Plaza, City and State of New York, United States of America, do hereby declare the invention, for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement:—

This invention relates to electronic switching circuits; and more particularly to electronic switching circuits using field-effect transistors.

In synchronous detector circuits, chopper circuits and in similar circuits it is desirable to permit current flow in either direction through the switch when the switch is closed. However, circuits wherein a junction transistor is used as a bidirectionally conductive switching element, with the desired signal information applied in series with the emitter-collector electrodes of the transistors and a switching voltage applied to the base electrode, are subject to the problem that the desired signal information is contaminated by the switching voltage. The contamination includes a direct current (d-c) component developed across the base-emitter junction and an alternating current (a-c) component caused by switching currents flowing through the signal input and/or output circuits. Another problem encountered in switching circuits using junction transistors is that the range of desired signal amplitude for which the device exhibits linear characteristics is limited to a very small voltage.

It is therefore an object of this invention to provide an improved electronic switching circuit.

According to the present invention, there is provided an electronic switching circuit comprising a field effect transistor having a gate electrode and source and drain elec-

trodes defining a current path of bidirectional conductivity through said transistor, the gate electrode being separated by a high impedance insulating gap respectively from the source and drain electrodes; a controlled circuit including the current path, an input for bidirectional signal voltages and a load impedance element; and a varying switching signal voltage which is superimposed on the gate electrode, with or without a predetermined bias potential to determine the conductivity state of the current path, to change the conductivity of the current path as a function of the switching voltage.

It has been found that field-effect devices exhibit a linear resistance over a large range of applied source-to-drain voltages as compared to junction transistors. Hence, the utility of switching circuits embodying the invention is not, as a practical matter, limited by the amplitude of the applied signal voltage which can be tolerated.

Referring to the accompanying drawings:

FIGURE 1 is a diagrammatic view of a field-effect transistor suitable for use in circuits embodying the invention;

FIGURE 2 is a cross-sectional view taken along section line 2—2 of FIGURE 1;

FIGURE 3 is a graph showing a family of drain current versus source-to-drain voltage curves for various values of gate-to-source voltages for the transistor of FIGURES 1 and 2;

FIGURE 4 is a schematic circuit diagram of a switching circuit according to the invention;

FIGURE 5 is a schematic circuit diagram of a synchronous detector circuit embodying a switching circuit of the invention;

FIGURE 6 is a schematic circuit diagram of another synchronous detector circuit embodying a switching circuit of the invention;

FIGURE 7 is a schematic circuit diagram

[Price 4s. 6d.]

transistor

of a chopper circuit embodying a switching circuit of the invention; and

FIGURES 8a, 8b and 8c are graphs of voltage waveforms useful in explaining the operation of the chopper circuit of FIGURE 7.

Referring now to FIGURE 1, an insulated gate field-effect transistor 10 which may be used with circuits embodying the invention includes a body 12 of a semiconductor material. The body 12 may be either a single crystal or polycrystalline and may be of any of the semiconductor materials used to prepare transistors in the semiconductor art. For example, the body 12 may be nearly intrinsic silicon, such as for example, lightly doped P-type silicon of 100 ohm cm. material.

In the manufacture of a device shown in FIGURE 1, heavily doped silicon dioxide is deposited over the surface of the silicon body 12. The silicon dioxide is doped with N-type impurities. By means of a photo-resist and acid etching, or other suitable technique, the silicon dioxide is removed where the gate electrode is to be formed, and around the outer edges of the silicon wafer as viewed on FIGURE 1. The deposited silicon dioxide is left over those areas where the source-drain regions are to be formed.

The body 12 is then heated in a suitable atmosphere such as in water vapour so that exposed silicon areas are oxidized to form grown silicon dioxide layers indicated by the stippled areas of FIGURE 1. During the heating process, impurities from the deposited silicon dioxide layer diffuse into silicon body 12 to form the source and drain regions. FIGURE 2, which is a cross-sectional view taken along section line 2—2 of FIGURE 1, shows the source-drain regions labelled S and D respectively.

By means of another photo-resist and acid etching or like step, the deposited silicon dioxide over part of the source-drain diffused regions are removed. Electrodes are formed for the source, drain and gate regions by evaporation of conductive materials through a mask. First chromium is put down to form a bonding film on which deposits of gold are formed by evaporation to provide non-oxidizing electrodes. Other suitable electrically conductive materials may be used.

The finished wafer is shown in FIGURE 1, in which the stippled area, between the outside boundary and the first more darkly stippled zone 14, is grown silicon dioxide. The white area 16 is the metal electrode corresponding to the source electrode. Dark zones 14 and 18 are deposited silicon dioxide zones overlying the diffused source region, and the dark zone 20 is a deposited silicon dioxide zone overlying the diffused drain region. White areas 22 and 24 are the metallic electrodes which correspond to the gate

and drain electrodes respectively. The stippled zone 28 is a layer of grown silicon dioxide on a portion of which the gate electrode 22 is placed and which insulates the gate electrode 22 from the substrate silicon body 12 and from the source and drain electrodes as shown in FIGURE 2. The input resistance of the device at low frequencies is approximately 10^{14} ohms.

The layer of grown silicon dioxide 28 on which the gate electrode 22 is mounted, overlies an inversion layer or channel C of controllable conductivity connecting the source and drain regions. The gate electrode 22 is disposed symmetrically between the source region S and the drain region D. If desired, the gate electrode 22 may be disposed towards the source region S and may overlap the deposited silicon dioxide layer 18.

It should be noted that electrodes D and S interchangeably operate as the drain and the source electrodes as a function of the polarity of the bias potential applied therebetween; i.e., the electrode to which a positive bias potential is applied (relative to the bias potential applied to the other electrode) operates as a drain electrode. The conduction of current through the channel C is by majority current carriers, in the present case electrons. If the device has an N-type substrate, and P-type source and drain regions, the majority current carriers are holes, and the electrode to which the negative terminal of a supply source is applied operates as the drain electrode.

The channel C, i.e., the source-to-drain current path, has controllable conductivity as shown by FIGURE 3. The conductivity of the channel C is a function of the amplitude and polarity of the applied gate-to-source voltage. FIGURE 3 is a family of curves 29—41 illustrating the linear portion below the knee of the drain current versus drain voltage characteristic of the insulated gate field-effect transistor shown in FIGURE 1 connected in a common source configuration. In FIGURE 3, drain-to-source voltage is represented in volts along the abscissa; and drain current in milliamps along the ordinate.

In order to more easily explain the conditions for obtaining the curves shown in FIGURE 3, one of the two electrodes will always be referred to as the drain electrode regardless of the polarity of the bias voltage applied thereto, and the other electrode will be referred to as the source electrode. The curves 29—41 shown in the first quadrant in FIGURE 3 were obtained by applying a bias potential to the drain electrode which is positive with respect to the potential of the source electrode, and by biasing the gate electrode with respect to the source electrode by a voltage having a magnitude as indicated by the voltage of E_g (gate voltage) corresponding to each of the curves 29—41. The por-

70

75

80

85

90

95

100

105

110

115

120

125

130

1

2

3

3'

40

45

50

55

60

65

tion of the curves 29—41 corresponding to the third quadrant were obtained by reversing the polarity of the bias voltage applied between the source and drain electrodes, i.e., by applying a bias potential to the drain electrode which is negative with respect to the potential of the source electrode.

It should be noted that the drain current versus drain voltage characteristics shown in FIGURE 3 is substantially linear over a substantial range of drain voltages as compared to a bipolar or junction transistor. With a gate-to-source voltage corresponding to the curve 29, substantially no source-to-drain current flows, while a gate-to-source voltage corresponding to the curve 41, permits source-to-drain current as a linear function of applied source-to-drain voltage.

A feature of an insulated gate field-effect transistor is that it can be manufactured so that the zero gate bias voltage characteristic is at any one of the curves shown in FIGURE 3. In FIGURE 3, for example, the curve 41 corresponds to the zero bias voltage curve, as indicated by the notation $E_g = 0$. The location of the zero bias curve is established during the manufacture of the transistor, e.g., by controlling the time and/or temperature of the step of the process when the silicon dioxide layer 28 shown in FIGURES 1 and 2 is grown. The longer the transistor is baked and the higher the temperature, in a dry oxygen atmosphere, the larger the drain current will be for a given amount of drain voltage at zero bias between the source and gate electrodes. Hence, if desired, the curve 29 could be made to correspond to the zero gate bias condition, with the curves 30—41 corresponding to progressively more positive gate voltages.

Reference is now made to FIGURE 4 which is a schematic diagram of a switching circuit employing an insulated gate field-effect transistor 43 similar of the type described with reference to FIGURES 1 and 2. The transistor 43 has a source electrode 42, a drain electrode 44, and a gate electrode 46. The source electrode 42 is connected to a source of signals 48 which has an internal resistance indicated by the resistor 50 effectively in circuit between the source electrode 42 and ground. The drain electrode 44 is connected to a load circuit 52 which has a resistance indicated by the resistor 54 which completes the drain electrode 44 circuit to ground.

The transistor 43 operates as a switch to connect and disconnect the signal source 48 from the load 52. To control the conductivity of the source-to-drain path of the transistor 43, a single-pole double-throw switch 56 is connected to the gate electrode 46, so that in a first position of the switch the gate is connected through a resistor 58 and a source of direct voltage, shown as a battery

60 to ground; and in a second position of the switch 56, (the position illustrated in the drawing) the gate electrode is connected through a resistor 62 and a source of potential, shown as a battery 64, to ground.

Assume that the transistor 43 has a zero bias gate voltage characteristic corresponding to one of the curves 33—37 of FIGURE 3. When the switch 56 is in its first position, the gate electrode 46 is maintained at a positive potential with respect to ground, and the device operates to provide a low source-to-drain resistance as indicated by the curve 41 of FIGURE 3. Under these conditions, current flows in either direction between the signal source 48 and load 52. In addition, due to the very high d-c resistance between the source and gate electrodes, not only is there very little loading on the battery 60, but substantially no current from the battery 60 flows in the signal source or load circuits for any applied signal condition which would cause signal contamination.

When it is desirable to interrupt the circuit between the signal source 48 and load 52, the switch 56 is thrown to its second position, wherein the gate electrode 46 is held at a negative potential by the battery 64. The potential of the battery 64 is sufficiently negative that the source-drain path of the transistor 43 is cutoff and the device may be considered to be operating on the curve 29 of FIGURE 3.

If the transistor 43 has a zero bias gate voltage characteristic corresponding to the curve 41 of FIGURE 3, then the voltage supply source represented by the battery 60, and the resistor 58 can be eliminated and the left-hand stationary contact as viewed in FIGURE 4 of the switch 56 can be either directly grounded, or grounded through a direct current conductive impedance element such as a resistor or inductor. Alternatively, if the transistor 43 has a zero bias gate voltage characteristic corresponding to the curve 29 of FIGURE 3, then the battery 64, and resistor 62 can be eliminated, and the right-hand stationary contact as viewed in FIGURE 4 can be either directly grounded or grounded through a direct current conductive impedance element.

The principles of the invention are embodied in the synchronous detector circuit of FIGURE 5, wherein the conductivity of the field-effect transistor is switched electronically. Synchronous detectors, often referred to as product detectors, are useful for demodulating signal wave transmissions which include sideband information representative of two or more different message signals. Examples of such wave transmissions are suppressed carrier wave transmission, single or independent sideband transmission, quadrature sideband transmission and the like.

The synchronous detector circuit of

70

75

80

85

90

95

100

105

110

115

120

125

130

FIGURE 5 includes an insulated gate field-effect transistor 70 having a source electrode 72, a gate electrode 74 and a drain electrode 76. For the purposes of a generalized description it will be assumed that the transistor 70 has a zero bias gate electrode characteristic corresponding to the curve 33 of FIGURE 3.

Signals from a suitable source (not shown) are applied to the primary winding of a transformer 78, and are coupled to a secondary winding 80 which connects the source electrode 72 to a point of reference potential, shown as ground. The gate electrode 74 is biased to cutoff by a voltage divider comprising a pair of resistors 82 and 84 connected between ground and the negative terminal of a direct voltage source. A reference signal source (not shown) which provides a voltage of the original carrier frequency is applied to the primary winding of a transformer 86. Where more than one message signal is contained in the sidebands of the signal being demodulated, the reference voltage phase is adjusted to provide the desired relation to the sideband energy for proper separation of the message signals. The reference voltage is applied to the gate electrode 74 through a coupling capacitor 88.

The drain electrode 76 is coupled to a suitable utilization or load circuit, represented by a resistor 90, through a low-pass filter circuit including a series resistor 92 and a pair of shunt capacitors 94 and 96.

The reference voltage applied to the gate electrode 74 is of sufficient amplitude to drive the transistor 70 to a conductive condition represented by the curve 41 of FIGURE 3. During this interval signal currents from the input circuit can flow to the load 90 in either direction through the transistor 70. It should be noted that there is no direct voltage polarizing supply required, and hence d-c stability problems associated with supply voltage drift, device aging and the like are not encountered. By properly controlling the phase of the reference signal applied to the gate electrode 74 with respect to the phase of the signals applied to the source electrode 72, the input signals are sampled in a manner to derive the desired message signal. The low-pass filter comprising the resistor 92 and capacitors 94 and 96 serve to filter r-f components of the applied signal from the desired modulation products. Due to the very high impedance between the gate electrode 74 and either of the source or drain electrodes 72 and 76 respectively, very little current from the reference signal source flows in the input or output circuits of the synchronous detector to produce contamination of the desired signal.

The angle of sampling of the input signal applied to the source electrode 72 can be controlled as a function of the bias voltage applied to the gate electrode 74. For ex-

ample, as the negative voltage applied to the gate electrode 74 is increased, the angle of sampling of the input signal will be reduced, since a greater amount of the reference signal input swing will be required to overcome the increased reverse bias.

As mentioned above in connection with FIGURE 4, if the transistor 70 has a zero gate electrode bias characteristic corresponding to the curve 29 of FIGURE 3, the capacitor 88, the resistors 82 and 84, and the bias voltage supply can be eliminated and the secondary winding of the transformer 86 directly connected between the gate electrode 74 and ground.

A modification of the synchronous detector circuit wherein the signal input circuit and load circuit are connected in parallel between the source and drain electrodes of an insulated gate field-effect transistor is shown in FIGURE 6. The circuit of FIGURE 6 includes an insulated gate field-effect transistor 100 which can be of the type as described with reference to FIGURES 1 and 2. The transistor 100 is presumed to have a zero bias gate electrode characteristic corresponding to the curve 41 of FIGURE 3. If desired, a suitable positive biasing potential may be provided to maintain the gate electrode 102 at a positive potential with respect to ground and the source electrode 104.

A signal input source, not shown, which has a high impedance relative to the minimum resistance exhibited between the source and drain electrodes of the transistor 100 is coupled to the input terminals 106. The input terminals 106 are capacitively coupled through a coupling capacitor 108 between the source and drain electrodes of the transistor 100. A reference input signal is applied to the terminals 110. The reference signals are coupled through a capacitor 112 and across resistor 114 connected between the gate electrode 102 and source electrode 104. An output or utilization circuit having a resistance represented by the resistor 116 is connected between the source and drain electrodes by way of a low-pass filter comprising a pair of series resistors 118 and 120 and a pair of shunt capacitors 122 and 124.

In operation, the transistor 100 serves as a switch to short out the desired signal applied to the terminals 106 except during the sampling interval. Accordingly, as the reference signal swings positively, the transistor 100 remains in its high conduction condition, and effectively shorts the input terminals. When the reference signal swings sufficiently negative to cutoff the transistor 100, the signal applied to the terminals 106 is fed to the output circuit, with the r-f components being filtered by the resistor 120 and capacitors 122 and 124.

FIGURE 7 is a schematic circuit diagram of a chopper circuit for converting a

direct-voltage (slowly varying voltage) to an alternating voltage amplitude modulated as a function of the original direct voltage. The chopper circuit includes an insulated gate field-effect transistor 130 having a source electrode 132, drain electrode 134 and gate electrode 136. A direct voltage source 138 is coupled to the drain electrode 134, with the internal resistance of the signal source 138, represented by the resistor 140, provided a d-c path between the drain 134 and a point of reference potential shown as ground.

A source of switching voltage 142 is coupled through a transformer 144, the secondary winding 146 of which is connected between the gate electrode 136 and the source electrode 132. The switching voltage which comprises essentially a square voltage wave as shown in FIGURE 8, may be coupled between the gate and either of the source and drain electrodes in any suitable manner.

A load resistor 148 is connected between the source electrode 132 and ground and chopped signals developed thereacross are coupled by way of the capacitor 150 to a load circuit 152. The load circuit 152 may comprise an a-c amplifier of a kind known in the art, with means for synchronously demodulating the amplified a-c signal.

The operation of the chopper circuit of FIGURE 7 will be explained with reference to the graphs of FIGURES 8a, 8b and 8c. The graph of FIGURE 8a represents the slowly varying direct voltage from the d-c signal source 138 applied to the drain electrode 134. The graph of FIGURE 8b represents the switching or chopping voltage waveform from the switching voltage source 142 which is applied between the gate electrode 136 and source electrode 132. The graph of FIGURE 8c represents the resultant a-c signal which is developed across the resistor 148 and coupled to the load 152. It will be noted that the resultant a-c signal is a suppressed carrier, amplitude modulated as a function of the slowly varying a-c voltage from the signal input source 138.

The switching voltage source 142 provides a signal of sufficient amplitude to drive the transistor 130 between cutoff and a relatively highly conductive condition. When the gate electrode 136 is positive relative to the source electrode 132, the transistor is conductive, and the voltage across the signal source 138 appears across the resistor 148. The resistance of the resistor 148 is made large relative to the minimum source-to-drain resistance of the transistor 130 to prevent excessive d-c signal voltage drop across the transistor. When the gate electrode 136 is driven negatively relative to the source electrode 132, the transistor 130 is cutoff, and the voltage across the resistor 148 is zero as shown in FIGURE 8c. The continuous or periodic chopping converts the direct voltage to an amplitude

modulated a-c wave which can be amplified without severe drift problems in a-c amplifiers. It will be noted, that a reversal in polarity of the applied direct voltage as indicated by the right-hand portion of FIGURE 8a does not affect the operation of the circuit because of the bidirectional conduction capabilities of the transistor 130.

The chopper circuit of FIGURE 7 provides excellent operational characteristics without contamination of the chopped output signal developed across the resistor 148 by the switching voltage. As discussed hereinbefore, where junction transistors are used as choppers, the switching voltage developed across the emitter-base path of the transistor appears across the output resistor even with zero input voltage from the signal source. This undesired emitter-base voltage, which is known as an offset voltage, is temperature responsive, and must be compensated if the chopper is to provide acceptable operation. In the junction transistor art, two transistors were connected back-to-back, and simultaneously switched, to compensate for the offset voltage.

The chopper circuit of FIGURE 7 requires only a single insulated gate field-effect transistor to provide contamination free chopping action. Since there is no rectifying junction between the gate electrode 136 and source electrode 132, the gate electrode can be driven either positive or negative relative to the source electrode without producing significant gate current. Accordingly, the power demand on the switching voltage source 142 is low. Furthermore, the high gate impedance permits flexibility of design, in that the end of the secondary winding 146 can be disconnected from the source electrode 132 and connected to ground without introducing appreciable contamination of the output signal by the switching signal.

Although the circuits of FIGURES 4-6 have been described in connection with an insulated gate field-effect transistor having a P-type semiconductor substrate, other types of insulated gate devices may be used. For example, a complementary conductivity type device having an N-type semiconductor substrate may be used. Alternatively, other types of insulated gate devices may also be used such as thin film devices formed on an insulating support.

WHAT WE CLAIM IS:—

1. An electronic switching circuit comprising a field effect transistor having a gate electrode and source and drain electrodes defining a current path of bidirectional conductivity through said transistor, the gate electrode being separated by a high impedance insulating gap respectively from the source and drain electrodes; a controlled circuit including the current path, an input for bidirectional sig-



direct-voltage (slowly varying voltage) to an alternating voltage amplitude modulated as a function of the original direct voltage. The chopper circuit includes an insulated gate field-effect transistor 130 having a source electrode 132, drain electrode 134 and gate electrode 136. A direct voltage source 138 is coupled to the drain electrode 134, with the internal resistance of the signal source 138, represented by the resistor 140, provided a d-c path between the drain 134 and a point of reference potential shown as ground.

A source of switching voltage 142 is coupled through a transformer 144, the secondary winding 146 of which is connected between the gate electrode 136 and the source electrode 132. The switching voltage which comprises essentially a square voltage wave as shown in FIGURE 8, may be coupled between the gate and either of the source and drain electrodes in any suitable manner.

A load resistor 148 is connected between the source electrode 132 and ground, and chopped signals developed thereacross are coupled by way of the capacitor 150 to a load circuit 152. The load circuit 152 may comprise an a-c amplifier of a kind known in the art, with means for synchronously demodulating the amplified a-c signal.

The operation of the chopper circuit of FIGURE 7 will be explained with reference to the graphs of FIGURES 8a, 8b and 8c. The graph of FIGURE 8a represents the slowly varying direct voltage from the d-c signal source 138 applied to the drain electrode 134. The graph of FIGURE 8b represents the switching or chopping voltage waveform from the switching voltage source 142 which is applied between the gate electrode 136 and source electrode 132. The graph of FIGURE 8c represents the resultant a-c signal which is developed across the resistor 148 and coupled to the load 152. It will be noted that the resultant a-c signal is a suppressed carrier, amplitude modulated as a function of the slowly varying a-e voltage from the signal input source 138.

The switching voltage source 142 provides a signal of sufficient amplitude to drive the transistor 130 between cutoff and a relatively highly conductive condition. When the gate electrode 136 is positive relative to the source electrode 132, the transistor is conductive, and the voltage across the signal source 138 appears across the resistor 148. The resistance of the resistor 148 is made large relative to the minimum source-to-drain resistance of the transistor 130 to prevent excessive d-c signal voltage drop across the transistor. When the gate electrode 136 is driven negatively relative to the source electrode 132, the transistor 130 is cutoff, and the voltage across the resistor 148 is zero as shown in FIGURE 8c. The continuous or periodic chopping converts the direct voltage to an amplitude

modulated a-c wave which can be amplified without severe drift problems in a-c amplifiers. It will be noted, that a reversal in polarity of the applied direct voltage as indicated by the right-hand portion of FIGURE 8a does not affect the operation of the circuit because of the bidirectional conduction capabilities of the transistor 130.

The chopper circuit of FIGURE 7 provides excellent operational characteristics without contamination of the chopped output signal developed across the resistor 148 by the switching voltage. As discussed hereinbefore, where junction transistors are used as choppers, the switching voltage developed across the emitter-base path of the transistor appears across the output resistor even with zero input voltage from the signal source. This undesired emitter-base voltage, which is known as an offset voltage, is temperature responsive, and must be compensated if the chopper is to provide acceptable operation. In the junction transistor art, two transistors were connected back-to-back, and simultaneously switched, to compensate for the offset voltage.

The chopper circuit of FIGURE 7 requires only a single insulated gate field-effect transistor to provide contamination free chopping action. Since there is no rectifying junction between the gate electrode 136 and source electrode 132, the gate electrode can be driven either positive or negative relative to the source electrode without producing significant gate current. Accordingly, the power demand on the switching voltage source 142 is low. Furthermore, the high gate impedance permits flexibility of design, in that the end of the secondary winding 146 can be disconnected from the source electrode 132 and connected to ground without introducing appreciable contamination of the output signal by the switching signal.

Although the circuits of FIGURES 4-6 have been described in connection with an insulated gate field-effect transistor having a P-type semiconductor substrate, other types of insulated gate devices may be used. For example, a complementary conductivity type device having an N-type semiconductor substrate may be used. Alternatively, other types of insulated gate devices may also be used such as thin film devices formed on an insulating support.

WHAT WE CLAIM IS:—

1. An electronic switching circuit comprising a field effect transistor having a gate electrode and source and drain electrodes defining a current path of bidirectional conductivity through said transistor, the gate electrode being separated by a high impedance insulating gap respectively from the source and drain electrodes; a controlled circuit including the current path, an input for bidirectional sig-

- nal voltages and a load impedance element; and a varying switching signal voltage which is superimposed on the gate electrode, with or without predetermined bias potential to determine the conductivity state of the current path; to change the conductivity of the current path as a function of the switching voltage. 20
- 5 2. A switching circuit according to claim 1 in which the gate electrode is also coupled to ground. 25
- 10 3. An electronic switching circuit according to Claim 1 or Claim 2 when operated as a synchronous detector, wherein the input signal includes message signals to be detected, and a reference voltage source with said bias potential is connected between the gate electrode and ground or a source of said bias potential to provide the switching signal voltages to said gate electrode to sample the message signals. 30
4. An electronic switching circuit according to Claim 3, wherein conduction through said transistor effectively shorts out the load and sampling of the input signal source is effective when the transistor is cut off by a negative gate electrode bias.
5. An electronic switching circuit according to Claim 1 or Claim 2, when operated as a chopper circuit wherein a slowly varying direct voltage source provides the source of bidirectional signal voltages.

A. M. & WM. CLARK,
Chartered Patent Agents,
5, Stone Buildings, Lincoln's Inn,
London W.C.2.

Leamington Spa; Printed for Her Majesty's Stationery Office by the Courier Press.—1967.

Published at The Patent Office, 25, Southampton Buildings, London, W.C.2, from which copies may be obtained.



* C L M S *