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(54) IMPROVEMENTS IN OR RELATING TO THE FABRICATION OF SEMICONDUCTOR DEVICES

(71) We, FAIRCHILD CAMERA AND INSTRUMENT CORPORATION 464 Ellis Street, Mountain View California 94042 U. S. A. a corporation of the State of Delaware, U.S.A., do hereby declare the invention, for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement:—

This invention relates to a process for fabricating at least one oxide-isolated semiconductor device in a semiconductor substrate and to an oxide-isolated semiconductor structure.

The at least one semiconductor device can comprise a family of devices for example vertical bipolar transistors, complementary oxide-isolated lateral bipolar transistors, or composite bipolar transistors merging both a vertical and a lateral bipolar transistor.

It is generally desirable to produce both vertical bipolar transistors and complementary lateral bipolar transistors using the same process steps. Vertical bipolar transistors, particularly vertical NPN's, are the most widely used device in bipolar integrated circuit design. The electron mobility in NPN's is greater than the hole mobility in PNP's. In such vertical bipolar transistors the base width can be accurately controlled and can be made as small as 0.1 micron by thermal diffusion or ion-implantation techniques. Thus, high device gain, β, can be achieved over a wide range of currents in small areas using controlled processing. When vertical bipolar transistors are used in the inverted mode, they are useful for common emitter/multi-collector structures which are frequently used in logic functions.

Such structures can be realized by using a common buried layer as the emitter with separate collectors being formed in the surface of the epitaxial layer. This concept is disclosed in U. S. Patent No. 3,244,950 issued to J. P. Ferguson. Lateral bipolar transistors, such as lateral PNP's, are highly useful for such applications as level shifters, active loads and current mirrors. See R. J. Widler, *Journal of Solid-State Circuits*, Vol. SC-4, No. 4, August 1969. While it is within the state of the art to produce vertical bipolar transistors and complementary lateral bipolar transistors on the same chip, typically such joint fabrication requires that additional sequences of process steps be utilized in order to provide optimal versions of the two types of devices. It would be desirable, then, to be able to produce vertical bipolar transistors, i.e., vertical NPN's and complementary lateral bipolar transistors, i.e., lateral PNP's using the same process steps so that both types of devices can be incorporated on the same chip without additional process steps which usually lower yield and increase cost.

A new type of logic called integrated injection logic (also called merged transistor logic) has been proposed. It is a radically different but remarkably simple form of bipolar logic. Integrated injection logic (commonly abbreviated I^2L) reduces a gate to a complementary transistor pair. This complementary transistor pair may be integrated into a single device if the lateral device, e.g., a lateral PNP, is used as the current source for the base of the vertical device, e.g., a vertical NPN, which is operating in an inverse mode. See *Electronics*, February 21, 1974, pp. 92—95. See also Hart et al, "Bipolar LSI Takes New Direction with I^2L", *Electronics*, October 3, 1974, pp. 111. The origin of this concept is found in two papers delivered to the IEEE International Solid-State Circuits Conference in February 1972. See H. H. Berger and S. K. Wiedman, "Merged Transistor Logic—a low-cost bipolar logic", Digest, 1972 ISSCC, pp. 90—91, *Journal of Solid-State Circuits*, Vol. 7, No. 5,

October 1972, pp. 340—346, and C. J. Hart and A. Slob, "Integrated Injection Logic—A New Approach to LSI", Digest 1972 ISSCC, pp. 92—93, *Journal of Solid-State Circuits*, October 1972, Vol. 7, No. 5, pp. 346—351. As described in these articles, integrated injection logic possesses the inherent advantage of being able to reduce the size of circuit elements since gates are reduced to a single device format, possesses an inherently low propagation-delay power product as a result of low operating voltage and capacitance, and can generally be fabricated with as few as five masks. Using an additional masking step to form a buried layer associated with each silicon island, logic families such as T^2L, ECL and DTL may be fabricated on the same chip. Since each gate, as stated above, is comprised of a complementary transistor pair, it is desirable to be able to fabricate complementary transistor pairs, e.g., a vertical bipolar NPN and a complementary transistor pair may be integrated into the same device, it is especially desirable to be able to make a composite structure which incorporates a vertical bipolar transistor and a complementary lateral bipolar transistor.

Oxide-isolated devices are known to provide significant advantages over junction-isolated or cut-and-fill-isolated devices. The employment of Isoplanar oxide-isolation, as disclosed in U. S. Patent 3,648,125 issued to Peltzer, particularly in the walled emitter format (see W. D. Baker et al, "Oxide Isolation Brings High Density to Production Bipolar Memories", *Electronics*, March 29, 1973, pp. 67), accomplishes the objective of inter-device isolation, achieves high packing densities, reduces sidewall capacitances and reduces direct current losses for vertical bipolar devices. It would clearly be desirable, then, to be able to fabricate the merged complementary transistor pair described above utilizing oxide isolation. However, even though vertical bipolar transistors fabricated in the preferred walled emitter format have a considerably improved inverse gain, it is found that inversion of the base occurs between the emitter and collector along the oxide wall. This inversion occurs because charges in the oxide induce charges of opposite polarity at the silicon surface. For example, the charges due to Q_{ss} and sodium ions are positive and induce a negative charge at the silicon surface. See Bruce E. Deal, "The Current Understanding of Charges in the Thermally Oxidized Silicon Structure", *Journal of Electrochemical Society*, Vol. 121, No. 6, June 1974, pp. 198C. In the case of a p-type silicon region, the presence of these charges depletes the p-type concentration and can invert the surface of the region to n-type. In addition, the p-type silicon is normally doped with boron which, during the oxidation process, preferentially segretates into the oxide and results in a lower concentration of boron at the surface than in the bulk silicon. To prevent this inversion, additional impurities of the same conductivity type as the base are introduced to the oxide wall adjacent the boundary with the base (see U. S. Patent 3,648,125 issued to Peltzer; W. J. Evans et al, "Oxide-Isolated Monolithic Technology and Applications", *Journal of Solid-State Circuits*, Vol SC-8, No. 5, October 1973, pp. 373—379); these impurities are sometimes called field implants because they are implanted in the field oxide regions and are sometimes called guard rings because they guard the periphery of active regions from inversion. If the alternative of a more heavily doped base region is used, the beta of the vertical bipolar transistor is severely reduced because the beta (ratio of collector current to base current) is inversely related to the base impurity concentration; the result is that the use of a heavily doped base reduces the beta below normally acceptable values. The use of a p-type impurity in the oxide wall adjacent the boundary with the base, as stated above, can alleviate this problem, but since the base of the vertical bipolar transistor is also the collector of the lateral bipolar transistor and has the same conductivity type as the emitter of the complementary lateral bipolar transistor, the guard ring in the oxide wall tends to allow conduction between the emitter and collector of the lateral bipolar device, i.e., the solution to the inversion problem for the vertical bipolar transistor creates a new inversion problem for the lateral bipolar transistor, if one postulates a structure merging a lateral bipolar transistor and a complementary vertical bipolar transistor into a composite injection-logic gate.

The present invention provides a process for fabricating at least one oxide-isolated semiconductor device in a semiconductor substrate, comprising:

growing a doped epitaxial layer on said semiconductor substrate, said epitaxial layer being of conductivity type opposite to the conductivity type of said substrate;

forming a groove in said epitaxial layer, said groove laterally surrounding and defining a device region;

applying an impurity to selected regions of said groove to form a guard ring at selected portions of an interface between the device region and an oxide-isolation region to be formed in the groove, said impurity being of a

conductivity type opposite to the conductivity type of said epitaxial layer;

forming an oxide of said semiconductor in said groove to form the oxide-isolation region; and

forming at least one semiconductor device in said device region.

In a preferred embodiment in which vertical bipolar transistors and complementary lateral bipolar transistors are merged into an injection-logic gage, the step of forming a groove is effected by applying a first insulation material in a selected pattern over the epitaxial layer to define oxide-isolation regions and device regions and by etching those areas in which oxide-isolation regions will be formed and the step of selectively applying an impurity to the grooves is accomplished by applying a self-aligned base insulation material over those portions of the grooves which bound the region between the base of any vertical bipolar transistor to be formed and the emitter of any lateral bipolar transistor to be formed and by applying the impurity.

The invention also provides an oxide-isolated semiconductor structure comprising:

an epitaxial layer overlaying a semiconductor substrate, said epitaxial layer being of a conductivity type opposite to the conductivity type of said substrate;

an oxide-isolation region composed of an oxide of said semiconductor and formed in a groove within said epitaxial layer, said oxide isolated region laterally surrounding and defining a device region, said device region having a guard ring formed at selected portions of the interface between said oxide-isolation region and said device region and containing an impurity of a conductivity type opposite to the conductivity type of the epitaxial layer; and

at least one semiconductor device formed in the device region.

The semiconductor device may be a discrete vertical bipolar transistor capable of operation in the conventional or in the inverse mode, a discrete lateral bipolar transistor of a composite structure in which a vertical bipolar transistor and a lateral bipolar transistor are merged together on the same silicon island to form an injection-logic gate so that the base of the vertical bipolar transistor serves as the collector of the lateral bipolar transistor, the vertical transistor being operated in the inverse mode.

For a more complete understanding of the present invention reference may be made to the following illustrative description and the accompanying drawings, in which:

Figure 1 is a cross-sectional view of a semiconductor substrate having buried layer regions formed in the surface thereof;

Figure 2 is a further cross-sectional view of Figure 1 after growth of a doped epitaxial semiconductor layer;

Figure 3 is a further cross-sectional view of Figure 2 wherein the epitaxial layer is etched to form grooves in which oxide-isolation regions will be formed;

Figure 4A is further cross-sectional view of Figure 4 after application of the self-aligned base insulation material and introduction of the additional impurities to form the guard ring or field implant;

Figure 4B is a plan view of the cross-sectional view of Figure 4A;

Figure 4C is a sectional view taken from Figure 4B as indicated and illustrates the relationship of the self-aligned base insulation material to the underlying structure;

Figure 5A is a further view of the cross-section of Figure 4A after the thermal growth of the oxide-isolation regions in the etched grooves and outward migration of the additional impurities to form a guard ring;

Figure 5B is a plan view of the cross-section of Figure 5A;

Figure 5C is a sectional view taken from Figure 5B as indicated;

Figure 5D is a sectional view taken from Figure 5B as indicated;

Figure 6 is a further view of the cross-section of Figure 5A after formation of the vertical transistor base/lateral transistor collector and the lateral transistor emitter/injector;

Figure 7 is a further view of the cross-section of Figure 6 after formation of the vertical transistor emitters/inverse collectors and formation of the vertical transistor inverse emitter contact;

Figure 8 is a further view of Figure 7 after formation of the base contact for the vertical transistor and the resultant increase in concentration of the impurity in the injector region;

Figure 9 is a cross-section in pictorial form of the merged injection-logic gate formed by the process of the present invention;

Figure 10 is a logic diagram for the injection-logic gate of Figure 9;

Figure 11 is a graph showing the propagation-delay power relationship for devices fabricated with various technologies including Isoplanar injection-logic devices;

Figure 12 is a graph showing the qualitative interdependence of the β of the vertical transistor in the inverse mode

(inverse β NPN) and the β of the complementary lateral transistor (β PNP) in the oxide-isolated merged injection-logic gate structure of the present invention;

Figure 13 is a cross-sectional view of an intermediate process step for a modified standard process taken generally from Figure 4A after the silicon nitride layer has been selectively etched and injector, base and base contact regions have been formed;

Figure 14 is a cross-sectional view of Figure 13 after selective growth of a silicon dioxide layer on the area not covered by silicon nitride and implantation of lightly doped regions between segments of the base region and the base contact region;

Figure 15 is a further view of Figure 14 after selective removal of the silicon nitride layer in preparation for diffusion of the inverse collector/emitter region and the inverse collector contact for the vertical bipolar device; and

Figure 16 is a further view of Figure 15 after formation of the inverse collector/emitter regions, inverse collector contact and opening up of the base contact for the vertical bipolar device.

The concept of injection logic offers the prospect of powerful bipolar devices which can compete with metal-oxide-semiconductor devices on the basis of price per function, while retaining the speed advantage inherent to bipolar. The attainment of high density and a competitive price per function may only be completely realized, however, by employing oxide-isolated structures. With injection logic generally the merged nature of the devices, e.g., the combination of a vertical bipolar transistor and a lateral bipolar transistor with shared regions, introduces severe interdependencies between the operating parameters of the constituent devices. With the employment of the oxide-isolation walled emitter format, this difficulty may be compounded by the need to prevent emitter-to-collector inversion along the wall of the vertical, e.g., NPN, transistor.

In an injection-logic cell the α (ratio of collector current to emitter current) of the lateral injector device, e.g., the α of the lateral PNP, will determine overall efficiency. With an α of 0.5, fifty percent of the current reaches the base of the NPN and is useful current. In the case of large scale integration where several thousand injectors may be used, a high value of α is obviously desirable to minimize power dissipation. However, increasing α (and hence β, the ratio of collector current to base current) of the injector PNP device will result is an increase in the reverse α and the reverse β of the PNP device. Consequently, current due to reverse injection from the NPN base will tend to lower the β of the inversely operated NPN. This interdependence of operating parameters of the constituent devices is thus inherently a critical feature of injection-logic devices.

For an injection-logic cell to function, the constituent vertical bipolar transistor operating in inverse mode must have a $\beta > 1$. It is desirable to have a vertical transistor with an inverse β which is significantly greater than 1 since a faster switching time will be achieved. Figure 12 shows qualitatively the interdependence of the lateral PNP β (the a and a' curves) and the vertical NPN inverse β (the b and b' curves) for an oxide-isolated walled emitter injection-logic structure as the integrated impurity concentration in the base of the lateral PNP is varied.

$$(Q_B = \int_0^w N_x dx$$

where w=base width and N_x=impurities/volume in lateral PNP base). It can be seen from the a curves that for low impurity concentrations in the lateral PNP base the lateral PNP has a high β and from the b curves that the vertical NPN has low values of inverse β. The shift from the a' to the a curve is obtained by increasing the p-doping in the injector of the lateral PNP; the shift from the b' to the b curve is obtained by increasing the p-doping in the base contact of the vertical NPN. It can be seen that while the interdependence of the device parameters still exists for the a and b curves, higher values of β can be achieved on both devices due to the reduction in recombination current at the contact areas if the optimal p doping is carried out.

The present invention permits improved forms, to be obtained of the merged injection-logic structure as well as of discrete vertical transistors, e.g., vertical NPN's and lateral discrete transistors, e.g., lateral PNP's. This is accomplished by utilizing a low concentration of p-type impurities in the base of the vertical NPN transistor, with inversion along the base wall being prevented by guard ring. Shorting of the emitter to collector in the lateral PNP is prevented by a self-aligned base mask which permits the guard ring to be excluded from the base wall of the lateral PNP. Additionally, the implantation of p-type impurities in the emitter of the lateral transistor, e.g., lateral PNP, prior to application of the metallization layer, allows the β of the lateral PNP to be optimized by minimizing the recombination current at the emitter contact. And,

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further, the additional implantation of *p*-type impurities in the base contact region of the NPN minimizes the recombination current at the base contact to improve the inverse NPN β.

The fabrication of oxide-isolated injection-logic merged structures in accordance with a preferred embodiment of the present invention begins with the formation of buried layers 11 in a semiconductor substrate 10 as shown in Figure 1. As described above and in the cited references, this merged structure will ultimately comprise an injection-logic gate having a vertical NPN and a lateral PNP in which the base of the vertical NPN is also the collector of the lateral PNP. The buried layer permits the inverse emitter of the vertical bipolar device to be isolated from devices on other silicon islands on the same chip; if a common emitter is acceptable, such as with a chip containing only injection-logic devices, then this step may be omitted and the epitaxial layer, described below, may serve as the common inverse emitter for all devices. A suitable substrate would be a *p*-type single-crystal silicon material of (111) orientation with a concentration of *p*-type impurities in the range of 4×10^{14} to 5×10^{15} atoms/cm^2. Buried layer regions 11 may be formed by a standard photomasking step along with diffusion or implantation techniques and constitutes an n-type region with an impurity concentration between 1×10^{19} and 1×10^{20} atoms/cm^2 with the higher concentration being preferred. As used above and throughout this specification, the phrase "photomasking step" refers to the well-known sequence of applying a uniform layer of a photoresist polymer, selectively exposing the photoresist by radiation of an appropriate wavelength and developing the photoresist to leave a desired pattern, thereby allowing an active step such as diffusion to be performed. Then, typically, the photoresist is removed. The details of each individual masking step are not shown in the drawings and should be inferred from the use of the phrase "photomasking step". Next, an epitaxial layer 12, for example a layer of n-type single-crystal silicon, having an impurity concentration of 10^{16} n-type impurity atoms/cm^2 and thickness of 1.2 microns, is applied over the substrate and buried layers. As shown by the dotted line in Figure 2, the impurities in the buried layer will diffuse upwardly into the epitaxial layer so that the metallurgical interface between the substrate and epitaxial layer is slightly below the effective upper boundary of the buried layer.

A layer of insulating material 13, such as silicon nitride, as shown in Figure 3, is then applied over the layer of epitaxial silicon and defined by a photomasking step to expose the areas in which oxide-isolation regions are to be formed. The phrase "oxide-isolation regions" is used to denote the silicon dioxide masses which are grown in the epitaxial silicon layer and which serve to produce electrical isolation. See U.S. Patent 3,648,125 issued to D. L. Peltzer. Next, using standard etching techniques, the epitaxial layer is etched away to a depth of about 0.5 micron to produce grooves 14 in which the oxide-isolation regions will be formed.

A photomasking step is then employed to selectively apply self-aligned base insulating material 17 such as chemically deposited silicon dioxide, to the insulating layer 13. Self-aligned base insulating material 17 lies on two sides of the base region of the vertical transistor to be formed. It serves to separate the base region of the vertical transistor to be formed from the emitter/injector of the lateral transistor to be formed and covers the collector contact for the vertical transistor to be formed. Self-aligned base insulating material 17 forms a self-aligned base mask whose coverage is shown clearly in Figure 4B. Since this mask defines the width of the base of the vertical transistor, transistors of varying base width can be fabricated on the same die by varying the configuration of this mask. Thus, if discrete devices are to be fabricated along with the merged injection-logic structure, parameters such as breakdown voltage and beta can be tailored and transistors with different properties can be fabricated simultaneously. The device areas are those encompassed by grooves 14.

As shown in Figure 4C, the self-aligned base insulating material 17 covers those portions of the intersection of insulating material 13 and grooves 14 which lie between regions 20 and 21. Thus, subsequently, when impurities are applied to the exposed areas of grooves 14 to form a guard ring, they are introduced only adjacent region 20 and region 21 and not adjacent the region between them. The impurities will be of the same conductivity type as the base of the vertical NPN and will be of opposite conductivity type to the expitaxial layer, e.g., the impurities will be p-type, to prevent emitter-to-collector inversion along the wall of the base of the vertical NPN. These impurities are then introduced by a standard diffusion step to a shallow depth in the contours of the exposed area of groove 14, as shown by dotted line 18 in Figures 4A and 4C. Next, the isolation oxide is formed by thermal treatment or by the application of an oxidizing agent, and the impurities proceed

ahead of the oxide to form a guard ring as the oxide grows into the epitaxial layer of silicon.

Since no impurities were introduced to oxide wall underneath self-aligned base insulating material 17, no guard ring is formed between the PNP emitter and the NPN base. Also, no guard ring is formed adjacent the collector contact of the vertical NPN so that no spurious p-n junction is formed. As discussed above, the guard ring serves (1) to inhibit inversion of the p-type substrate between the buried collector regions of adjacent devices (see dotted line 32 of Figure 5A), (2) to inhibit inversion between inverse collector regions 37*a* or 37*b* (shown in Figure 7) and the inverse emitter region formed by buried layer 11, and (3) to provide preliminary doping for the emitter/injector region 35 of Figure 6. The guard dog ring can also serve to allow, if desired, electrical contact to the substrate from the surface of the epitaxial layer. In addition, in walled emitter devices the guard ring provides an effective low resistance path in the base of the NPN (see dotted line 33 in Figure 5B) and minimizes debiasing effects which would otherwise lead to lower switching speeds, and lesser fan-outs in injection-logic structures; without the guard ring this resistance could have a value of several tens of kilohms for walled structures. It can readily be seen that each oxide-isolation region 31 lies between two distinct structures such as structures 23 and 22, each of which is formed on its own silicon island. In this embodiment, structure 22 will become a merged injection-logic gate, but in other embodiments, described subsequently, this structure may be one of a variety of discrete devices. From the plan view of Figure 5B, it is evident that as the oxide grows to form the oxide-isolation regions, it extends sideways as well as downwardly so that the device regions 20 and 21 of structure 22 are somewhat diminished in size. Also, the *p*-type impurities of the guard ring have proceeded ahead of the oxide laterally as well as downwardly so that the guard ring extends into the device region 20 as shown by dotted line 33 in Figures 5B and 5C and into device region 21 as shown by dotted line 30 in Figure 5A.

Using a standard photomasking step and ion-implantation, the emitter/injector region 35 of the lateral PNP is produced, as shown in Figure 6. The concentration of the p-type impurities implanted in the injector region 35 adds to the p-type impurities of the guard ring so that the injector region 35 generally has a peak concentration of 5×10^{18} atoms/cm^2 at the top surface with a relatively constant concentration of 1×10^{18} atoms/cm^2 around its sides. At the same time, the base region 36 of the vertical NPN is produced between the two areas of self-aligned base insulating material 17. Next, parts of the layer of silicon nitride insulation material 13 are removed so that inverse collector regions 37*a* and 37*b* may be formed by standard diffusion or implantation techniques. These inverse collector regions will have a peak *n*-type concentration on the order of 5×10^{19} atoms/cm^2. An *n*-type emitter contact 38 for the buried layer emitter 11 can be formed in the same step. The silicon nitride 13 which remains over the injector region 35 prevents any alteration of that region. Next, contact openings are made by a photomasking step to injector region 35 and base region 36. At that point, an additional dosage of *p*-type impurities can be added to produce a heavily doped injector region 35 and a satisfactory base contact 40. This step is accomplished by utilizing the photoresist layer as a barrier to the implant and thus implanting the emitter/injector and the base contact region without adding to the *p*-type concentration in the base of the vertical NPN. Thus, this important step is achieved without an additional masking step.

As described above, the beta of the lateral PNP will be increased by the additional dose of *p*-type material to the emitter/injector. The base contact implant improves the beta of the vertical NPN operating in the inverse mode since there is no increase of the impurity concentration in the intrinsic base region, i.e., in the area underlying the inverse collectors, but only in the contact region so that the recombination current at that contact is minimized. The depth 41 of base region 36 is increased underneath the location of the base contact 40 but no harm is done to the vertical NPN parameters so long as buried collector region 11 is not contacted. The structure is then completed by the application of suitable conductive contacts.

The process used to fabricate the oxide-isolated merged injection-logic gate structure as described above can be generalized to a standard isoplanar process sequence which can be used to fabricate a large number of discrete devices as well. This standard sequence includes following steps for a *p*-substrate (for an *n*-substrate starting material, the conductivity types of the respective dopants would be reversed in each successive step):

1. Oxidize the p-substrate.
2. Mask to define the buried collector regions (inverse emitters in the injection-logic structure); diffuse n-type impurities in the buried collector regions and cross-unders.

3. Strip the oxide by etching and then grow n-type epitaxial silicon layers with a thickness on the order of 1 micron.
4. Deposit a layer of silicon nitride.
5. Mask to define oxide-isolation regions and etch grooves to a depth of about .5 microns.
6. Vapour-deposit layers of silicon dioxide to produce self-aligned base mask over boundary of base of lateral PNP and oxide-isolation region and over boundary of emitter contact of vertical NPN and oxide-isolation region.
7. Diffuse p-type impurities in exposed grooves.
8. Form or deposit oxide-isolation regions in grooves and diffuse guard ring ahead of oxide growth.
9. Ion-implant *p*-type impurities into all epitaxial silicon regions not covered with vapor-deposited oxide or isolation oxide to form emitter and collector of PNP and base of NPN.
10. Mask to define inverse collector region and buried layer contact of vertical transistor.
11. Diffuse n-type impurities into the inverse collector region and buried layer contact of vertical transistors.
12. Mash to expose the emitter/injector region of the lateral transistor and the base contact region and ion-implant *p*-type impurities into these regions.
13. Deposit metal to form the interconnecting layer, mask and define the interconnecting layer.

As can be seen, the standard process sequence takes a total of six masking steps, viz., steps 2, 5, 6, 10, 12 and 13.

The standard process sequence set forth in the preceding paragraph may be employed to produce a variety of devices without the addition of specific process steps. The primary devices are catalogued below:

1. Vertical NPN transistors in walled and non-walled format.
2. Lateral PNP transistors in walled and non-walled format.
3. Merged transistor logic cells.
4. Vertical PNP transistors with a substrate contact.
5. Vertical PNP transistors in low β version.
6. p-type resistors in walled or non-walled format.
7. Buried layer resistors.
8. Epitaxial resistors.
9. Pinched-base resistors.
10. p-channel field-effect transistors.
11. Pinched epitaxial resistors.
12. Epitaxial field-effect transistors.
13. Schottky devices providing an additional masking step is added to define the metal contact.

A variation of the standard process sequence set out above may be employed to produce a merged injection-logic gate which has improved speed and lower losses. The process is essentially the same through formation of the oxide-isolation regions and application of the self-aligned base, except that the self-aligned base does not extend to the oxide-isolation region (compare Figures 5A and 13).

After formation of the guard ring around the oxide-isolation regions as shown in Figure 5A, parts of the insulation layer 13 are removed as shown in Figure 13 to permit the formation by ion-implantation or diffusion of emitter/injector region 60, base region segments 61 and 62, and base contact segment 63. For the preferred merged injection-logic structure fabricated from a lateral PNP and a vertical NPN, these regions would be diffused p-regions with a peak concentration on the order of 1×10^{19} atoms/cm^2. Then, as shown in Figure 14, a screening material 70, such as a layer of thermally grown silicon dioxide 0.5 micron thick is formed on all exposed surfaces of the epitaxial layer. Using ion-implantation, a low concentration of p-type impurities with a peak concentration on the order of 5×10^{17} atoms/cm^2 is implanted underneath the still-exposed nitride regions to form base segments 65 and 66. A segmented base region is thereby formed which has alternating sections of heavy p-type concentration (regions 61, 62 and 63) and light p-type concentrations (regions 65 and 66). As shown in Figure 15, the nitride insulation layer is selectively removed above low concentration regions 65 and 66 and above the location of the inverse emitter contact 69 to be formed so that diffused inverse collector regions 67 and 68 may be formed in the base region. At the same time, inverse emitter contact region 69 is formed as shown in Figure 16. With the subsequent application of suitable metallization, a merged injection-logic gate structure is formed in which there is a high concentration of p-type material between adjacent inverse collectors and therefore a lower resistance. This lowers resistance even beyond the value achieved by the presence of the guard ring. Thus, debiasing under the collector is reduced at high current levels so that the speed of the injection-logic gate is improved. This means that the propagation delay-power product is lowered in the flat portion of the graph of Figure 11. Also, the β of a discrete lateral PNP is improved without requiring process steps which compromise the vertical transistor. And, the higher

concentration of *p*-type doping in the extrinsic base region minimizes current injected into this area from the buried layer emitter so that the d.c. characteristics of the inverse β of the vertical NPN are improved. The structure is effectively a self-aligned emitter structure which has heavy doping in the extrinsic base region and low doping in the intrinsic base region. Inherently this produces controllably high gains and diode-like structures if discrete devices are fabricated.

The processing sequence for this preferred modified standard process uses the first five steps of the standard process in identical form. After these five steps, the modified standard process includes the steps of:

6. Vapor-deposit a layer of silicon dioxide to produce a self-aligned base mask over boundary of base of lateral PNP and oxide-isolation region as well as between base contact region and inverse emitter contact region of vertical NPN.
7. Diffuse *p*-type impurities in exposed grooves.
8. Form isolation oxide regions and diffuse guard ring ahead of oxide growth.
9. Mask nitride regions and remove nitride except where n-type regions will be required.
10. Diffuse *p*-type impurities into areas not protected by nitride or isolation oxide and thermally treat to oxidize exposed epitaxial regions and to effect drive-in of the diffused impurities to form heavily doped extrinsic base segments and injection region.
11. Apply and define photoresist and ion-implant a low concentration of *p*-type impurities in between base segment regions to form intrinsic base segments of NPN transistors.
12. Etch nitride regions to define inverse collector regions and inverse emitter contact region for vertical NPN and diffuse n-type impurities.
13. Mask to define p contact regions. Ion-implant p-type impurities into contact regions if required.
14. Deposit metal to form the interconnecting layer, mask and define the interconnecting layer.

It can be seen that the modified standard process requires seven masking steps: 2, 4, 6, 9, 11, 13 and 14. This modified standard process can be used to fabricate the same catalogue of thirteen devices listed above for the standard process.

The merged structure of the injection-logic gate is shown in pictorial form in Figure 9. As described above, the merged structure 50, in the preferred embodiment, comprises a vertical NPN with multiple inverse collectors 52 and 53, base 51 and emitter 58, and a complementary lateral PNP with emitter/injector 56, base 55 and collector 51. The lateral PNP serves as a current injector and lead for the vertical PNP. Oxide-isolation regions 59 provide electrical isolation between adjacent structures and result in increased packing density. Sidewall capacitance between the emitter and base is also reduced as disclosed in A. Alberts et al, "Oxide-Isolation Integrated Injection Logic", 1974, *ISSCC Conf. Reports*, pp. 16 et seq. The merged structure 50 of the present invention has a guard ring along the interface between oxide wall 59 and base region 51 where they come in contact (not shown in Figure 9 but akin to the showing in Figures 4B and 5B). This guard ring allows the walled emitter format, without emitter-to-collector inversion along the interface between the base and the adjacent oxide-isolation region. The presence of the guard ring also enhances lateral conduction in the collector 51 of the PNP, a feature which is especially desirable if the contact to region 51 is placed on the side of inverse collectors 52 and 53 opposite emitter 56 so that current would have to pass through the constricted passageway underneath the inverse collectors. The guard ring is especially useful for achieving high fan-out since a high resistance would reduce the speed of the last collector in a circuit.

The logic diagram of the injection-logic gate of the composite structure of Figure 9 is shown in Figure 10. Merged structure 50 of Figure 9 will function as an injection-logic gate if terminal 80 is the injector, terminal 81 is the base input, terminals 82 and 83 are the collector contacts and terminal 84 is the emitter contact. In an optimal injection-logic device, such as the structure of the present invention, the emitter of the vertical transistor is close to the base to minimize current loss; this is accomplished without emitter-to-collector inversion by the selective use of a guard ring as described above. The walled emitter format further allows a high inverse emitter-to-base area ratio which allows optimization of the inverse βs to also be achieved. This optimization and the high betas for the constituent devices due to the heavy doping in the injector/emitter of the lateral device and the heavy doping in the base contact of the vertical device results in the low propagation delay versus power relationship shown in Figure 11.

WHAT WE CLAIM IS:—

1. A process for fabricating at least one

concentration of *p*-type doping in the extrinsic base region minimizes current injected into this area from the buried layer emitter so that the d.c. characteristics of the inverse β of the vertical NPN are improved. The structure is effectively a self-aligned emitter structure which has heavy doping in the extrinsic base region and low doping in the intrinsic base region. Inherently this produces controllably high gains and diode-like structures if discrete devices are fabricated.

The processing sequence for this preferred modified standard process uses the first five steps of the standard process in identical form. After these five steps, the modified standard process includes the steps of:

6. Vapor-deposit a layer of silicon dioxide to produce a self-aligned base mask over boundary of base of lateral PNP and oxide-isolation region as well as between base contact region and inverse emitter contact region of vertical NPN.
7. Diffuse *p*-type impurities in exposed grooves.
8. Form isolation oxide regions and diffuse guard ring ahead of oxide growth.
9. Mask nitride regions and remove nitride except where n-type regions will be required.
10. Diffuse *p*-type impurities into areas not protected by nitride or isolation oxide and thermally treat to oxidize exposed epitaxial regions and to effect drive-in of the diffused impurities to form heavily doped extrinsic base segments and injection region.
11. Apply and define photoresist and ion-implant a low concentration of *p*-type impurities in between base segment regions to form intrinsic base segments of NPN transistors.
12. Etch nitride regions to define inverse collector regions and inverse emitter contact region for vertical NPN and diffuse n-type impurities.
13. Mask to define p contact regions. Ion-implant p-type impurities into contact regions if required.
14. Deposit metal to form the interconnecting layer, mask and define the interconnecting layer.

It can be seen that the modified standard process requires seven masking steps: 2, 4, 6, 9, 11, 13 and 14. This modified standard process can be used to fabricate the same catalogue of thirteen devices listed above for the standard process.

The merged structure of the injection-logic gate is shown in pictorial form in Figure 9. As described above, the merged structure 50, in the preferred embodiment, comprises a vertical NPN with multiple inverse collectors 52 and 53, base 51 and emitter 58, and a complementary lateral PNP with emitter/injector 56, base 55 and collector 51. The lateral PNP serves as a current injector and lead for the vertical PNP. Oxide-isolation regions 59 provide electrical isolation between adjacent structures and result in increased packing density. Sidewall capacitance between the emitter and base is also reduced as disclosed in A. Allen et al, "Oxide-Isolation Integrated Injection Logic", 1974, *ISSCC Conf. Reports*, pp. 16 et seq. The merged structure 50 of the present invention has a guard ring along the interface between oxide wall 59 and base region 51 where they come in contact (not shown in Figure 9 but akin to the showing in Figures 4B and 5B). This guard ring allows the walled emitter format, without emitter-to-collector inversion along the interface between the base and the adjacent oxide-isolation region. The presence of the guard ring also enhances lateral conduction in the collector 51 of the PNP, a feature which is especially desirable if the contact to region 51 is placed on the side of inverse collectors 52 and 53 opposite emitter 56 so that current would have to pass through the constricted passageway underneath the inverse collectors. The guard ring is especially useful for achieving high fan-out since a high resistance would reduce the speed of the last collector in a circuit.

The logic diagram of the injection-logic gate of the composite structure of Figure 9 is shown in Figure 10. Merged structure 50 of Figure 9 will function as an injection-logic gate if terminal 80 is the injector, terminal 81 is the base input, terminals 82 and 83 are the collector contacts and terminal 84 is the emitter contact. In an optimal injection-logic device, such as the structure of the present invention, the emitter of the vertical transistor is close to the base to minimize current loss; this is accomplished without emitter-to-collector inversion by the selective use of a guard ring as described above. The walled emitter format further allows a high inverse emitter-to-base area ratio which allows optimization of the inverse βs to also be achieved. This optimization and the high betas for the constituent devices due to the heavy doping in the injector/emitter of the lateral device and the heavy doping in the base contact of the vertical device results in the low propagation delay versus power relationship shown in Figure 11.

WHAT WE CLAIM IS:—

1. A process for fabricating at least one

* C L M S *

oxide-isolated semiconductor device in a semiconductor substrate, comprising:

growing a doped epitaxial layer on said semiconductor substrate, said epitaxial layer being of a conductivity type opposite to the conductivity type of said substrate;

forming a groove in said epitaxial layer, said groove laterally surrounding and defining a device region;

applying an impurity to selected regions of said groove to form a guard ring at selected portions of an interface between the device region and an oxide-isolation region to be formed in the groove, said impurity being of a conductivity type opposite to the conductivity type of said epitaxial layer;

forming an oxide of said semiconductor in said groove to form the oxide-isolation region; and

forming at least one semiconductor device in said device region.

2. A process as claimed in claim 1 including before the step of growing a doped epitaxial layer the step of

forming a buried layer regin in said semiconductor substrate.

3. A process as claimed in claim 2 wherein the step of forming a groove in said epitaxial layer comprises the steps of

applying a first insulation material in a selected pattern over the epitaxial layer to define oxide-isolation and device regions, and

etching the exposed epitaxial layer to form a groove therein, and wherein the step of applying an impurity to selected regions of said groove to form the guard ring comprises the steps of

applying a self-aligned base insulation material over those portions of said groove which abut the region between the base of a vertical bipolar transistor to be formed and the emitter of a lateral bipolar transistor to be formed, and

applying said impurity to the portions of said grooves not covered by said self-aligned base insulation material to thereby form the guard ring.

4. A process as claimed in claim 3 wherein the step of applying an impurity is accomplished by means of thermal diffusion.

5. A process as claimed in claim 3 or 4 wherein the step of forming at least one semiconductor device comprises the step of

forming a merged injection-logic structure in said device region, said merged structure having a vertical bipolar transistor and a complementary lateral bipolar transistor, the base of said vertical bipolar transistor serving as the collector of said lateral bipolar transistor.

6. A process as claimed in claim 5 wherein the step of applying a self-aligned base insulation material includes applying a self-aligned base insulation material over those portions of the groove which abut the inverse emitter contact region to be formed for said vertical bipolar transistor.

7. A process as claimed in claim 6 wherein the step of forming a merged injection-logic structure includes the step of increasing the impurity concentration of the emitter region of said lateral bipolar transistor when the contact region for the base of said vertical bipolar transistor is formed.

8. A process as claimed in claim 7 wherein the step of increasing the impurity concentration of said emitter region of said lateral bipolar transistor comprises the step of heavily doping both the base contact region for the vertical bipolar transistor and the emitter contact region for the lateral bipolar transistor.

9. A process as claimed in claim 5 wherein said step of forming a merged injection-logic structure includes the step of forming a segmented base region for said vertical bipolar transistor, said segmented base region having heavily doped base regions and lightly doped base regions.

10. A process as claimed in claim 9 wherein said step of applying a self-aligned base insulation material includes applying a self-aligned base insulation material over those portions of said groove which lie between the base contact and inverse emitter contact regions for said vertical bipolar transistor.

11. A process as claimed in any one of claims 5 to 10 wherein the semiconductor substrate is of *p*-type conductivity, said buried layer region is of *n*-type conductivity, said epitaxial layer is of *n*-type conductivity, said impurity is of *p*-type conductivity so that said vertical bipolar transistor is NPN and said lateral bipolar transistor is PNP.

12. A process as claimed in any preceding claim wherein the step of forming an oxide of said semiconductor in said groove comprises the step of thermally treating the exposed groove to oxidize the exposed epitaxial layer.

13. A process of fabricating at least one oxide-isolated semiconductor device in a semiconductor substrate substantially as hereinbefore described with reference to the accompanying drawings.

14. An oxide-isolated semiconductor device in a semiconductor substrate

* C L M S *

fabricated by the process of any preceding claim.

15. An oxide-isolated semiconductor structure comprising:

an epitaxial layer overlaying a semiconductor substrate, said epitaxial layer being of a conductivity type opposite to the conductivity type of said substrate;

an oxide-isolation region composed of an oxide of said semiconductor and formed in a groove within said epitaxial layer, said oxide isolation region laterally surrounding and defining a device region, said device region having a guard ring formed at selected portions of the interface between said oxide-isolation region and said device region and containing an impurity of a conductivity type opposite to the conductivity type of the epitaxial layer; and

at least one semiconductor device formed in the device region.

16. A semiconductor structure as claimed in claim 15 wherein said at least one semiconductor device comprises a merged injection-logic structure having a vertical bipolar transistor and a complementary lateral bipolar transistor, the base of the vertical bipolar transistor serving as the collector of the lateral bipolar transistor.

17. A semiconductor structure as claimed in claim 16 wherein said vertical bipolar transistor is an NPN whose collector is formed in said buried layer, whose base is formed in the surface of said epitaxial layer and whose emitter is formed in said base region and wherein said complementary lateral bipolar transistor is a PNP whose emitter is formed in the surface of said epitaxial layer in spaced-apart lateral relation to said vertical bipolar transistor, whose base is the portion of said epitaxial layer between said emitter and said lateral PNP vertical bipolar transistor and whose collector is common with said base region of said vertical bipolar transistor.

18. A semiconductor structure as claimed in claim 16 or 17 wherein said guard ring is present everywhere along said interface except adjacent the base region of said lateral bipolar transistor.

19. A semiconductor structure as claimed in claim 16 or 17 wherein said guard ring is present everywhere along said interface except adjacent the base region of said lateral bipolar transistor and adjacent the emitter contact of said vertical bipolar transistor.

20. A semiconductor structure as claimed in claim 16 wherein said vertical bipolar transistor is fabricated with multiple inverse emitters and with a segmented base having segments of low and high impurity concentrations.

21. A semiconductor structure as claimed in claim 20 wherein said guard ring is present along said interface everywhere except adjacent the base region of said lateral bipolar transistor and between the base contact and emitter contact for said vertical bipolar transistor.

22. A semiconductor structure as claimed in any one of claims 16 to 21 wherein the emitter of said lateral bipolar transistor and the base contact region of said vertical bipolar transistor are heavily doped to minimize recombination current.

23. A semiconductor structure as claimed in claim 15 or 16 wherein said at least one semiconductor device comprises a vertical NPN.

24. A semiconductor structure as claimed in claim 15 or 16 wherein said at least one semiconductor device comprises a lateral PNP.

25. A semiconductor structure as claimed in any one of claims 15 to 25 including a buried layer region formed in the surface of the semiconductor substrate.

26. A semiconductor structure as claimed in any one of claims 15 to 25 wherein said at least one semiconductor device comprises a buried layer resistor.

27. A semiconductor structure as claimed in any one of claims 15 to 26 wherein said at least one semiconductor device comprises a field-effect transistor.

28. An oxide-isolated semiconductor structure substantially as hereinbefore described with reference to the accompanying drawings.

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