CLAIMS

WHAT IS CLAIMED IS:

1. A pattern sheet, comprising a first mask layer, a second mask layer, a dielectric layer, and a substrate layer, which are sequentially stacked from top to bottom, wherein the first mask layer is a photoresist layer;

wherein the first mask layer includes a first hole penetrating the first mask layer along a thickness direction of the first mask layer and satisfies:

$d1 \times S5 > d2$, and $d2 \geqslant (d1 - d4/S3) \times S2/S1 + d4/S4$; or

$d1 \times S5 = d2$, and $d2 > (d1 - d4/S3) \times S2/S1 + d4/S4$;

wherein, d1 denotes a thickness of the first mask layer, d2 denotes a thickness of the second mask layer, d4 denotes a thickness of the dielectric layer, S1 denotes an etching selectivity ratio of the substrate and the first mask layer, S2 denotes an etching selectivity ratio of the substrate and the second mask layer, S3 denotes an etching selectivity ratio of the dielectric layer and the first mask layer, S4 denotes an etching selectivity ratio of the dielectric layer and the second mask layer, and S5 denotes an etching selectivity ratio of the second mask layer and the first mask layer.

2. The pattern sheet according to claim 1, wherein the second mask layer includes a material containing silicon.

3. The pattern sheet according to claim 2, wherein the second mask layer is a silicon dioxide layer.

4. A pattern sheet, comprising a first mask layer, a second mask layer, a third mask layer, a dielectric layer, and a substrate sequentially arranged in stacks from top to bottom;

wherein the first mask layer is a photoresist layer and includes a first hole penetrating the first mask layer along a thickness direction of the first mask layer and satisfies:

$d1' \times S5' > d2'$, and $d2' \times S6' \geq d3'$, and $d3' \geq (d1' - d4'/S3') \times S2'/S1' + d4'/S4'$; or

$d1' \times S5' \geq d2'$, and $d2' \times S6' > d3'$, and $d3' \geq (d1' - d4'/S3') \times S2'/S1' + d4'/S4'$; or

$d1' \times S5' \geq d2'$, and $d2' \times S6' \geq d3'$, and $d3' > (d1' - d4'/S3') \times S2'/S1' + d4'/S4'$

wherein, d1' denotes a thickness of the first mask layer, d2' denotes a thickness of the second mask layer, d3' denotes a thickness of the third mask layer, d4' denotes a thickness of the dielectric layer, S1' denotes an etching selectivity ratio of the substrate and the first mask layer, S2' denotes an the etching selectivity ratio of the substrate and the third mask layer, S3' denotes an etching selection ratio of the dielectric layer and the first mask layer, S4' denotes an etching selectivity ratio of the dielectric layer and the third mask layer, S5' denotes an etching selectivity ratio of the second mask layer and the first mask layer, and S6' denotes an etching selectivity ratio of the third mask layer and the second mask layer.

5. The pattern sheet according to claim 4, wherein the second mask layer is a silicon dioxide layer.

6. The pattern sheet according to claim 4 or 5, wherein the third mask layer is an APFα-C layer.

7. The pattern sheet according to claim 4 or 5, wherein the thickness of the first mask layer ranges from 1 μm to 2 μm, the thickness of the second mask layer ranges from 400 nm to 700 nm, and the thickness of the third mask layer ranges from 6 μm to 7 μm.

8. A semiconductor intermediate product, which is formed from the pattern sheet according to any one of claims 1 to 3 by an etching process, wherein the semiconductor intermediate product includes a second mask layer, a dielectric layer, and a substrate sequentially arranged in stacks from top to bottom, wherein a thickness of the second mask layer of the semiconductor intermediate product is smaller than the thickness of the second mask layer of the pattern sheet; the second mask layer includes a second hole penetrating the second mask layer; the dielectric layer includes a fourth hole arranged corresponding to the second hole and penetrating the dielectric layer; and the substrate includes a fifth hole arranged corresponding to the fourth hole and penetrating the substrate.

9. A semiconductor intermediate product, which is formed from the pattern sheet according to any one of claims 4 to 7 by an etching process, wherein the semiconductor intermediate product includes a third mask layer, a dielectric layer, and a substrate sequentially arranged in stacks from top to bottom, wherein a thickness of the third mask layer of the semiconductor intermediate product is smaller than the thickness of the third mask layer of the pattern sheet; the third mask layer includes a third hole penetrating the third mask layer; the dielectric layer includes a fourth hole arranged corresponding to the third hole and penetrating the dielectric layer; and the substrate includes a fifth hole arranged corresponding to the fourth hole and penetrating the substrate.

10. A hole etching method, wherein the substrate and the dielectric layer arranged on the substrate are etched to form the corresponding holes by using the pattern sheet according to any one of claims 1 to 7, the hole etching method comprising:

etching a lower layer of a mask layer to form a through-hole penetrating a thickness of the lower layer of the mask layer by using an upper layer of any two neighboring layers of the mask layer as a mask; and

etching a dielectric layer to form a through-hole penetrating a thickness of the dielectric layer and forming a hole with a set depth in the substrate by using the remaining mask layer with at least one layer above the dielectric layer.