CLAIMS

1. A processing system, comprising:

a receiving device;

a bus having first, second and third channels; and

a sending device configured to address the receiving device on the first channel, and read a payload from the receiving device on the second channel, the sending device being further configured to select between the first and third channels to write a payload to the receiving device.

2. The processing system of claim 1 wherein the sending device is further configured to write the payload to a first address of the receiving device on the first channel and write a second payload to a second address of the receiving device on the third channel.

3. The processing system of claim 1 further comprising a second receiving device, and wherein the sending device is further configured to write the payload to the receiving device on the first channel and write a payload to the second receiving device on the third channel.

4. The processing system of claim 1 wherein the bus further comprises a fourth channel, the sending device being further configured to address the receiving device on the first channel for write operations and address the receiving device on the fourth channel for read operations, and wherein the sending device is further configured to select between the first, third and fourth channels to write the payload to the receiving device.

5. The processing system of claim 4 wherein the sending device is further configured to write the payload to a first address of the receiving device on one of the first, third and fourth channels and write a second payload to a second address of the receiving device on another one of the first, third and fourth channels.

6. The processing system of claim 4 wherein the sending device is further configured to write the payload to a first address of the receiving device on the first channel, write a second payload to a second address of the receiving device on the third channel, and write a third payload to a third address of the receiving device on the fourth channel.

7. The processing system of claim 4 further comprising a second receiving device, and wherein the sending device is further configured to write the payload to the receiving device on one of the first, third and fourth channels and write a second payload to the second receiving device on another one of the first, third and fourth channels.

8. The processing system of claim 4 further comprising second and third receiving devices, and wherein the sending device is further configured to write the payload to the receiving device on the first channel, write a second payload to the second receiving device on the third channel, and write a third payload to the third receiving device on the fourth channel.

9. The processing system of claim 1 wherein the sending device is further configured to provide a control signal to the receiving device indicating whether the first channel is currently being used to address the receiving device or write the payload to the receiving device.

10. The processing system of claim 1 wherein the sending device is further configured to provide a control signal to the receiving device while addressing the receiving device, the control signal indicating whether a payload for the address will be written to the receiving device on the first or third channel.

11. A processing system, comprising:

a receiving device;

a bus having first, second and third channels;

means for addressing the receiving device on the first channel;

means for reading a payload from the receiving device on the second channel; and

means for selecting between the first and third channels to write a payload to the receiving device.

12. A method of communicating between a sending device and one or more receiving devices over a bus, the bus comprising first, second and third channels, the method comprising:

addressing a receiving device on the first channel,

reading a payload from the receiving device on the second channel; and

selecting between the first and third channels to write a payload to the receiving device.

13. The method of claim 12 further comprising writing the payload to a first address of the receiving device on the first channel and writing a second payload to a second address of the receiving device on the third channel.

14. The method of claim 12 further comprising writing the payload to the receiving device on the first channel and writing a second payload to a second receiving device on the third channel.

15. The method of claim 12 wherein the bus further comprises a fourth channel, and wherein the receiving device is addressed on the first channel for a write operation, the method further comprising addressing the receiving device on the fourth channel for a read operation, wherein the selection of which channel to write the payload to the receiving device further comprises selecting between the first, third and fourth channels to write the payload to the receiving device.

16. The method of claim 15 further comprising writing the payload to a first address of the receiving device on one of the first, third and fourth channels and writing a second payload to a second address of the receiving device on another one of the first, third and fourth channels.

17. The method of claim 15 further comprising writing the payload to a first address of the receiving device on the first channels and writing a second payload to a

second address of the receiving device on the third channel and writing a third payload to a third address of the receiving device on the fourth channel.

18. The method of claim 15 further comprising writing the payload to the receiving device on one of the first, third and fourth channels and writing a second payload to a second receiving device on another one of the first, third and fourth channels.

19. The method of claim 15 further comprising writing the payload to the receiving device on the first channel and writing a second payload to a second receiving device on the third channel and writing a third payload to a third receiving device on the fourth channel.

20. The method of claim 12 further comprising providing a control signal to the receiving device indicating whether the first channel is currently being used to address the receiving device or write a payload to the receiving device.

21. The method of claim 12 further comprising providing a control signal to the receiving device while addressing the receiving device, the control signal indicating whether a payload for the address will be written to the receiving device on the first or third channel.

22. A bus mastering device, comprising:

a processor; and

a bus interface configured to interface the processor to a bus having first, second and third channels, the bus interface being further configured to address a slave on the first channel, receive a payload from the slave on the second channel, and select between the first and third channels to send a payload to the slave.

23. The bus mastering device of claim 22 wherein the bus interface device is further configured to send the payload to a first address of the slave on the first channel and send a second payload to a second address of the slave on the third channel.

24. The bus mastering device of claim 22 wherein the bus interface is further configured to send the payload to the slave on the first channel and send a payload to a second slave on the third channel.

25. The bus mastering device of claim 22 wherein the bus further comprises a fourth channel, and wherein the bus interface is further configured to address the slave on the first channel for write operations and address the slave on the fourth channel for read operations, and wherein the sending device is further configured to select between the first, third and fourth channels to write the payload to the slave.

26. The bus mastering device of claim 25 wherein the bus interface is further configured to send the payload to a first address of the slave on one of the first, third and fourth channels and send a second payload to a second address of the slave on another one of the first, third and fourth channels.

27. The bus mastering device of claim 25 wherein the bus interface is further configured to send the payload to a first address of the slave on the first channel, send a second payload to a second address of the slave on the third channel, and send a third payload to a third address of the slave on the fourth channel.

28. The bus mastering device of claim 25 wherein the bus interface is further configured to send the payload to the slave on one of the first, third and fourth channels and send a second payload to a second slave on another one of the first, third and fourth channels.

29. The bus mastering device of claim 25 further comprising second and third slaves, and wherein the bus interface is further configured to send the payload to the slave on the first channel, send a second payload to a second slave on the third channel, and send a third payload to a third slave on the fourth channel.

30. The bus mastering device of claim 22 wherein the bus interface is further configured to provide a control signal to the slave indicating whether the first channel is currently being used to address the slave or send the payload to the slave.

31. The bus mastering device of claim 22 wherein the bus interface is further configured to provide a control signal to the slave while addressing the slave, the control signal indicating whether a payload for the address will be sent to the slave on the first or third channel.

32. A bus mastering device, comprising:

a processor; and

means for interfacing the processor to a bus having first, second and third channels, the means for interfacing the processor to the bus comprising means for addressing a slave on the first channel, means for receiving a payload from the slave on the second channel, and means for selecting between the first and third channels to send a payload to the slave.

33. A slave device, comprising:

memory; and

a bus interface configured to interface the memory to a bus having first, second and third channels, the bus interface being configured to receive a memory address and a first payload from a bus mastering device on the first channel, receive a second payload from the bus mastering device on the second channel, and send a payload to the bus mastering device on the third channel.

34. The slave device of claim 33 wherein the bus interface is further configured to receive the first and second payloads.

35. The slave device of claim 33 wherein the bus further comprises a fourth channel, wherein the memory is further configured to be addressed through the bus interface by the sending the device on the first channel for write operations and on the fourth channel for read operation, the bus interface being further configured to receive a third payload from the bus mastering device on the fourth channel.

36. The slave device of claim 35 wherein the bus interface is further configured to receive the first, second and third payloads.

37. The slave device of claim 34 wherein the bus interface is further configured to receive a control signal from the bus mastering device indicating whether the first channel is currently being used to address the memory or send the first payload.

38. The slave device of claim 22 wherein the bus interface is further configured to receive a control signal from the bus mastering device while the memory is being addressed, the control signal indicating whether a payload for the address will be received on the first or third channel.

39. A slave device, comprising:

memory; and

means for interfacing the memory to a bus having first, second and third channels, the means for interfacing the memory to the bus comprising means for receiving a memory address and a first payload from a bus mastering device on the first channel, means for receiving a second payload from the bus mastering device on the second channel, and means for sending a payload to the bus mastering device on the third channel.

CLAIMS

1. A processing system, comprising:
a receiving device;
a bus having first, second and third channels; and
a sending device configured to:
address the receiving device on the first channel,
read from the receiving device on the second channel,
write to the receiving device on the third channel, and
select between:
a first bus transmission mode wherein payload write data is to be written to the receiving device on the third channel; and
a second bus transmission mode wherein first payload write data is to be written to the receiving device on the third channel during a first clock cycle and second payload write data is to be concurrently written to the receiving device on the first channel during the first clock cycle, wherein the first payload write data is associated with a first write operation and the second payload write data is associated with a second write operation, and wherein the first and second payload write data are distinct from address and control information.

2. The processing system of claim **1** wherein, in the second bus transmission mode, the sending device is further configured to write the second payload write data to a first address of the receiving device on the first channel and write the first payload write data to a second address of the receiving device on the third channel.

3. The processing system of claim **1** further comprising a second receiving device, and wherein, in the second bus transmission mode, the sending device is further configured to write the second payload write data to the receiving device on the first channel and write the first payload write data to the second receiving device on the third channel.

4. The processing system of claim **1** wherein the bus further comprises a fourth channel, the sending device being further configured to address the receiving device on the first channel for write operations and address the receiving device on the fourth channel for read operations, and wherein, in the first bus transmission mode, the sending device is further configured to select between the first, third and fourth channels to write the first payload write data to the receiving device.

5. The processing system of claim **4** wherein the sending device is further configured, in the second bus transmission mode, to write the first payload write data to a first address of the receiving device on one of the first, third and fourth channels and write the second payload write data to a second address of the receiving device on another one of the first, third and fourth channels.

6. The processing system of claim **4** wherein the sending device is further configured, in the second bus transmission mode, to write the second payload write data to a first address of the receiving device on the first channel, write the first payload write data to a second address of the receiving device on the third channel, and write a third payload write data to a third address of the receiving device on the fourth channel.

7. The processing system of claim **4** further comprising a second receiving device, and wherein the sending device is further configured, in the second bus transmission mode, to write the first payload write data to the receiving device on one of the first, third and fourth channels and write the second payload write data to the second receiving device on another one of the first, third and fourth channels.

8. The processing system of claim **4** further comprising second and third receiving devices, and wherein the sending device is further configured, in the second bus transmission mode, to write the second payload write data to the receiving device on the first channel, write the first payload write data to the second receiving device on the third channel, and write a third payload write data to the third receiving device on the fourth channel.

9. The processing system of claim **1** wherein the sending device is further configured to provide a control signal to the receiving device indicating whether the first channel is currently being used to address the receiving device or write the second payload write data to the receiving device.

10. The processing system of claim **1** wherein the sending device is further configured to provide a control signal to the receiving device while addressing the receiving device, the control signal indicating whether a payload for the address will be written to the receiving device on the first or third channel.

11. The processing system of claim **1**, wherein the sending device writes the first payload write data in accordance with the selected bus transmission mode.

12. The processing system of claim **1**, wherein writing of the first payload write data and writing of the second payload write data are completed during the first clock cycle.

13. A processing system, comprising:

a receiving device;

a bus having first, second and third channels;

means for addressing the receiving device on the first channel;

means for reading from the receiving device on the second channel;

means for writing to the receiving device on the third channel; and

means for selecting between:

a first bus transmission mode wherein payload write data is to be written to the receiving device on the first channel or the third channel; and

a second bus transmission mode wherein second payload write data is to be written to the receiving device on the first channel during a first clock cycle and first payload write data is to be concurrently written to the receiving device on the third channel during the first clock cycle, wherein the first payload write data is associated with a first write operation and the second payload write data is associated with a second write operation, and wherein the first and second payload write data are distinct from address and control information.

14. A method of communicating between a sending device and one or more receiving devices over a bus, the bus comprising first, second and third channels, the method comprising:

addressing a receiving device on the first channel;

reading from the receiving device on the second channel;

writing to the receiving device on the third channel; and selecting between:

a first bus transmission mode wherein payload write data is to be written to the receiving device on the first channel or the third channel; and

a second bus transmission mode wherein second payload write data is to be written to the receiving device on the first channel during a first clock cycle and first payload write data is to be concurrently written to the receiving device on the third channel during the first clock cycle, wherein the first payload write data is associated with a first write operation and the second payload write data is associated with a second write operation, and wherein the first and second payload write data are distinct from address and control information.

15. The method of claim **14** further comprising, in the second bus transmission mode, writing the second payload write data to a first address of the receiving device on the first channel and writing the first payload write data to a second address of the receiving device on the third channel.

16. The method of claim **14** further comprising, in the second bus transmission mode, writing the second payload write data to the receiving device on the first channel and writing the first payload write data to a second receiving device on the third channel.

17. The method of claim **14** wherein the bus further comprises a fourth channel, and wherein the receiving device is addressed on the first channel for a write operation, the method further comprising addressing the receiving device on the fourth channel for a read operation, wherein, in the first bus transmission mode, the method further comprises selecting between the first, third and fourth channels to write the first payload write data to the receiving device.

18. The method of claim **17** further comprising, in the second bus transmission mode writing the first payload write data to a first address of the receiving device on one of the first, third and fourth channels and writing the second payload write data to a second address of the receiving device on another one of the first, third and fourth channels.

19. The method of claim **17** further comprising, in the second bus transmission mode, writing the second payload write data to a first address of the receiving device on the first channel, writing the first payload write data to a second address of the receiving device on the third channel and writing a third payload write data to a third address of the receiving device on the fourth channel.

20. The method of claim **17** further comprising, in the second bus transmission mode, writing the first payload write data to the receiving device on one of the first, third and fourth channels and writing the second payload write data to a second receiving device on another one of the first, third and fourth channels.

21. The method of claim **17** further comprising, in the second bus transmission mode, writing the second payload write data to the receiving device on the first channel, writing the first payload write data to a second receiving device on the third channel, and writing a third payload write data to a third receiving device on the fourth channel.

22. The method of claim **14** further comprising providing a control signal to the receiving device indicating whether the first channel is currently being used to address the receiving device or write the second payload write data to the receiving device.

23. The method of claim **14** further comprising providing a control signal to the receiving device while addressing the receiving device, the control signal indicating whether a payload for the address will be written to the receiving device on the first or third channel.

24. A bus mastering device, comprising:
a processor; and
a bus interface configured to:
interface the processor to a bus having first, second and third channels,
address a slave on the first channel,
receive from the slave on the second channel,
write to the slave on the third channel, and
select between
a first bus transmission mode wherein payload write data is to be sent to the slave on the first channel or the third channel; and
a second bus transmission mode wherein second payload write data is to be sent to the slave on the first channel during a first clock cycle and first payload write data is to be concurrently sent to the slave on the third channel during the first clock cycle, wherein the first payload write data is associated with a first write operation and the second payload write data is associated with a second write operation, and wherein the first and second payload write data are distinct from address and control information.

25. The bus mastering device of claim **24** wherein the bus interface device is further configured, in the second bus transmission mode, to send the second payload write data to a first address of the slave on the first channel and send the first payload write data to a second address of the slave on the third channel.

26. The bus mastering device of claim **24** wherein the bus interface is further configured, in the second bus transmission mode, to send the second payload write data to the slave on

the first channel and send the first payload write data to a second slave on the third channel.

27. The bus mastering device of claim **24** wherein the bus further comprises a fourth channel, and wherein the bus interface is further configured to address the slave on the first channel for write operations and address the slave on the fourth channel for read operations, and wherein, in the first bus transmission mode, the bus interface is further configured to select between the first, third and fourth channels to send the first payload write data to the slave.

28. The bus mastering device of claim **27** wherein the bus interface is further configured, in the second bus transmission mode, to send the first payload write data to a first address of the slave on one of the first, third and fourth channels and send the second payload write data to a second address of the slave on another one of the first, third and fourth channels.

29. The bus mastering device of claim **27** wherein the bus interface is further configured, in the second bus transmission mode, to send the second payload write data to a first address of the slave on the first channel, send the first payload write data to a second address of the slave on the third channel, and send a third payload write data to a third address of the slave on the fourth channel.

30. The bus mastering device of claim **27** wherein the bus interface is further configured, in the second bus transmission mode, to send the first payload write data to the slave on one of the first, third and fourth channels and send the second payload write data to a second slave on another one of the first, third and fourth channels.

31. The bus mastering device of claim **27** further comprising second and third slaves, and wherein the bus interface is further configured, in the second bus transmission mode, to

send the second payload write data to the slave on the first channel, send the first payload write data to a second slave on the third channel, and send a third payload write data to a third slave on the fourth channel.

32. The bus mastering device of claim **24** wherein the bus interface is further configured to provide a control signal to the slave indicating whether the first channel is currently being used to address the slave or send the second payload write data to the slave.

33. The bus mastering device of claim **24** wherein the bus interface is further configured to provide a control signal to the slave while addressing the slave, the control signal indicating whether a payload for the address will be sent to the slave on the first or third channel.

34. The slave device of claim **24** wherein the bus interface is further configured to receive a control signal from the bus mastering device while the memory is being addressed, the control signal indicating whether a payload for the address will be received on the first or third channel.

35. A bus mastering device, comprising:

a processor; and

means for interfacing the processor to a bus having first, second and third channels, the means for interfacing the processor to the bus comprising:

means for addressing a slave on the first channel,

means for receiving from the slave on the second channel,

means for writing to the slave on the third channel, and

means for selecting between:

a first bus transmission mode wherein payload write data is to be sent to the slave on the first channel or the third channel; and

a second bus transmission mode wherein second payload write data is to be sent to the slave on the first channel during a first clock cycle and first payload

write data is to be concurrently sent to the slave on the third channel during the first clock cycle, wherein the first payload write data is associated with a first write operation and the second payload write data is associated with a second write operation, and wherein the first and second payload write data are distinct from address and control information.

36. A slave device, comprising:

memory; and

a bus interface configured to:

interface the memory to a bus having first, second and third channels,

receive a memory address on the first channel,

in a first bus transmission mode, receive payload data from a bus mastering device on the first channel or the second channel,

in a second bus transmission mode, receive second payload write data from the bus mastering device on the first channel during a first clock cycle and concurrently receive first payload write data from the bus mastering device on the second channel during the first clock cycle, wherein the first payload write data is associated with a first write operation and the second payload write data is associated with a second write operation, and wherein the first and second payload write data are distinct from address and control information, and

send a payload to the bus mastering device on the third channel.

37. The slave device of claim **36** wherein the bus further comprises a fourth channel, wherein the memory is further configured to be addressed through the bus interface by the bus mastering device on the first channel for write operations and on the fourth channel for read operation, the bus interface being further configured to receive, in the second bus transmission mode, a third payload write data from the bus mastering device on the fourth channel.

38. The slave device of claim **36** wherein the bus interface is further configured to receive a control signal from the bus mastering device indicating whether the first channel is currently being used to address the memory or receive the second payload write data.

39. A slave device, comprising:

memory; and

means for interfacing the memory to a bus having first, second and third channels, the means for interfacing the memory to the bus comprising:

means for receiving a memory address on the first channel,

means for receiving, in a first bus transmission mode, payload data from a bus mastering device on the first channel or the second channel,

means for receiving, in a second bus transmission mode, second payload write data from the bus mastering device on the first channel during a first clock cycle and concurrently receiving first payload write data from the bus mastering device on the second channel during the first clock cycle, wherein the first payload write data is associated with a first write operation and the second payload write data is associated with a second write operation, and wherein the first and second payload write data are distinct from address and control information, and

means for sending a payload to the bus mastering device on the third channel.