C L A I M S

1. A storage system comprising:

a first memory chip unit including a first pad electrode unit including a first portion and a second portion electrically coupled to each other, and a first memory cell array electrically coupled to the first pad electrode unit; and

a prober that is able to hold the first memory chip unit and executes reading and writing on the first memory cell array of the held first memory chip unit, wherein

the prober includes

a probe card including a first probe electrode that is able to be in contact with the first pad electrode unit of the held first memory chip unit, and a first memory controller that is able to be electrically coupled to the first probe electrode and execute reading and writing on the first memory cell array via the first probe electrode, and

a movement mechanism that moves the probe card or the held first memory chip unit to bring the first pad electrode unit of the held first memory chip unit into contact with the first probe electrode, ~~and~~

the movement mechanism executes a first operation that brings the first probe electrode into contact with the first portion of the first pad electrode unit and does not bring the first probe electrode into contact with the second portion of

the first pad electrode unit, and a second operation that does not bring the first probe electrode into contact with the first portion of the first pad electrode unit and brings the first probe electrode into contact with the second portion of the first pad electrode unit, and

the movement mechanism is configured to

execute the first operation when a first condition is not satisfied, and

execute the second operation when the first condition is satisfied.

2. The storage system according to claim 1, further comprising:

a first wafer including the first memory chip unit, wherein

the prober is able to hold the first wafer, and holds the first memory chip unit by holding the first wafer, and

the movement mechanism moves the first memory chip unit by moving the first wafer.

~~3. The storage system according to claim 1, wherein~~

~~the movement mechanism is configured to~~

~~execute the first operation when a first condition is not satisfied, and~~

~~execute the second operation when the first condition is satisfied.~~

~~4~~3. The storage system according to claim ~~3~~1, wherein the first condition includes that the number of times of contact between the first probe electrode and the first portion of the first pad electrode unit is equal to or larger than a first threshold.

~~5~~4. The storage system according to claim ~~3~~1, wherein the first condition includes that the first memory controller has failed in error correction processing of data from the first memory chip unit.

~~6~~5. The storage system according to claim ~~3~~1, wherein the first condition includes that the first memory chip unit has failed in error correction processing of data from the first memory controller.

~~7~~6. The storage system according to claim 1, wherein the first memory chip unit includes a latch circuit that is commonly coupled to the first portion and the second portion of the first pad electrode unit.

~~8~~7. The storage system according to claim ~~4~~3, further comprising:

a first wafer including the first memory chip unit; and

a second wafer, wherein

the prober is able to hold the first wafer, and holds the first memory chip unit by holding the first wafer,

the movement mechanism moves the first memory chip unit by moving the first wafer, and

the movement mechanism is further able to execute a third operation that brings the first probe electrode into contact with the second wafer.

~~9~~8. The storage system according to claim ~~8~~7, wherein

the movement mechanism is configured to execute the first operation or the second operation after executing the third operation, when a second condition is satisfied.

~~10~~9. The storage system according to claim ~~9~~8, wherein

the second condition includes that the number of times of contact between the first probe electrode and the first wafer is equal to or larger than a second threshold larger than the first threshold.

~~11~~10. The storage system according to claim 2, wherein

the first wafer further includes a second memory chip unit including a second pad electrode unit including a first portion and a second portion electrically coupled to each other, and a second memory cell array electrically coupled to the second pad electrode unit,

the probe card further includes a second probe electrode electrically coupled to the first memory controller,

the first operation further includes bringing the second probe electrode into contact with the first portion of the second pad electrode unit, and

the second operation further includes bringing the second probe electrode into contact with the second portion of the second pad electrode unit.

~~12~~11. The storage system according to claim 2, wherein

the first wafer further includes a third memory chip unit including a third pad electrode unit including a first portion and a second portion electrically coupled to each other, and a third memory cell array electrically coupled to the third pad electrode unit,

the probe card further includes a third probe electrode and a second memory controller electrically coupled to the third probe electrode,

the first operation further includes bringing the third probe electrode into contact with the first portion of the third pad electrode unit, and

the second operation further includes bringing the third probe electrode into contact with the second portion of the third pad electrode unit.

~~13~~12. The storage system according to claim 2, wherein

the first pad electrode unit has a convex shape from the first wafer toward the probe card in a state where the first wafer is placed in the prober, and

a portion of the first probe electrode facing the first wafer placed in the prober has a flat plate shape.

~~14. A memory chip unit, comprising:~~

~~a memory structure including a plurality of first conductor layers stacked in a first direction above a substrate, a first semiconductor layer extending in the first direction in the plurality of first conductor layers, and a first charge storage layer provided between the plurality of first conductor layers and the first semiconductor layer;~~

~~a first interconnect layer and a second interconnect layer provided above the memory structure so as to be electrically insulated from each other;~~

~~a second conductor layer provided on a top surface of a first portion of the first interconnect layer;~~

~~a third conductor layer provided on a top surface of a second portion of the first interconnect layer;~~

~~a fourth conductor layer provided on a top surface of the first portion of the second interconnect layer; and~~

~~a fifth conductor layer provided on a top surface of a second portion of the second interconnect layer, wherein~~

~~the second conductor layer, the third conductor layer, the fourth conductor layer, and the fifth conductor layer include aluminum (Al), and~~

~~a relative position of the fourth conductor layer with respect to the second conductor layer is matched with a relative position of the fifth conductor layer with respect to the third conductor layer in a plane parallel to the substrate.~~

~~15. The memory chip unit according to claim 14, wherein~~

~~a direction in which the second conductor layer and the third conductor layer are arranged is parallel to a direction in which the fourth conductor layer and the fifth conductor layer are arranged, and~~

~~a direction in which the second conductor layer and the fourth conductor layer are arranged is parallel to a direction in which the third conductor layer and the fifth conductor layer are arranged.~~

~~16. The memory chip unit according to claim 14, further comprising:~~

~~a sixth conductor layer provided on a top surface of the second conductor layer; and~~

~~a seventh conductor layer provided on a top surface of the third conductor layer, wherein~~

~~the sixth conductor layer and the seventh conductor layer include a metal different from a metal of the second conductor~~

~~layer and the third conductor layer.~~

~~17. The memory chip unit according to claim 16, wherein~~

~~the sixth conductor layer and the seventh conductor layer include at least one metal selected from nickel (Ni), gold (Au), cobalt (Co), palladium (Pd), copper (Cu), and silver (Ag).~~

~~18. The memory chip unit according to claim 16, wherein~~

~~a top surface of the sixth conductor layer and a top surface of the seventh conductor layer are located above a top surface of an insulator layer between the sixth conductor layer and the seventh conductor layer.~~

~~19. The memory chip unit according to claim 14, further comprising~~

~~a dicing line provided between the second conductor layer and the third conductor layer.~~

~~20. A wafer comprising:~~

~~a memory structure including a plurality of first conductor layers stacked in a first direction above a substrate, a first semiconductor layer extending in the first direction in the plurality of first conductor layers, and a first charge storage layer provided between the plurality of first conductor layers and the first semiconductor layer;~~

~~a second conductor layer provided above the memory~~

~~structure;~~

~~a third conductor layer provided above the second conductor layer;~~

~~a fourth conductor layer electrically coupling the second conductor layer and the third conductor layer; and~~

~~an insulator layer provided between the second conductor layer and the third conductor layer and including polyimide, wherein~~

~~in plan view,~~

~~the fourth conductor layer crosses a dicing line, and~~

~~the second conductor layer and the third conductor layer sandwich the dicing line.~~

~~21. The wafer according to claim 20, wherein~~

~~the second conductor layer includes aluminum (Al), and~~

~~the fourth conductor layer includes copper (Cu).~~

~~22. The wafer according to claim 21, further comprising:~~

~~a fifth conductor layer adjacent to the second conductor layer in a first plane parallel to the substrate; and~~

~~a sixth conductor layer adjacent to the third conductor layer in a second plane parallel to the substrate, wherein~~

~~a distance between the third conductor layer and the sixth conductor layer is longer than a distance between the second conductor layer and the fifth conductor layer.~~

~~23. The wafer according to claim 22, further comprising:~~

~~a seventh conductor layer electrically coupled to the sixth conductor layer in the first plane, wherein~~

~~a distance between the third conductor layer and the sixth conductor layer is shorter than a distance between the second conductor layer and the seventh conductor layer.~~

~~24. The wafer according to claim 22, wherein~~

~~a direction in which the second conductor layer and the fifth conductor layer are arranged is different from a direction in which the third conductor layer and the sixth conductor layer are arranged.~~

~~25. The wafer according to claim 21, wherein~~

~~an area of the third conductor layer is larger than an area of the second conductor layer in plan view.~~

~~26. The wafer according to claim 21, further comprising:~~

~~an eighth conductor layer electrically coupled to the third conductor layer via the second conductor layer and including aluminum (Al).~~

~~27. The wafer according to claim 21, further comprising:~~

~~a ninth conductor layer electrically coupled to the third conductor layer without going through the second conductor layer and including aluminum (Al).~~

~~28. The wafer according to claim 21, further comprising:~~

~~a tenth conductor layer electrically coupled to the third conductor layer without going through the second conductor layer and the fourth conductor layer and including aluminum (Al).~~

~~29. The wafer according to claim 21, wherein~~

~~the third conductor layer includes gold (Au) or nickel (Ni).~~