**DRAWINGS**

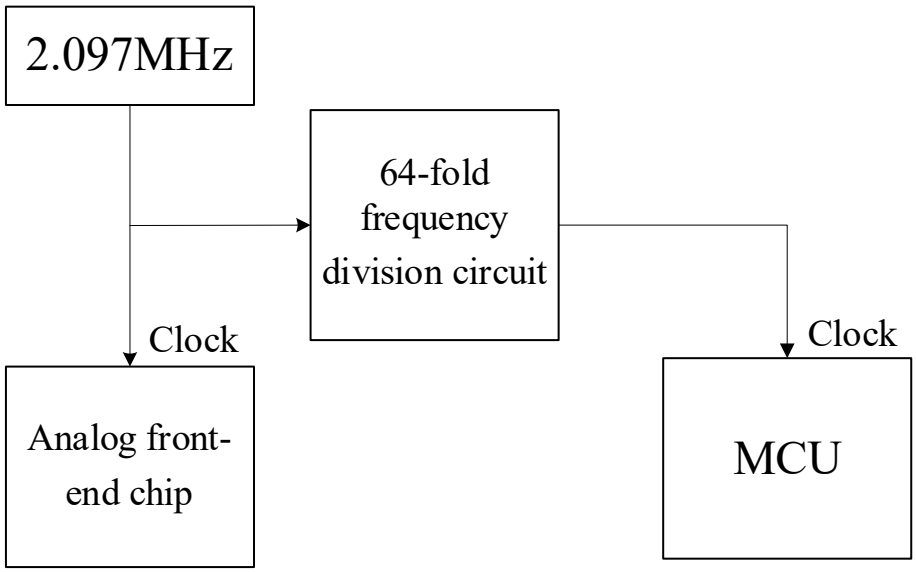


FIG. 1

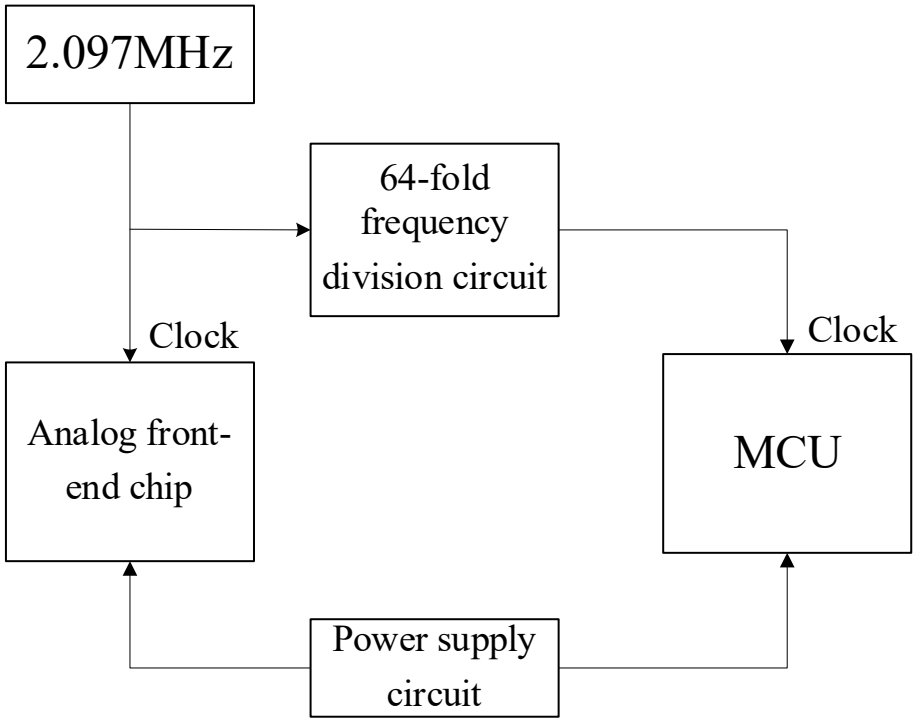
2.097MHz
64-fold frequency division circuit
Clock
Clock
Analog front-end chip
MCU
Power supply circuit

FIG. 2

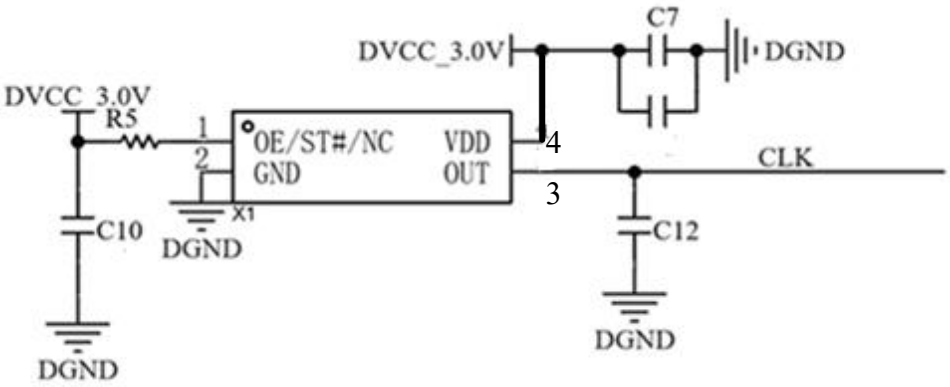
C7
DVCC_3.0V
DGND
DVCC_3.0V
R5
1
2
OE/ST#/NC
GND
VDD
OUT
4
3
CLK
X1
C10
DGND
C12
DGND
DGND

FIG. 3

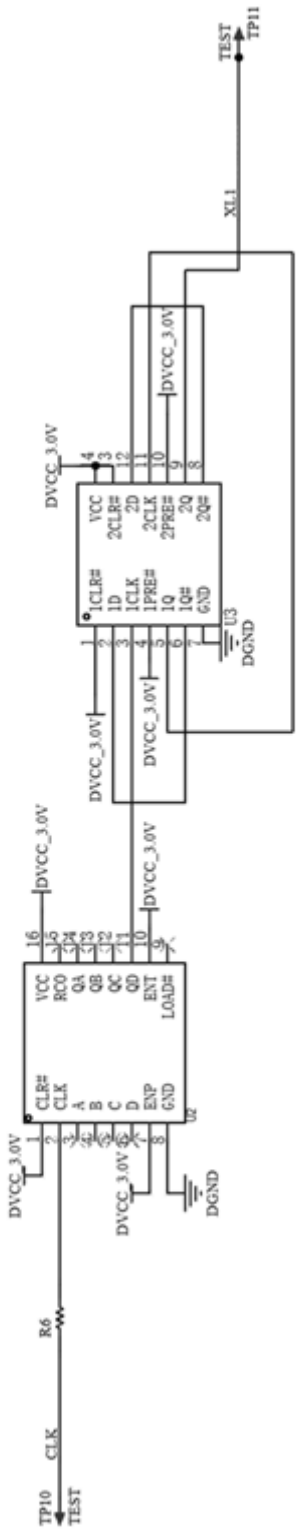


FIG. 4

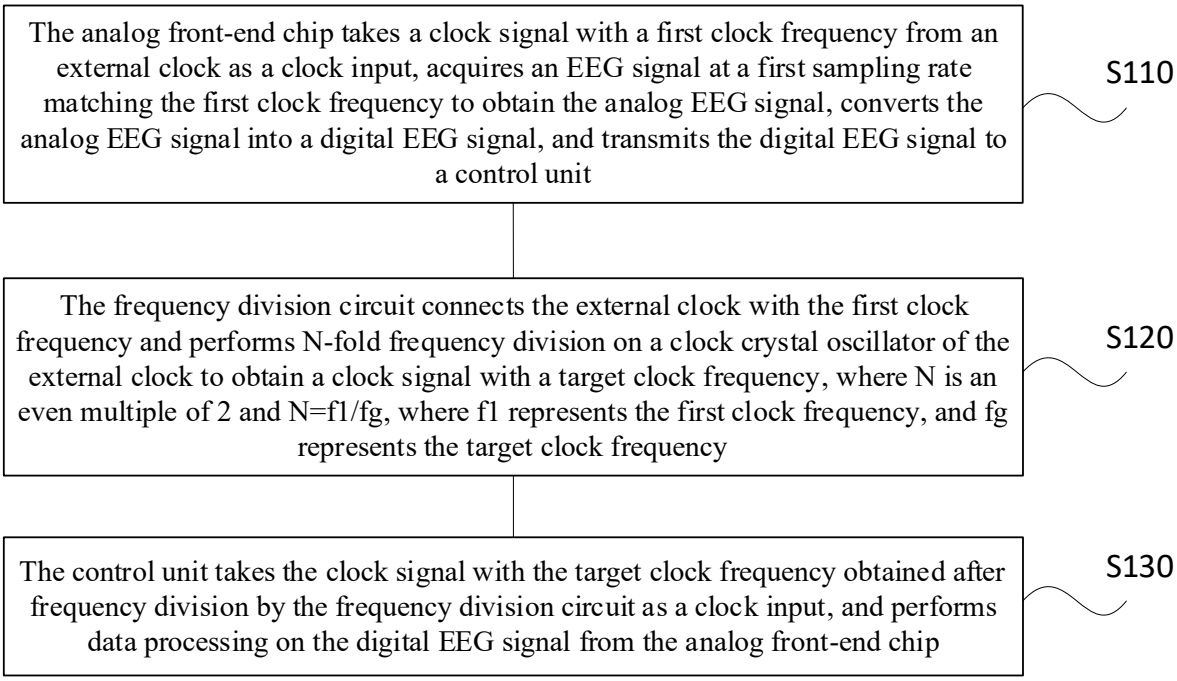
The analog front-end chip takes a clock signal with a first clock frequency from an external clock as a clock input, acquires an EEG signal at a first sampling rate matching the first clock frequency to obtain the analog EEG signal, converts the analog EEG signal into a digital EEG signal, and transmits the digital EEG signal to a control unit
S110
The frequency division circuit connects the external clock with the first clock frequency and performs N-fold frequency division on a clock crystal oscillator of the external clock to obtain a clock signal with a target clock frequency, where N is an even multiple of 2 and N=f1/fg, where f1 represents the first clock frequency, and fg represents the target clock frequency
S120
The control unit takes the clock signal with the target clock frequency obtained after frequency division by the frequency division circuit as a clock input, and performs data processing on the digital EEG signal from the analog front-end chip
S130

FIG. 5

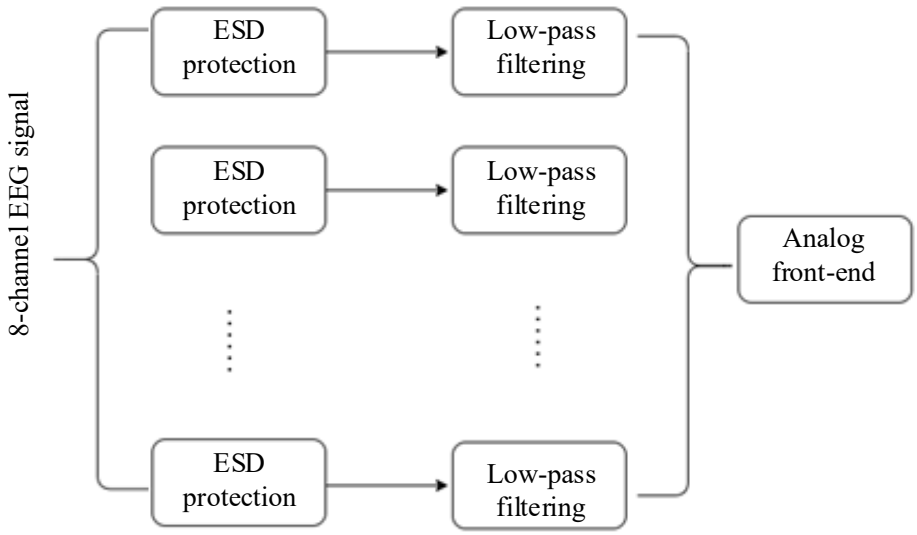
8-channel EEG signal
ESD protection
ESD protection
ESD protection
Low-pass filtering
Low-pass filtering
Low-pass filtering
Analog front-end

FIG. 6