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Description

Bus segment and bus access circuit for connecting an assembly of a programmable logic controller to a bus

The present invention relates to a bus segment according to the preamble of Claim 1 and a bus access circuit according to the preamble of Claim 2.

Bus segments and bus access circuits of this type are frequently used in programmable logic controllers having a modular structure. DE 36 03 750 A1 and DE 36 03 751 A1 are cited by way of example.

In the case of such a programmable logic controller having a modular structure, it may be necessary to insert or withdraw assemblies in the course of operation. However, the insertion or withdrawal may give rise to the occurrence of feedback to the bus which connects the assemblies to one another, which feedback disturbs the bus traffic. In order to avoid such disturbances, provision is customarily made in the prior art for providing leading and/or lagging contacts on the assembly, which is provided with an evaluation circuit and a variable resistor (typically a MOSFET), with the result that the assembly is electrically connected to the bus only after complete insertion and is already electrically isolated from the bus before complete withdrawal.

This procedure is disadvantageous insofar as at least the evaluation circuit must be supplied with power from the outset. However, even the connection of the evaluation circuit to the power supply can already bring about disturbances to the voltage supply of the bus, to be precise particularly when a fault occurs in the evaluation circuit or the voltage supply of the evaluation circuit. A short circuit of the two supply contacts, for example, of the assembly,

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by means of which the evaluation circuit is supplied with power, would ineluctably lead to a complete collapse of the power supply of the entire bus. The same consequence would emerge if other, external effects on the plug-in location for the assembly caused the supply contacts of the plug-in location to be short-circuited to one another. This case may occur particularly when an assembly which, although it can be inserted mechanically into the plug-in location, is not, however, electrically and functionally intended for this plug-in location is inserted into the plug-in location.

The object of the present invention consists in providing a bus segment and a bus access circuit by means of which negative feedback to the bus is avoided under all circumstances.

The object is achieved by means of the characterizing features of Claims 1 and 2, respectively.

The measure of Claim 3 ensures, in particular, that an inserted assembly is supplied with power only when all of its contacts, that is to say the signal contacts as well, are inserted into the plug-in location and the contacts thereof.

The measure according to Claim 4 yields particularly smooth and hence disturbance-free coupling of the assembly to the bus.

The measures of Claim 5 ensure that the assembly is isolated from the bus again if it is operating defectively or is not intended for this plug-in location.

Further advantages and details emerge from the following description of an exemplary embodiment. In the figures:

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FIG 1 shows a modular programmable logic controller,

FIG 2 shows the connection of an assembly of the programmable logic controller to the bus,

FIG 3 shows the voltage characteristic at the test contact,

FIG 4 shows the resistance characteristic of the variable resistor, and

FIG 5 shows the voltage characteristic at one of the supply contacts.

In accordance with FIG 1, a modular programmable logic controller comprises a power supply assembly 1, a central processing unit 2 and peripheral assemblies 3. The peripheral assemblies 3 may be, for example, digital or analog input and/or output assemblies. Furthermore, the peripheral assemblies may also be hybrid input/output assemblies or intelligent functional modules. Via the peripheral assemblies 3, the central processing unit 2 controls and monitors a technical process 6, for example a chemical installation or a hydraulic press.

The central processing unit 2 and the assemblies 3 are for this purpose connected to one another in terms of data technology via the control bus 4. The central processing unit 2 and the peripheral assemblies 3 are furthermore supplied with electrical energy via the supply lines 4', 4''. A common earth connection is established via the supply line 4''; the supply line 4' usually carries a potential of +5 volts. The control bus 4 and supply lines 4', 4'' together form the backplane bus 5 of the programmable logic controller.

In the example above, only two peripheral assemblies 3 are illustrated. Alternatively, of course, the programmable logic controller could have more assemblies, for example 5, 8, 10... Moreover, the control bus 4 may be designed as required. Thus, the control bus 4 may be, for example, a serial bus comprising just one clock line and one data line. However, the control bus 4 could also be a parallel bus comprising a multiplicity of address, data and

control lines. The concrete structure of the control bus 4 is of secondary importance within the context of the present invention. In every case, however, the lines of the control bus 4 form the signal lines of the present invention.

FIG 2 now shows the connection of the central processing unit 2 or of the peripheral assemblies 3 to a bus segment of the bus 5. As is immediately evident from FIG 2, the assembly 2, 3 connected to the bus 5 has an internal circuit 7. In the case of a peripheral assembly, the said circuit 7 is, moreover, connected to the technical process 6 via the process lines 8. In every case, however, the assembly is inserted into a plug-in location 10 via the plug-in connection 9 and connected to the bus 5 in this way.

As is furthermore immediately evident from FIG 2, the assembly 2, 3 is coupled in terms of data technology to the bus 5 directly via the assembly signal contacts 9-1 to 9-n and the plug-in location signal contacts 10-1 to 10-n, which are connected via the signal spur lines 11-1 to 11-n to the signal lines 4-1 to 4-n of the control bus 4.

The power supply of the assembly 2, 3, on the other hand, takes place via the assembly supply contacts 9', 9'', which are inserted into the plug-in location supply contacts 10', 10''. The plug-in location supply contacts 10', 10'' are connected via the supply spur lines 11', 11'' to the supply lines 4', 4''. A MOSFET 12 is in this case arranged in the supply spur line 11'. The volume resistance of the MOSFET 12 is, as is known, variable and adjustable within wide limits. The MOSFET 12 therefore represents the variable resistor of the present invention.

The MOSFET 12 is controlled to have a high resistance or low resistance by the evaluation circuit 13, which is likewise connected to the supply lines 4', 4'', in

accordance with the signals which are fed to the evaluation circuit 13.

As is furthermore evident from FIG 2, the plug-in location 10 has a test contact 14, which is connected via the pull-up resistor 15 to the supply line 4'. The potential present at the test contact 14 is fed to the evaluation circuit 13 via the test contact line 16. Furthermore, the potential present at the supply contact 10' is additionally fed to the evaluation circuit 13 via the supply contact line 17.

The present invention is essentially based on the fact that the potential of the supply line 4' is present at the test contact 14, on account of the pull-up resistor 15, if the assembly 2, 3 has not been inserted into the plug-in location 10. If, on the other hand, the assembly 2, 3 has been inserted into the plug-in location 10, the test contact 14 is connected directly to the supply line 4'' via the plug-in location supply contact 10'', the assembly supply contact 9'' and the mating test contact 18 directly connected to the latter, with the result that in this case the other supply potential is present at the evaluation circuit 13.

As a result, the evaluation circuit 13 can evaluate the potential present at the test contact 14 and control the variable resistor 12 to have a low resistance or high resistance, depending on whether or not the assembly 2, 3 has been inserted into the plug-in location 10. Furthermore, by evaluating the potential present on the supply contact line 17, it is possible to establish whether the supply potential is collapsing on account of the insertion of the assembly 2, 3. In this case, the MOSFET 12 is then controlled to have a high resistance again, with the result that the assembly 2, 3 is isolated from the bus 5. As a result, the other assemblies connected to the bus 5 can continue to be operated.

The exact method of operation of the evaluation circuit 13 will now be explained below with reference to FIGS 3 to 5.

On the ordinate, the voltage U_p present at the test contact is plotted in FIG 3, the resistance R of the MOSFET 12 is plotted in FIG 4 and the voltage U of the supply contact 10' is plotted in FIG 5. The time t is plotted in each case on the abscissa.

As long as the potential U_p, which is fed to the evaluation circuit 13 via the test contact line 16, of the test contact 14 corresponds, in accordance with FIG 3, to the supply voltage U_0 of, for example, 5 volts, the MOSFET 12 is driven by the evaluation circuit 13 in such a way that it has a high resistance, as illustrated in FIG 4. When the potential momentarily drops to 0 volts at the instant t_1 and rises to 5 volts again at the instant t_2, the MOSFET 12 likewise continues to have a high resistance, since the MOSFET is controlled to have a low resistance only when the potential U_p present at the test contact 14 approximately corresponds to the (earth) potential of the supply line 4'' in an uninterrupted manner during a previously determined waiting time T_1.

Such a brief drop in the potential U_p present at the test contact 14 can happen, for example, due to so-called contact bounce when the assembly 2, 3 is inserted.

Although, in accordance with FIG 5, the potential U transmitted via the supply contact line 17 at this instant likewise collapses, this is irrelevant for the driving of the MOSFET 12 at this instant.

At a later instant t_3, the assembly 2, 3 is definitively inserted into the plug-in location 10. As a result, the running of the waiting time T_1 is initiated. After this waiting time T_1 has elapsed, the MOSFET 12 is, as illustrated in FIG 4, gradually controlled to have a low resistance. Accordingly, the resistance of the MOSFET 12 decreases from the instant t_4, and the voltage U present at the supply contact 10' rises.

At an instant t_5, the evaluation circuit 13 tests whether the potential U present at the supply contact 10' approximately corresponds to the supply potential U_0 of the supply line 4'. In the present case, it is tested whether the potential present at the supply contact 10' deviates by a maximum of 0.5 volts above or below the desired potential U_0 = 5 volts. If the measured potential U lies within this value range, the resistor 12 continues to have a low resistance. It acquires a high resistance again (at the instant t_6) only when the test potential U_p rises again to the supply potential U_0.

If, on the other hand, as illustrated by dashed lines in FIGS 4 and 5, the potential U present at the supply contact 10' lies outside the predetermined value range (in the present case, for example, outside the range of 4.5 to 5.5 volts) at the instant t_5, this is assessed as a defective connection of the assembly 2, 3 to the bus 5. In this case, the evaluation circuit 13 immediately controls the resistor 12 to have a high resistance again (see dashed line in FIG 4). A flag is in this case set in the evaluation circuit 13 and prevents renewed controlling of the MOSFET 12 to have a low resistance until the assembly 2, 3 is withdrawn again from the plug-in location 10. The flag is therefore reset only at the instant t_6.

The time interval between t_5 and t_4 is the so-called stabilization time T_2.

In accordance with the circuit illustrated in FIG 2, the plug-in location 10, the evaluation circuit 13, the MOSFET 12 and the pull-up resistor 15 as well as the corresponding lines are part of the backplane bus 5. More precisely, the evaluation circuit 13, the MOSFET 12 and the resistor 15 are assigned to the bus segment in which the plug-in location 10 is arranged. The backplane bus 5 then has a plurality of such circuits, namely one circuit per plug-in location 10.

As an alternative, the backplane bus 5 itself could also have a modular structure, with the result that it comprises individual bus segments which can be connected to one another. This is indicated in FIG 2 by virtue of the fact that plug-in connections 19 drawn with dashed lines are indicated.

It would equally be possible to arrange the evaluation circuit 13, the MOSFET 12 and the resistor 15 together with associated interconnections and the plug-in location 10 in a dedicated bus access circuit 20, which can be plugged onto the bus 5, with the result that the access circuit is arranged between the assembly 2, 3 and the bus 5. This is also illustrated diagrammatically in FIG 2. In this case, the bus access circuit 20 also has, in addition to the plug-in location 10 for the assembly 2, 3, a bus connection 21 with contacts 21', 21'', 21-1 to 21-n. The contacts 21' and 10' are then again connected to one another via the connection line 11'; the same applies analogously to the contacts 21'' and 10'' and the contacts 21-1 and 10-1 to 21-1 and 10-n.

However, the functionality of the circuit always remains the same, irrespective of the concrete structure.

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Patent Claims

1. Bus segment for connecting an assembly (2, 3) of a programmable logic controller to a bus (5),

- the bus segment having at least a first and a second supply line (4', 4'') and a signal line (4-1 to 4-n) as well as a plug-in location (10) for inserting the assembly (2, 3),
- the plug-in location (10) having at least a first and a second supply contact (10', 10'') and a signal contact (10-1 to 10-n),
- the lines (4', 4'', 4-1 to 4-n) of the bus segment being connected via corresponding spur lines (11', 11'', 11-1 to 11-n) to the corresponding contacts (10', 10'', 10-1 to 10-n) of the plug-in location (10),

characterized

- in that the plug-in location (10) additionally has at least one test contact (14), which is connected to the first supply line (4') via a pull-up resistor (15), can be connected to the second supply line (4'') via the assembly (2, 3) and is connected to an evaluation circuit (13), and
- in that the evaluation circuit (13) is connected to the supply lines (4', 4''), evaluates the potential (U_p) present at the test contact (14) and controls a variable resistor (12), which is arranged in the first supply spur line (11'), to have a high resistance if the potential (U_p) present at the test contact (14) approximately corresponds to the potential (U_0) of the first supply line (4').

2. Bus access circuit for connecting an assembly (2, 3) of a programmable logic controller to a bus (5),

- the bus access circuit (20) having at least one bus connection (21) to the bus (5) and at least one plug-in location (10) for inserting the assembly (2, 3),

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- the bus connection (21) and the plug-in location (10) each having at least a first and a second supply contact (10', 10'', 21', 21'') and a signal contact (10-1 to 10-n, 21-1 to 21-n),
- corresponding contacts (10' and 21', 10'' and 21'', 10-1 and 21-1 to 10-n and 21-n) of the bus connection (21) and the plug-in location (10) being connected to one another via corresponding connection lines (11', 11'', 11-1 to 11-n),

characterized

- in that the plug-in location (10) additionally has at least one test contact (14), which is connected to the first supply contact (21') of the bus connection (21) via a pull-up resistor (15), can be connected to the second supply contact (21'') of the bus connection (21) via the assembly (2, 3) and is connected to an evaluation circuit (13), and
- in that the evaluation circuit (13) is connected to the supply contacts (21', 21'') of the bus connection (21), evaluates the potential (U_p) present at the test contact (14) and controls a variable resistor (12), which is arranged in the first supply connection line (11'), to have a high resistance if the potential (U_p) present at the test contact (14) approximately corresponds to the potential (U_0) of the first supply contact (21') of the bus connection (21).

3. Bus segment according to Claim 1 and bus access circuit according to Claim 2, characterized in that the evaluation circuit (13) controls the variable resistor (12) to have a low resistance only when the potential (U_p) present at the test contact (14) approximately corresponds to the potential of the second supply line (4'') and, respectively, of the second supply contact (21'') of the bus connection (21) in an uninterrupted manner during a predetermined waiting time (T_1).

4. Bus segment and bus access circuit according to Claim 3, characterized in that the evaluation

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circuit (13) gradually controls the variable resistor (12) to have a low resistance.

5. Bus segment and bus access circuit according to Claim 3 or 4, characterized in that the evaluation circuit (13) is connected to the first supply contact (10') of the plug-in location (10), and in that the evaluation circuit (13) controls the variable resistor (12) to have a high resistance again if, after a predetermined stabilization time (T_2), the potential (U) of the first supply contact (10') of the plug-in location (10) lies outside a predetermined value range.



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