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"A Radio Receiving Reproducing System".

The present invention relates to a radio receiving reproducing system which is suitable for installation in a vehicle such as a road vehicle.

5 In a sound field extending in the passenger compartment of a road vehicle, the surrounding noises other than the sounds generated by a radio receiver change greatly in volume.

10 In order to obviate this disadvantage, there has already been proposed an automatic sound volume control system for detecting those surrounding noises in order to control the output volume of the radio receiver proportionally in accordance with the noise level. Such a system has been disclosed in Japanese Laid-Open Patent Publication No. 82955/1979.

15 We have found that, if the control of the volume output is carried out in accordance with the automatic

sound volume control system disclosed in the above referred to publication, then under the circumstances where the receiving condition is bad (e.g., in the case where the road vehicle is travelling in a tunnel), the output volume of the audio signals containing much unwanted interference and noise is augmented to provide a rather unpleasant effect for the listener, especially if he is listening to rather "delicate" music (e.g. a baroque concerto).

It is therefore an object of the present invention to provide a receiving reproducing system which can effect the automatic control of the sound volume without substantially affecting the quality of the reproduction.

According to the present invention there is provided a radio receiving reproducing system including:

- (a) an AM tuner for obtaining an AM detected output signal from an AM radio-frequency signal;
- (b) an FM front end for obtaining an FM intermediate frequency signal from an FM radio-frequency signal;
- (c) an FM intermediate-frequency signal processing circuit for obtaining an FM detected output signal from said FM intermediate-frequency signal;
- (d) an FM stereo demodulator for obtaining a left-channel demodulated output signal and a right-channel demodulated output signal from said FM detected output signal;
- (e) a first terminal which can be supplied by way of a selection means with a selected one of said AM detected output signal and said left-channel demodulated

output signal;

a second terminal which can be supplied by way of
said selection means with a selected one of said AM
detected output signal and said right-channel demodulated
5 output signal;

(g) a first voltage-controlled attenuator having
an input terminal, a control terminal and an output terminal,
the signal transmission from said input terminal to said
output terminal being controllable by a control voltage
10 applied to said control terminal and said input terminal
being connected to said first terminal;

(h) a second voltage-controlled attenuator having
an input terminal, a control terminal and an output
terminal, the signal transmission from said input terminal
15 to said output terminal being controllable by a control
voltage applied to said control terminal and said input
terminal being connected to said second terminal;

(i) a first power amplifier the input terminal of
which is connected with said output terminal of said first
20 voltage-controlled attenuator;

(j) a second power amplifier the input terminal
of which is connected with said output terminal of said
second voltage-controlled attenuator;

(k) a first speaker which is driver by the output
25 signal of said first power amplifier;

(l) a second speaker which is driven by the output
signal of the second power amplifier;

(m) noise detector means for detecting the

surrounding noise level of a sound field;

(n) received level detector means for detecting an AM level which is dependent upon said AM radio-frequency signal as well as an FM level which is dependent upon said
5 FM radio-frequency signal; and

(o) control means responsive to an output signal of said received level detector means and connected between the output terminal of said noise detector means and both of said control terminals of said first and second voltage
10 controlled attenuators, said control means for transmitting the detected output of said noise detector means to both of said control terminals of said first and said second voltage controlled attenuators in the case where the output signal of said received level detector means is higher than a
15 preset value so as to control said output signals of said first and second power amplifiers proportionally in accordance with said surrounding noise level of said sound field and said control means forcibly lowering the level of said output signals of said first and second power ampli-
20 fiers in the case where said output signal of said received level detector means is lower than said preset value, thereby disabling sound field effects on said power amplifier output signals.

The present invention will now be described
25 in greater detail by way of examples, with reference to the accompanying drawings, wherein:-

Figure 1 is a block diagram showing a radio receiving reproducing system;

Figures 2A and 2B are block diagrams showing a preferred form of a radio receiving reproducing system;

Figure 3 is a block diagram showing the internal circuit of the first semiconductor integrated circuit used in the embodiment shown in Figures 2A and 2B;

Figure 4 is a block diagram showing the internal circuit of the second semiconductor integrated circuit used in the embodiment shown in Figures 2A and 2B;

Figure 5 is a block diagram showing the internal

circuit of the third semiconductor integrated circuit used in the embodiment shown in Figures 2A and 2B;

Figure 6 is a block diagram showing the internal circuit of the fourth semiconductor integrated circuit used in the embodiment shown in Figures 2A and 2B; and

Figure 7 is a graph illustrating the relationship in the embodiment of Figures 2A and 2B between the surrounding noise level in a sound field and the output voltage of a noise detector.

Referring to the block diagram of Figure 1 which shows a radio receiving reproducing system for installation in a road vehicle, the radio frequency signal received by an antenna ANT is transmitted to the input of a radio-frequency circuit 1 which comprises a high-frequency tuning amplifier, a local oscillator, a mixer and an intermediate-frequency amplifier. A detector 2, for detecting the intermediate-frequency amplified output, has its output amplified by a low-frequency power amplifier 4 before being transmitted to a speaker 5.

In order to control the output sound volume applied to the speaker 5 proportionally in accordance with the surrounding noise level of the sound field, the audio signal produced by the detector 2 is applied to the low-frequency power amplifier 4 through a variable gain

circuit 3. The variable gain circuit 3 is controlled by the signal according to the surrounding noise level of the sound field.

5 The signal level which is dependent upon the noise level in the sound field, i.e., both the audio output generated by the speaker 5 and the surrounding noises are converted into electric signals by a microphone 6 before being amplified by a pre-amplifier 7. The output signal of the pre-amplifier 7 and the audio signal
10 of the low-frequency power amplifier 4 are applied to a subtraction circuit 8, which comprises an operational amplifier, so that the audio signal is offset to generate only the surrounding noise component at the output of the subtraction circuit 8. The output signal of this
15 subtraction circuit 8 is converted into a D.C. signal by the action of an envelope detector 9 and an integrating circuit 10 so that the control signal of the variable gain circuit 3 is produced.

20 The noise detector, which comprises the microphone 6, the pre-amplifier 7, the subtraction circuit 8, the envelope detector 9 and the integration circuit 10, has its output signal transmitted under normal conditions to the variable gain circuit 3 through a control circuit 12. The gain of the variable gain circuit 3 is controlled

in accordance with the level of the D.C. signal output from the integration circuit 10, so that the level of the audio signal which is applied to the speaker 5 is controlled in proportion to the surrounding noise level of the sound field.

Thus, in the case where the surrounding noise level of the sound field is high, the speaker 5 is fed with the audio output signal at a high level from the output terminal of the power amplifier 4. In the case where the surrounding noise level of the sound field is relatively low, the speaker 5 is fed with the audio output signal at a relatively low level.

In accordance with the inventive concept of the present invention, a received level detector 11 for detecting the level which is dependent upon the received signal level of the antenna ANT is especially connected with the high-frequency circuit 1. The output signal of the received level detector 11 is applied to the control circuit 12 whereby the output signal of the received level detector 11 controls the variable gain circuit 3 in dependence upon the reduction in the received signal level of the antenna ANT so that the level of the output signal of the power amplifier 4, which is applied to the speaker 5, is lowered.

It is preferable that the control circuit 12 lowers the level of the output signal of the power amplifier 4, which is impressed upon the speaker 5, only in the case where the output signal of the received level detector 11 falls below a given reference value. This reference value is so set that the control circuit 12 performs the operation to lower the level of the output signal which is applied to the speaker 5, in the case where the road vehicle is travelling in a tunnel in which case the received signal level of the antenna ANT is very weak so that the detected output of the detector 2 contains substantially only the noise component.

Thus, under the conditions of weak field strength signals but high surrounding noises, e.g., under the conditions one would expect in a tunnel, the sound volume output by the speaker can be muted without raising the output sound volume. As a result, the noise contained in the received signals can be prevented from being amplified at a high gain and transmitted to the speaker whereby an automatic sound volume control of high quality can be achieved.

It should be appreciated that the scope of the invention is not limited by the principle outlined above, so that it can cover the case where the gain of the

variable gain circuit 3 is forcibly limited to a very low preset value by the output of the control circuit 12 or to the case where the transmission of the control signal is prevented from influencing the automatic sound volume control, so that the sound volume output by the speaker 5 is at a manually set low level.

The received level detector 11 can be used as a tuning meter driver if it is contained in the radio receiving reproducing system.

Referring now to the circuit diagrams shown in Figures 2A and 2B, there is illustrated an FM/AM receiving reproducing system which is installed in a road vehicle.

The AM radio-frequency signal received by an AM antenna ANT_1 is applied to a second terminal of a first semiconductor integrated circuit IC1 through an AM antenna tuning circuit which comprises capacitors C_{101} and C_{102} , coils L_{101} , L_{102} and L_{103} and a resistor R_{101} . The first semiconductor integrated circuit IC1 is an integrated circuit for an AM tuner and can use the integrated circuit of type HA 1197 which is sold by us.

Figure 3 shows the internal circuit block of a first preferred form of semiconductor integrated circuit

IC1. This first semiconductor integrated circuit IC1 comprises an RF amplifier 51a, a frequency converter 51b, a first intermediate-frequency amplifier 51c, a second intermediate-frequency amplifier 51d, an AM detector 51e, an AGC (automatic gain control) amplifier 51f, a tuning meter circuit 51g and terminals 1 to 16 (hereinafter referred to as the first to sixteenth terminals of the integrated circuit). The RF amplifier 51a has its input terminal connected to a second terminal of the integrated circuit and its output terminal likewise connected to a fourth terminal of the integrated circuit. The RF amplifier 51a has its first and sixteenth terminals earthed for A.C. signals. As shown in Figure 2A, these first and sixteenth terminals are connected to earth through capacitors C_{103} and C_{104} . The fourth terminal of the RF amplifier 51a, which acts as an output terminal, is connected through a capacitor C_{105} to a seventh terminal which acts as the input terminal of the frequency converter 51b. The fourth terminal is also connected with the third terminal through a resistor R_{102} .

The third terminal is supplied with a positive voltage from a voltage source V_{cc} through a filter which comprises a resistor R_{103} and a capacitor C_{106} . The RF amplifier 51a and the frequency converter 51b receive

their power from the voltage source V_{cc} . Between the fifth and sixth terminals, there are connected an oscillation coil OSC CL, capacitors C_{107} , C_{108} , C_{109} and C_{110} and a coil L_{104} , which form part of the frequency converter 51b for determining the local oscillation frequency of a local oscillator. The output terminal of the frequency converter 51b is connected to the fifth terminal of the integrated circuit.

The first intermediate-frequency amplifier 51c has its input and output terminals connected to the eighth and ninth terminals of the integrated circuit respectively. The eighth and fifth terminals are interconnected through the oscillation coil OSC CL, a first intermediate-frequency transformer IFT_1 , a resistor R_{104} and a capacitor C_{111} .

The second intermediate-frequency amplifier 51d has its input terminal connected to the thirteenth terminal of the integrated circuit. The ninth and thirteenth terminals are interconnected through a second intermediate-frequency transformer IFT_2 and a resistor R_{105} . The thirteenth terminal is further connected to earth through a capacitor C_{112} . The output of the second intermediate-frequency amplifier 51d is applied to the input terminal of the AM detector 51e in the integrated

circuit.

The twelfth terminal which acts as the output terminal of the AM detector 51e is connected to AM detection output terminals T_1 and T_2 through an output circuit which comprises a resistor R_{106} and capacitors C_{114} and C_{115} . The twelfth terminal is also connected to the voltage source V_{cc} through a capacitor C_{113} .

The AGC amplifier 51f which is constructed as a direct-current amplifier, has its input terminal connected to the fourteenth terminal of the integrated circuit.

Between the twelfth and fourteenth terminals, there is connected a time constant circuit, which comprises resistors R_{107} and R_{108} and capacitors C_{116} and C_{117} , so

that an AGC voltage is generated at the junction between the resistor R_{108} and the capacitor C_{117} . The AGC voltage thus generated is supplied to the fourteenth terminal (i.e., the input terminal of the AGC amplifier

51f) so that an AGC amplified voltage is generated at the output terminal of the AGC amplifier 51f. The AGC

amplified voltage thus generated is applied to the RF amplifier 51a and the first intermediate-frequency amplifier 51c so that the automatic gain control operation is carried out while controlling the gains of the amplifiers 51a and 51c.

28

The tuning meter circuit 51g is an impedance converter of an emitter follower circuit type and has its input fed with the AGC amplified voltage so that a tuning meter drive voltage is generated at the fifteenth terminal. The tuning meter drive voltage thus generated is applied to a tuning meter TM through a variable resistor R_{109} and a first change-over switch SW_1 .

The eleventh terminal is connected to the positive voltage source V_{cc} , to enable the first intermediate-frequency amplifier 51c, the second intermediate-frequency amplifier 51d, the AM detector 51e, the AGC amplifier 51f and the tuning meter circuit 51g to be supplied with power for their operation.

It should be noted that the AM tuner semiconductor integrated circuit of this kind is disclosed in detail in United States Patent Specification No. 4,030,035.

The FM radio-frequency signal received by an FM antenna ANT_2 is amplified by an RF amplifier 52a of an FM front end 52 and is applied to a mixer 52b. The mixer 52b is supplied with the local oscillation signal which is generated by a local oscillator 52c. Thus, the FM intermediate-frequency signal is obtained from the output terminal of the mixer 52b and is applied to a filter 53.

A second semiconductor integrated circuit IC2 is used for processing the FM intermediate-frequency signal and can make use of an integrated circuit of type HA1137W which is sold by us.

5 Figure 4 shows the internal circuit block of the second semiconductor integrated circuit IC2. This second semiconductor integrated circuit IC2 comprises a first intermediate-frequency amplifier 54a, a second intermediate-frequency amplifier 54b, a third intermediate-
10 frequency amplifier 54c, a quadrature detector 54d, a first level detector 54e, a second level detector 54f, a third level detector 54g, a fourth level detector 54h, a tuning meter circuit 54i, a mute drive circuit 54j, an AFC amplifier 54k, an audio amplifier 54z, a zero
15 volt switch circuit 54m, an audio mute control amplifier 54n, an OR circuit 54o, and terminals 1 to 16 (hereinafter referred to as the first to sixteenth terminals of the second integrated circuit).

20 The second semiconductor integrated circuit IC2 has its first terminal, which acts as an input terminal, supplied with the FM intermediate-frequency signal through the filter 53. The FM intermediate-frequency signal is amplified by the first, second and third intermediate-frequency amplifiers 54a, 54b and 54c which

are connected in cascade. These intermediate-frequency amplifiers operate as an FM limiter, by which the undesired AM signal component contained in the FM intermediate-frequency signal can be removed.

5 The second and third terminals are connected to earth through capacitors C_{118} and C_{119} , respectively, and a capacitor C_{120} is connected between the second and third terminals. A resistor R_{109} is connected between the first and third terminals so that negative feedback
10 is obtained from the third intermediate-frequency amplifier 54c to the first intermediate-frequency amplifier 54a.

 The second terminal is also connected to a second change-over switch SW_2 through a resistor R_{110}
15 and a diode D.

 The output signal of the third intermediate-frequency amplifier 54c is applied to the input of the quadrature detector 54d. A phase shift circuit is in the form of a network consisting of coils L_{105} , L_{106} and
20 L_{107} , capacitors C_{121} and C_{122} and resistors R_{111} and R_{112} and which is connected to the eighth, ninth and tenth terminals of the second semiconductor integrated circuit IC2. The phase shift circuit constitutes the FM detector together with the quadrature detector 54d. The FM

detector of this type is disclosed in IEEE TRANSACTIONS ON BROADCAST AND TELEVISION RECEIVERS, on pages 60 to 65, VOLUME BTR - 13 NUMBER 3, which was published in November, 1967.

5 The first intermediate-frequency amplifier 54a, the second intermediate-frequency amplifier 54b, the third intermediate-frequency amplifier 54c and the ninth terminal are connected to the first level detector 54e, the second level detector 54f, the third level detector
10 54g and the fourth level detector 54h, respectively. These level detectors detect the peak value of the applied signals.

 The outputs of the first, second and third level detectors 54e, 54f and 54g are applied to the
15 tuning meter circuit 54i. The output of the tuning meter circuit 54i is applied to the thirteenth terminal of the integrated circuit. The tuning meter drive voltage from that thirteenth terminal is applied to the tuning meter TM through a variable resistor R_{113} and
20 the first change-over switch SW_1 . The intermediate-frequency amplifiers 54a to 54c, detector 54d, level detectors 54e to 54h and tuning meter circuit 54i are all disclosed in United States Patent Specification Nos. 3,673,499 and 3,701,022.

The other output of the first level detector 54e is applied as an automatic gain control voltage to the RF amplifier 52a of the FM front end 52 through the fifteenth terminal. Between the fifteenth terminal and earth, there is connected a parallel circuit comprising a resistor R₁₁₄ and a capacitor C₁₂₃.

The quadrature detector 54d has its first output signal applied to the automatic frequency control amplifier 54k which in turn has its output signal applied to the local oscillator 52c of the FM front end 52 through the seventh terminal. Thus, since the frequency of the local oscillation signal obtained by the local oscillator 52c is controlled, the FM tuner can perform its stabilized tuning operation without being detuned from a preset radio-frequency signal.

The second output signal of the quadrature detector 54d is a stereo composite signal acting as the FM detection output signal and is transmitted to the sixth terminal through the audio amplifier 54z.

Both the voltage at the seventh terminal and the voltage at the tenth terminal are applied to the zero volt switch circuit 54m. The inter-terminal differential voltage $V_7 - V_{10}$ between the seventh and tenth terminals is reduced to zero volts at the S- characteristic centre

frequency of the FM detector which comprises the phase shift circuit and the quadrature detector 54d. The absolute value of that inter-terminal differential voltage is proportional to the detuned frequency, and the positive and negative polarities of the differential voltage are determined in dependence upon whether the detuned frequency is higher or lower than the centre frequency. Thus, between the seventh and tenth terminals, there is arranged external to the integrated circuit, a network which comprises a centre meter CM, resistors R_{115} and R_{117} , capacitors C_{124} , C_{125} and C_{126} , and a third change-over switch SW_3 .

In the case where the detuned frequency from the centre frequency is within a preset range, and in the case where the absolute value of the inter-terminal differential voltage between the seventh and tenth terminals is equal to or lower than a preset value, the zero volt switch circuit 54m feeds the OR circuit 54o with an output signal at a low level which is substantially equal to earth potential. When the frequency detuned from the centre frequency exceeds the range of the preset value, the zero volt switch circuit 54m feeds the OR switch 54o with an output signal at a high level.

The output of the fourth level detector 54h is

applied to the mute drive circuit 54j. In the case where the level of the FM intermediate-frequency signal to be applied to the first terminal is equal to or higher than a preset value, the mute drive circuit 54j feeds the OR circuit 54o with the output signal at the low level. When the level of the FM intermediate-frequency signal to be applied to the first terminal becomes equal to or lower than the preset value so that the signal-to-noise ratio is substantially reduced, the mute drive circuit 54j feeds the OR circuit 54o with the output signal at the high level.

When at least one of the outputs of the zero volt switch circuit 54m and the mute drive circuit 54j generates the output voltage at the high level, the OR circuit 54o transmits the output voltage at the high level to the twelfth terminal. If both of the outputs of the zero volt switch circuit 54m and the mute drive circuit 54j are at the low level, the voltage at the twelfth terminal is at the low level.

The twelfth terminal is connected to the fifth terminal through a resistor R_{116} , a fourth change-over switch SW_4 and a resistor R_{140} . The junction between the resistor R_{116} and the fourth change-over switch SW_4 is connected to earth through a capacitor C_{124} , whereas

the fifth terminal is connected to earth through parallel capacitors C_{126} and C_{127} .

The fifth terminal is connected to the control input terminal of the audio mute control amplifier $54n$.

5 When the fifth terminal is supplied with voltage at the high level, the output of the audio mute control amplifier $54n$ controls the gain of the audio amplifier $54z$ such that it is brought into a substantial zero condition. On the other hand, when the fifth terminal is supplied
10 with voltage at the low level, the gain of the audio amplifier $54z$ is set to its maximum value.

The fourth change-over switch SW_4 is normally closed at the side marked AUTO. Under this condition, the voltage at the twelfth terminal is transmitted to
15 the fifth terminal. As a result, either in the case where the frequency detuned from the centre frequency exceeds the preset range or in the case where the FM intermediate-frequency signal to be applied to the first terminal is equal to or lower than the preset value, the signal-to-
20 noise ratio is set at a very low condition, the fifth terminal being supplied with voltage at the high level. Thus, in this case, the gain of the audio amplifier $54z$ is substantially reduced to zero. As a result, no stereo composite signal appears at the sixth terminal so

that the audio mute operation is carried out. In the case where neither of the above referred to two conditions are satisfied, the voltage at the fifth terminal is at the low level so that the stereo composite output signal of the quadrature detector 54d is transmitted to the sixth terminal through the audio amplifier 54z which is set at its maximum value of gain.

The sixth terminal is connected to an output network which comprises capacitors C_{128} , C_{129} and C_{130} , and a resistor R_{118} . The fourth, fourteenth and sixteenth terminals are directly connected to earth.

The eleventh terminal is a voltage source supply terminal and is supplied with positive voltage from the voltage source V_{cc} through a filter which comprises a coil L_{108} and a capacitor C_{131} . The thirteenth terminal is connected to earth through a capacitor C_{132} , whereas the twelfth terminal is connected to earth through a parallel circuit comprising a capacitor C_{133} and a resistor R_{119} .

A third semiconductor integrated circuit IC3 is a semiconductor integrated circuit for PLL (phase-lock loop) FM stereo modulation and may consist of an integrated circuit of type HA1196 which is sold by us.

Figure 5 shows the internal circuit block of the

third semiconductor integrated circuit IC3. This third semiconductor integrated circuit IC3 comprises a pre-amplifier 55a, a first phase detector 55b, a first direct-current amplifier 55c, a voltage-controlled oscillator 55d, a first frequency divider 55e, a second frequency divider 55f, a third frequency divider 55g, a second phase detector 55h, a second direct-current amplifier 55i, a lamp driver 55j, a monaural-stereo switch circuit 55k, a stereo demodulator 55z, a first-post amplifier 55m, a second post-amplifier 55n, a stabilized power source supply circuit 55o, a switch 55t, and terminals 1 to 16 (hereinafter referred to as the first to sixteenth terminals of the third integrated circuit).

The second terminal which acts as the input terminal of the third semiconductor integrated circuit IC3 is fed with a stereo composite signal from the sixth terminal of the second semiconductor integrated circuit IC2. This stereo composite signal is amplified by the pre-amplifier 55a and is transmitted to the third terminal. A capacitor C₁₃₄ is connected between the third terminal and the thirteenth terminal so that the stereo composite signal at the output terminal of the pre-amplifier 55a is transmitted to the inputs of the

first and second phase detectors 55b and 55h.

Connected between fourteenth and fifteenth terminals is a low-pass filter which comprises a resistor R_{122} and capacitors C_{135} and C_{136} . The fifteenth terminal which acts as the input terminal to the first direct-current amplifier 55c is supplied with the low-frequency component of the output of the first phase detector 55b through the low-pass filter. The low-frequency component is amplified in a D.C. manner by the first D.C. amplifier 55c and is applied to the oscillation control terminal of the voltage-controlled oscillator 55d. The oscillation controlled terminal is connected to the sixteenth terminal of the third integrated circuit. The sixteenth terminal is connected to earth through a parallel network comprising a capacitor C_{137} and series connected resistors R_{120} and R_{121} . By adjusting the value of resistance of the resistor R_{121} , the free-running oscillation frequency of the voltage-controlled oscillator 55d is controlled. This free-running oscillation frequency should be set to such a frequency which is equal to a value several times as high as the frequency of a pilot signal contained in the stereo composite signal. The frequency of the pilot signal is 19 KHz, and by way of example the free-running

oscillation frequency is preset at a frequency of 76 KHz which is equal to four times the frequency of the pilot signal.

5 Since the first frequency divider 55e generates an output signal having one half the frequency of the input signal, there are generated at two signal lines 55p and 55q two signals having a frequency of about 38 KHz, which are equal in amplitude but opposite in phase to each other.

10 The second frequency divider 55f feeds the first phase detector 55b with the output signal which has one half the frequency of the input signals on the signal lines 55p and 55q. The first phase detector 55b detects the difference between the phase of the
15 pilot signal of 19 KHz, which is contained in the stereo composite signal obtained from the output terminal of the pre-amplifier 55a, and the phase of the output signal of about 19 KHz, which is obtained from the output terminal of the second frequency divider 55f. Since
20 the error output signal of the first phase detector 55b is transmitted to the voltage-controlled oscillator 55d through the low-pass filter and first direct-current amplifier 55c, the output signal of the first frequency divider at the two signal lines 55p and 55q has a

substantially accurate frequency of 38 KHz and a phase which is synchronized with the phase of the pilot signal of 19 KHz. The closed loop, which consists of the first phase detector 55b, low-pass filter, first direct-current amplifier 55c, voltage-controlled oscillator 55d, first frequency divider 55e and second frequency divider 55f, constitutes the so-called "phase-lock loop (PLL)".

The output signal of 38 KHz, which is obtained from the first frequency divider 55e in the phase-lock loop, is fed in phase opposition to each through the two signal lines 55p and 55q to first and second input terminals z_1 and z_2 of the stereo demodulator 55z.

If the FM radio-frequency signal received by the FM antenna ANT_2 is an FM stereo broadcasting signal, there is fed out to the sixth terminal of the second semiconductor integrated circuit IC2 the stereo composite signal, in which there is contained a pilot signal having a frequency of 19 KHz having a preset amplitude.

On the other hand, in the case where the FM radio-frequency signal received by the FM antenna ANT_2 is an FM monaural broadcasting signal, not the stereo composite signal but the FM monaural detected output signal is supplied to the sixth terminal of the second semiconductor integrated circuit IC2. The latter FM monaural detected

output signal no longer contains the pilot signal having a frequency of 19 KHz having a preset amplitude as described above.

In order to detect whether the FM radio-frequency signal received by the FM antenna ANT₂ is the FM stereo broadcasting signal or the FM monaural broadcasting signal, the existence of the pilot signal has to be detected. The third frequency divider 55g and the second phase detector 55h, which are arranged in the third semiconductor integrated circuit IC3, operate as the detector for detecting the existence of the pilot signal. It should be noted that the second phase detector 55h operates as a synchronous detector. During reception of the FM stereo broadcast signal, since the phase of the output signal of 38 KHz of the first frequency divider 55e in the phase-lock loop is in synchronism with that of the pilot signal of 19 KHz in the stereo composite signal, the phase of the output signal of 19 KHz of the third frequency divider 55g likewise synchronizes with that of the pilot signal of 19 KHz in the stereo composite signal under that condition. During reception of the FM stereo broadcast signal, consequently, the second phase detector 55h which acts as a synchronous detector detects the pilot signal of

19 KHz, which is contained in the stereo composite signal applied to the thirteenth terminal in synchronism with the frequency-divided output signal of 19 KHz, which is supplied from the third frequency divider 55g so that the tenth terminal is fed with the detected output signal which is proportional to the amplitude level of the pilot signal of 19 KHz.

During reception of the FM monaural broadcast signal, since the random noise component, which is contained in the FM monaural detected output signal applied to the thirteenth terminal, is applied to the second phase detector 55h, the average level of the output voltage of the second phase detector 55h, which is generated at a tenth terminal, is at earth potential.

A capacitor C_{138} is connected between the tenth terminal and the eleventh terminal, said capacitor C_{138} constituting a part of the low-pass filter. As a result, the low-frequency component of the output of the second phase detector 55h is transmitted to the eleventh terminal acting as the input terminal of the second direct-current amplifier 55i.

The stereo-monaural switch circuit 55k has its control input terminal connected to the twelfth terminal of the third integrated circuit. In the case where the

twelfth terminal is fed with the control voltage at a high level, the output signal of the stereo-monaural switch circuit 55k inhibits the amplification of the second direct-current amplifier 55i. On the contrary,

5 in the case where the control voltage at the low level is applied to the twelfth terminal, the second direct-current amplifier 55i operates normally. The twelfth terminal is connected to the fourth change-over switch SW₄ through a resistor R₁₂₃.

10 The lamp driver 55j has an input threshold value which has to be exceeded by the output signal of the second direct-current amplifier 55i in order to energize a lamp 56. In the case where the output signal of the second direct-current amplifier 55i is at a level
15 having a value which exceeds that threshold, the lamp driver 55j turns on the stereo indicator lamp 56 which is connected to the ninth terminal through a resistor R₁₂₄. The energization of the stereo indicator lamp 56 indicates that the FM tuner is receiving the FM stereo
20 broadcast signal. On the contrary, the non-energization of the stereo indicator lamp 56 indicates not only that the FM tuner is receiving the FM monaural broadcast signal but also that it is operating under one of the two following conditions.

More specifically, in the case where the fourth change-over switch SW_4 is closed on the side marked MONO, the positive voltage of the voltage source V_{cc} is applied as the control signal at the high voltage level to the
5 twelfth terminal through the switch SW_4 and the resistor R_{123} . Thus, since the output signal of the stereo-monaural switch circuit $55k$ inhibits the amplification of the second direct-current amplifier $55i$, the lamp driver $55j$ partly turns off the stereo indicator lamp 56, which
10 is connected to the ninth terminal, and partly controls the switch $55t$, which is connected between the second output signal line $55q$ of the first frequency divider $55e$ and the second input terminal z_2 of the stereo demodulator $55z$ into its open state. Since the output
15 signal of 38 KHz appearing on the first output signal line $55p$ of the first frequency divider $55e$ drives the first and second input terminals z_1 and z_2 of the stereo demodulator $55z$ in in-phase mode through resistors r_1 and r_2 , the stereo demodulation of the stereo demodulator
20 $55z$ is not operational.

On the other hand, in the case where the fourth change-over switch SW_4 is closed on the side marked AUTO, the voltage at the twelfth terminal of the second semiconductor integrated circuit IC2 is applied to the

twelfth terminal of the third semiconductor integrated circuit IC3 through the fourth change-over switch SW₄ and through the resistor R₁₁₆. Either in the case where the level of the FM intermediate-frequency signal applied to the first terminal of the second semiconductor integrated circuit IC2 becomes equal to or lower than a preset value so that the signal-to-noise ratio is substantially reduced or in the case where the detuned frequency from the S-characteristic centre frequency of the FM detector exceeds a preset value, there appears an output voltage of a high level at the twelfth terminal of the second semiconductor integrated circuit IC2. As a result, the gain of the audio amplifier 54z of the second semiconductor integrated circuit IC2 is reduced to substantially zero, and at the same time the lamp driver 55j of the third semiconductor integrated circuit IC3 partly turns out the stereo indicator lamp 56 and partly controls the switch 55t, which is connected between the second output signal line 55q of the first frequency divider 55e and the second input terminal z2 of the stereo demodulator 55z, into its open condition.

On the other hand, in the case where the lamp driver 55j turns on the stereo indicator lamp 56, it moves the switch 55t to its closed state. The anti-phase output signal of 38 KHz at the first and second

output signal lines 55p and 55q of the first frequency divider 55e drives the first and second input terminals $\underline{z}_1$ and $\underline{z}_2$ of the stereo demodulator 55z in phase opposition. The first and second input terminals $\underline{z}_1$ and $\underline{z}_2$ which are driven in phase opposition by the signal of 38 KHz so that the stereo demodulator 55z can achieve its stereo switching demodulation.

The other input terminal $\underline{z}_3$ of the stereo demodulator 55z is fed with the stereo composite signal from the pre-amplifier 55a, and the first and second input terminals $\underline{z}_1$ and $\underline{z}_2$ are supplied with the switching signals of 38 KHz in phase opposition so that the stereo demodulator 55z outputs a left-channel demodulated output signal and a right-channel demodulated output signal to a first output terminal 55r and a second output terminal 55s respectively. A stereo demodulator of this switching type is disclosed in IEEE TRANSACTIONS ON BROADCAST AND TELEVISION RECEIVERS, on pages 58 to 73, VOLUME BTR - 14 NUMBER 3.

Moreover, the semiconductor integrated circuit for FM stereo demodulation, which uses the phase-lock loop, is disclosed in the publication Electronics, (November 1971) on pages 62 to 66.

The left- and right-channel demodulated signals

at the first and second output terminals $55r$ and $55s$ of the stereo demodulator $55z$ are amplified by the first and second post-amplifiers $55m$ and $55n$ respectively, and are transmitted to the seventh and sixth terminals respectively. The first and second post-amplifiers $55m$ and $55n$ are supplied with negative feedback signals on respective fourth and fifth terminals of the integrated circuit. The first, fourth and seventh terminals are connected with a network, which comprises resistors R_{125} , R_{126} and R_{127} and capacitors C_{138} and C_{139} , which enable the gain of the first post-amplifier $55m$ to be controlled. Likewise, the first, fifth and sixth terminals are connected with a network which comprises resistors R_{128} , R_{129} and R_{130} and capacitors C_{140} and C_{141} , which enable the gain of the second post-amplifier $55n$ to be controlled.

The left-channel demodulated output signal, which is obtained from the seventh terminal, is transmitted to a terminal T_3 through a capacitor C_{142} , a resistor R_{131} and a low-pass filter 57, whereas the right-channel demodulated output signal, which is obtained from the sixth terminal, is transmitted to a terminal T_4 through a capacitor C_{143} , a resistor R_{132} and a low-pass filter 58. The terminals T_3 and T_4 are connected to earth

through resistors R_{133} and R_{134} , respectively. The first terminal of the third semiconductor integrated circuit IC3 is supplied with the positive voltage of the voltage source V_{cc} so that the stabilized power source supply circuit 55g feeds the stabilized operation voltage to the interior of the third semiconductor integrated circuit IC3.

The oscillation control terminal of the voltage-controlled oscillator 55d is connected to the sixteenth terminal of the integrated circuit and is connected to earth through a resistor R_{135} and the collector-emitter path of a transistor TR1. The AM side terminal of the second change-over switch SW_2 is connected to earth through resistors R_{136} and R_{137} . Moreover, the junction point of the resistors R_{136} and R_{137} is connected to the base electrode of the transistor TR1.

During an AM broadcast, since the second change-over switch SW_2 is closed on the AM side, there is generated at the junction point between the resistors R_{136} and R_{137} a divided voltage which is determined by dividing the positive voltage V_{cc} in the ratio of the resistances of the resistors R_{136} and R_{137} . The voltage thus divided renders the transistor TR1 conductive so that the potential at the sixteenth terminal is at a relatively

low level. Thus, the sixteenth terminal of the third semiconductor integrated circuit IC3 is preset at a relatively low potential so that the oscillating operation of the voltage-controlled oscillator 55d of the integrated circuit IC3 is inhibited. Thus, the circuit operation of the phase-lock loop in the third semiconductor integrated circuit IC3 is stopped during an AM broadcast.

During an FM broadcast, since the second change-over switch SW_2 is closed at the FM side, the positive voltage of the voltage source V_{cc} is fed to the local oscillator 52c in the FM front end 52 through the second change-over switch SW_2 . Thus, the operation of the FM front end 52 is achieved.

During an AM broadcast, a fifth change-over switch SW_5 makes contact with the terminal T_1 , and a sixth change-over switch SW_6 makes contact with the terminal T_2 . The terminals T_1 and T_2 are fed with the AM detected output signal which is obtained from the twelfth terminal of the first semiconductor integrated circuit IC1.

During an FM broadcast, the fifth change-over switch SW_5 makes contact with the terminal T_3 , and the sixth change-over switch SW_6 makes contact with the terminal T_4 . The terminal T_3 is supplied with the left-channel demodulated output signal from the seventh terminal of the third

semiconductor integrated circuit IC3. On the other hand, the terminal T_4 is supplied with the right-channel demodulated output signal from the sixth terminal of the third semiconductor integrated circuit IC3.

5 A fourth semiconductor integrated circuit IC4 shown in Figure 2B is a semiconductor integrated circuit for a voltage-controlled attenuator, which is used as a variable gain circuit. This integrated circuit is disclosed in detail in British Patent Application No.
10 80.17243 published under Serial No. .

15 The fourth semiconductor integrated circuit IC4 has first, sixth, tenth, eighth, thirteenth and third terminals which respectively act as a first signal input terminal, a second signal input terminal, a first signal output terminal, a second signal output terminal, a first control input terminal and a second control input terminal. The signal transmission from the first
20 signal input terminal to the first signal output terminal can be controlled by the control voltage which is applied to the first control input terminal. Likewise, the signal transmission from the second signal input terminal to the second signal output terminal can be controlled by the second control voltage.

Referring now to Figure 6, the fourth semiconductor

integrated circuit IC4 includes a first operational amplifier 59a, a first level shift circuit 59b, a first transistor network 59c, a second operational amplifier 59d, a third operational amplifier 59e, a second level shift circuit 59f, a second transistor network 59g, a fourth operational amplifier 59h and a fifth operational amplifier 59i.

The first operational amplifier 59a has its inverting input terminal (-) and non-inverting input terminal (+) connected to the first and second terminals, respectively. The second terminal is connected to earth externally of the integrated circuit.

The output signal of the first operational amplifier 59a is applied to the first transistor network 59c through level shift elements 591 and 592 of the first level shift circuit 59b.

The first transistor network 59c comprises NPN transistors Q_1 and Q_3 and PNP transistors Q_2 and Q_4 . The transistors Q_1 and Q_2 have their collector electrodes connected in common with the inverting input terminal (-) of the first operational amplifier 59a. The transistors Q_3 and Q_4 have their collector electrodes connected in common with the inverting input terminal (-) of the second operational amplifier 59d. The base electrodes

of the transistors Q_2 and Q_3 are connected to the second terminal, whilst the base electrodes of the transistors Q_1 and Q_4 are connected to the thirteenth terminal.

5 The second operational amplifier $59d$ has its inverting input terminal (-) connected to the commoned collector electrodes of the transistors Q_3 and Q_4 and to the ninth terminal of the integrated circuit. The non-inverting input terminal (+) and the output terminal of the second operational amplifier $59d$ are
10 connected with a second terminal and the tenth terminal, respectively.

The third operational amplifier $59e$ has its inverting input terminal (-) and non-inverting input terminal (+) connected with the sixth and second terminals,
15 respectively. The output of the third operational amplifier $59e$ is connected to the second transistor network $59g$ through level shift elements 593 and 594 of the second level shift circuit $59f$.

The second transistor network $59g$ comprises NPN
20 transistors Q_5 and Q_7 and PNP transistors Q_6 and Q_8 . The transistors Q_5 and Q_6 have their collector electrodes connected in common with the inverting input terminal (-) of the third operational amplifier $59e$. The transistors Q_7 and Q_8 have their collector electrodes

connected in common to the inverting input terminal (-) of the fourth operational amplifier 59h. The base electrodes of the transistors Q_6 and Q_7 are connected to the second terminal, whilst the base electrodes of the transistors Q_5 and Q_8 are connected to the third terminal.

The fifth operational amplifier 59i, which is not used in the present embodiment, is arranged inside the integrated circuit and has its inverting input terminal (-), non-inverting input terminal (+) and output terminal connected with a fourth terminal, the second terminal and a fifth terminal, respectively.

Outside the integrated circuit, the first and sixth terminals are connected with the fifth change-over switch SW_5 and the sixth change-over switch SW_6 , respectively, through resistors R_{138} and R_{139} . Also the thirteenth and third terminals are connected in common and supplied with a control voltage V_c .

A positive voltage $+V_{cc}$ and a negative voltage $-V_{cc}$ are supplied to the five operational amplifiers 59a, 59d, 59e, 59h and 59i through the eleventh and twelfth terminals, respectively.

A resistor R_{141} and a capacitor C_{144} are connected in parallel between the ninth and tenth terminals, whilst a resistor R_{142} and a capacitor C_{145} are connected

in parallel between the seventh terminal and eighth terminals.

Such relationships as are expressed by the following equations hold, for a first input signal current i_{in} which flows through the first terminal, a second input signal current i'_{in} which flows through the sixth terminal, a first output signal current i_{out} which flows through the ninth terminal, a second output signal current i'_{out} which flows through the seventh terminal, the absolute value $|V_c|$ of the control voltage V_c at the thirteenth and third terminals, a first input signal voltage v_{in} at one end of the resistor R_{138} , a second input signal voltage v'_{in} at one end of the resistor R_{139} , a first output signal voltage v_{out} at the tenth terminal, and a second output signal voltage v'_{out} at the eighth terminal:

$$i_{out} = i_{in} \cdot \exp \frac{q(-|V_c|)}{kT} \quad (1);$$

$$i'_{out} = i'_{in} \cdot \exp \frac{q(-|V_c|)}{kT} \quad (2);$$

$$v_{in} = R_{138} \cdot i_{in}, \quad v'_{in} = R_{139} \cdot i'_{in} \quad (3);$$

and

$$v_{out} = R_{141} \cdot i_{out}, \quad v'_{out} = R_{142} \cdot i'_{out} \quad (4).$$

As will be apparent from the above description, the first and second output signal voltages v_{out} and v'_{out} at the tenth and eighth terminals exponentially decrease with an increase in the absolute value $|V_c|$ of the control voltage V_c .

The first output signal voltage v_{out} is transmitted to the input terminal of a first power amplifier 60 through a tone control capacitor C_{146} , a variable resistor R_{143} and a sound volume adjusting variable resistor R_{145} . A first speaker 61 for the left hand channel of the stereo system is driven by the amplified output signal of the first power amplifier 60.

Likewise, the second output signal voltage v'_{out} is transmitted to the input terminal of a second power amplifier 62 through a tone control capacitor C_{147} , a variable resistor R_{144} and a sound volume adjusting variable resistor R_{146} . A second speaker 63 for the right hand channel of the stereo system is driven by the amplified output signal of the second power amplifier 62.

As shown in Figures 2A and 2B, the tuning meter TM is connected to the non-inverting input terminal (+) of an operational amplifier 64 which acts as a voltage comparator. The inverting input terminal (-) of the

operational amplifier 64 is supplied with a reference voltage V_{REF} . In order to generate this reference voltage V_{REF} , a resistor R_{147} and a zener diode ZD are connected in series between the positive voltage source + V_{cc} and earth. A variable resistor R_{148} is connected in parallel with the both ends of the zener diode ZD so that the reference voltage V_{REF} can be obtained from the tap of the variable resistor R_{148} .

The output terminal of the operational amplifier 64 is connected to a control input terminal 69 of a seventh change-over switch SW_7 . When the control input terminal 69 is supplied with a voltage at the high level, the seventh change-over switch SW_7 transmits only a voltage, which is applied to a first input terminal 70, to an output terminal 72. On the other hand, when the control input terminal 69 is supplied with a voltage at the low level, the seventh change-over switch SW_7 transmits only the voltage, which is applied to a second input terminal 71, to the output terminal 72. The seventh change-over switch SW_7 comprises a first switch unit 65 and a second switch unit 66.

These first and second switch units 65 and 66 are constituted by a CMOS analog switch. The first switch unit 65 comprises an N channel MOSFET 65a and a

P channel MOSFET 65b, the source-drain paths of which are connected in parallel, and a first inverter 65c which is connected between the gate electrodes of the two MOSFETs 65a and 65b. Likewise, the second switch unit 5 66 comprises an N-channel MOSFET 66a and a P channel MOSFET 66b, the source-drain paths of which are connected in parallel and a second inverter 66c which is connected between the gate electrodes of the two MOSFETs 66a and 66b.

10 The first input terminal 70 of the seventh change-over switch SW₇ is connected to an output terminal 67a of a noise detector 67 for detecting the noise in a sound field 68. The second input terminal 71 of the seventh change-over switch SW₇ is supplied with the 15 positive voltage V_{cc} so as to carry out a forced attenuation.

20 A first microphone 67b and a second microphone 67c of the noise detector 67 are arranged in the sound field 68 extending in the passenger compartment of the road vehicle. The surrounding noises such as the engine noise from the engine compartment of the road vehicle or the road noises outside of the vehicle are transmitted to the sound field 68 or the passenger compartment of the vehicle. These surrounding noises exhibit

relatively large changes.

The noise detector 67 further comprises a first pre-amplifier 67d, a second pre-amplifier 67e, a first operational amplifier 67f, a second operational amplifier 67g, a first envelope detector 67h, a second envelope detector 67i, a first integration circuit 67j, a second integration circuit 67k and an adder 67z. The adder 67z comprises resistors R_{149} , R_{150} and R_{151} , an inverting amplifier 73 and a level shift circuit 74.

The output signal of the first microphone 67b and the output signal of the second microphone 67c are transmitted through the first and second pre-amplifiers 67d and 67e, respectively, to the non-inverting input terminal (+) of the first operational amplifier 67f and the non-inverting input terminal (+) of the second operational amplifier 67g.

The output signal of the first operational amplifier 67f and the output signal of the second operational amplifier 67g are transmitted to the adder 67z through the first envelope detector 67h and the first integration circuit 67j and through the second envelope detector 67i and the second integration circuit 67k, respectively.

The adder 67z is in the form of an analog adder

comprising resistors R_{149} , R_{150} and R_{151} , an inverting amplifier 73 and a level shift circuit 74. The adder 67z supplies the output terminal 67a with the output component which is the summation of the output of the first microphone 67b and the output of the second microphone 67c.

According to the preferred embodiment, the audio amplified signal of the first power amplifier 60 is applied to the inverting input terminal (-) of the first operational amplifier 67f, whereas the audio amplified signal of the second power amplifier 62 is applied to the inverting input terminal (-) of the second operational amplifier 67g. As a result, the first and second operational amplifiers 67f and 67g offset the audio amplified signal, which is contained in the output signal of the first pre-amplifier 67d, and the audio amplified signal, which is contained in the output signal of the second pre-amplifier 67e, in response to the audio amplified signals which are applied to their respective inverting input terminals (-). Thus, neither the audio signal of the first speaker 61 nor the audio signal of the second speaker 63 are substantially transmitted to the output terminal 67a of the noise detector 67, but the surrounding noise component in the sound field 68 or the

passenger compartment are transmitted to the output terminal 67a.

Such relationships as are expressed by the following equation hold for a noise detection signal voltage v_j at the output terminal of the first integration circuit 67j, a noise detection signal voltage v_k at the output terminal of the second integration circuit 67k, and a voltage v_{73} at the output terminal of the inverting amplifier 73:

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$$v_{73} = - \left[\frac{R_{151}}{R_{149}} v_k + \frac{R_{151}}{R_{150}} v_j \right] \text{ --- (5).}$$

If the values of resistance of the resistors R_{149} , R_{150} and R_{151} are preset equal to one another, the voltage v_{73} is given by the following equation:

$$v_{73} = - (v_k + v_j) \text{ --- (6).}$$

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As a result, the relationship between the output voltage v_{73} of the inverting amplifier 73 and the surrounding noise level N_L of the sound field 68 or the passenger compartment is as illustrated in Figure 7. The output voltage v_{73} in the case where the surrounding noise level N_L of the sound field 68 is low is substantially at zero, whereas the output voltage v_{73} in the case where

the surrounding noise level N_L is high is at a negative potential level. The level shift circuit 74 feeds the output terminal 67a with an output voltage v_{74} which has its level shifted by a preset potential from the output voltage v_{73} , but the minimum potential of the output voltage v_{74} is limited to zero. The relationship between the output voltage v_{74} of the level shift circuit 74 and the surrounding noise level N_L of the sound field 68 is likewise illustrated in Figure 7.

The first change-over switch SW_1 connected to the tuning meter TM is closed at the AM side during the AM broadcast reproduction and is closed at the FM side during the FM broadcast reproduction. As a result, the tuning meter TM is fed with either that component of the AM broadcast received signal, which is dependent upon the level of the AM detected output signal, or that component of the FM broadcast received signal, which is dependent upon the level of the FM intermediate-frequency signal. In the case where the AM or FM broadcast signal under the preferred condition is being received, the tuning meter TM is supplied with the tuning meter drive voltage which is proportional to the level of the received signal.

Under this preferred condition, the tuning meter drive voltage is at a higher level than the reference

voltage V_{REF} which is applied in advance to the inverting input terminal (-) of the operational amplifier 64 which acts as a voltage comparator. Under this condition, the output voltage at the output terminal of the operational amplifier 64, which is connected with the control input terminal 69 of the seventh change-over switch SW_7 , is at the high level so that the seventh change-over switch SW_7 has its first switch unit 65 turned on and its second switch unit 66 turned off. As a result, the output voltage V_{74} at the output terminal 67a of the noise detector 67 is fed through the output terminal 72 of the seventh change-over switch SW_7 to the third and thirteenth terminals of the fourth semiconductor integrated circuit IC4.

Under this preferred condition, in the case where the surrounding noise level N_L of the sound field or the passenger room is high, the output voltage V_{74} of the noise detector 67, which is fed to the third and thirteenth terminals of the fourth semiconductor integrated circuit IC4, is substantially at zero so that the signal attenuation during the signal transmission from the first terminal to the tenth terminal and during the signal transmission from the sixth terminal to the eighth terminal is very low. As a result, in the case where the surrounding noise level

N_L of the sound field 68 is high, the first and second speakers 61 and 63 are driven by the audio amplified output signal at the high level.

5 Under these conditions, when the surrounding noise level N_L of the sound field 68 or the passenger compartment is lowered, the output voltage v_{74} is raised to the high level so that the signal attenuation during the signal transmission from the first terminal to the tenth terminal and during the signal transmission from the sixth terminal to the eighth terminal is increased. 10 As a result, when the surrounding noise level N_L of the sound field 68 is lowered, the first and second speakers 61 and 63 are driven by the audio amplified output signal at the low level.

15 On the contrary, in the case where the road vehicle is travelling in a tunnel, neither the AM radio-frequency signal nor the FM radio-frequency signal are received by the AM and FM antennae ANT_1 and ANT_2 . As a result, the tuning meter TM is fed with a low voltage 20 which is the noise component.

During the period when the road vehicle is within the tunnel, the only signal which appears in the AM detected output signal, which is obtained from the twelfth terminal of the first semiconductor integrated circuit and which is

fed to the terminal T_1 of the fifth change-over switch SW_5 and to the terminal T_2 of the sixth change-over switch SW_6 , is the noise component. Moreover, the audio muting operation is carried out, at the second semiconductor integrated circuit IC2 by the control of the audio mute control amplifier 54n so that only the noise component appears at the sixth terminal. The noise component at the sixth terminal of the second semiconductor integrated circuit IC2 is transmitted to the second terminal of the third semiconductor integrated circuit IC3. This noise component transmitted to the second terminal does not contain any substantial pilot signal component at 19 KHz.

The stereo demodulator 55z of the third semiconductor integrated circuit IC3 does not carry out the stereo switching demodulation but transmits that noise component of the second terminal, which is amplified by the pre-amplifier 55a, to the first and second post-amplifiers 55m and 55n. As a result, the noise component, which is further amplified by the post-amplifiers, appears at the seventh and sixth terminals of the integrated circuit IC3 so that it appears at the terminal T_3 of the fifth change-over switch SW_5 and at the terminal T_4 of the sixth change-over switch SW_6 .

The fifth and sixth change-over switches SW_5 and SW_6 are selectively closed on either the AM or FM side. In either selection, the noise component is transmitted to the first and sixth terminals of the fourth semiconductor integrated circuit IC4. If, under this condition, the seventh change-over switch SW_7 has its first switch unit 65 maintained in the conductive state and its second switch unit 66 maintained in the non-conductive state, an undesirable audible feeling results, as follows.

Specifically, the noise component, which is transmitted from the first terminal to the tenth terminal of the fourth semiconductor integrated circuit IC4, and the noise component, which is transmitted from the sixth terminal to the eighth terminal, are amplified by the first and second power amplifiers 60 and 62, respectively, and are then transmitted to the first and second speakers 61 and 63, respectively. When the surrounding noise level N_L of the sound field 68, which is dependent upon the engine noise or the road noise, is raised, the output voltage v_{74} at the output terminal 67a of the noise detector 67 is lowered to earth or zero potential so that the attenuation during the signal transmission from the first terminal to the tenth terminal and during the signal

transmission from the sixth terminal to the eighth terminal is lowered. In this case, an undesired phenomena results in that the noise voltages dependent upon the noise components supplied to the first and sixth terminals are generated at high levels from the first and second speakers 61 and 63, respectively.

In order to prevent these undesirable effects, the tuning meter drive voltage of the tuning meter TM is applied to the non-inverting input terminal (+) of the operational amplifier 64. During the period whilst the road vehicle is within the tunnel, the tuning meter drive voltage falls to such a low value that its level becomes equal to or lower than the reference voltage V_{REF} .

As a result, the output voltage of the operational amplifier 64, which is connected with the control input terminal 69 of the seventh change-over switch SW_7 , takes a low level so that the seventh change-over switch SW_7 has its first switch unit 65 rendered non-conductive and its second switch unit 66 rendered conductive. Thus, the positive power source voltage $+V_{CC}$, which is fed to the second input terminal 71 of the seventh change-over switch SW_7 , is fed through the output terminal 72 of that switch SW_7 to the third and thirteenth terminals of the

fourth integrated circuit IC4, so that the signal attenuation during the signal transmission from the first terminal to the tenth terminal of the integrated circuit IC4 and during the signal transmission from the sixth terminal to the eighth terminal becomes substantially high.

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Thus during the period whilst the vehicle is travelling in the tunnel, little noise voltage is generated from the first and second speakers 61 and 63 so that the undesired effects described above can be prevented.



CLAIMS.

1. A radio receiving reproducing system including:

(a) an AM tuner for obtaining an AM detected output signal from an AM radio-frequency signal;

5 (b) an FM front end for obtaining an FM intermediate frequency signal from an FM radio-frequency signal;

(c) an FM intermediate-frequency signal processing circuit for obtaining an FM detected output signal from said FM intermediate-frequency signal;

10 (d) an FM stereo demodulator for obtaining a left-channel demodulated output signal and a right-channel demodulated output signal from said FM detected output signal;

(e) a first terminal which can be supplied by way of a selection means with a selected one of said AM
15 detected output signal and said left-channel demodulated output signal;

(f) a second terminal which can be supplied by way of said selection means with a selected one of said AM detected output signal and said right-channel demodulated
20 output signal;

(g) a first voltage-controlled attenuator having an input terminal, a control terminal and an output terminal, the signal transmission from said input terminal to said output terminal being controllable by
25 a control voltage applied to said control terminal and said input terminal being connected to said first terminal;

(h) a second voltage-controlled attenuator



having an input terminal, a control terminal and an output terminal, the signal transmission from said input terminal to said output terminal being controllable by a control voltage applied to said control terminal and said input
5 terminal being connected to said second terminal;

(i) a first power amplifier the input terminal of which is connected with said output terminal of said first voltage-controlled attenuator;

(j) a second power amplifier the input terminal
10 of which is connected with said output terminal of said second voltage-controlled attenuator;

(k) a first speaker which is driven by the output signal of said first power amplifier;

(l) a second speaker which is driven by the
15 output signal of said second power amplifier;

(m) noise detector means for detecting the surrounding noise level of a sound field;

(n) received level detector means for detecting an AM level which is dependent upon said AM radio-
20 frequency signal as well as an FM level which is dependent upon said FM radio-frequency signal; and

(o) control means responsive to an output signal of said received level detector means and connected between the output terminal of said noise detector means
25 and both of said control terminals of said first and second voltage controlled attenuators, said control means for transmitting the detected output of said noise detector means to both of said control terminals of said first



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and second voltage controlled attenuators in the case where the output signal of said received level detector means is higher than a preset value so as to control said output signals of said first and second power amplifiers proportionally in accordance with said surrounding noise level of said sound field and said control means forcibly lowering the level of said output signals of said first and second power amplifiers in the case where said output signal of said received level detector means is lower than said preset value, thereby disabling sound field effects on said power amplifier output signals.

2. A radio receiving reproducing system according to claim 1, wherein said noise detector means includes: a microphone; a pre-amplifier for amplifying the output signal of the microphone; a subtraction circuit connected to receive the output signal of the pre-amplifier and an audio signal of one of the power amplifiers, a detector connected to the output of the subtraction circuit, and an integration circuit connected to the output of the detector, the output signal of the integration circuit being utilized as an output signal of the noise detector means.

3. A radio receiving reproducing system according to claim 1 or 2, wherein said received level detector means is also utilized as a tuning meter driver, and includes a tuning meter circuit in the AM tuner and a tuning meter circuit in the FM intermediate-frequency signal processing circuit.



4. A radio receiving reproducing system according to claim 3, wherein said control means includes: a voltage comparator which is supplied with a drive voltage from said tuning meter circuits; and a reference voltage which corresponds to said preset value.
5. A radio receiving reproducing system according to any one of the preceding claims, wherein at least the antenna, the speaker, and the noise detector means are carried on a road vehicle.
- 10 6. A radio receiving reproducing system according to any one of the preceding claims wherein the FM intermediate-frequency signal processing circuit includes audio mute control amplifier means for causing said FM detected output signal to become zero when the level
- 15 of the FM intermediate frequency signal is lower than a predetermined value.
7. A radio receiving reproducing system constructed and arranged to operate substantially as herein described with reference to and as illustrated in Figures 2A, 2B,
- 20 3, 4, 5 and 6 of the accompanying drawings.

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